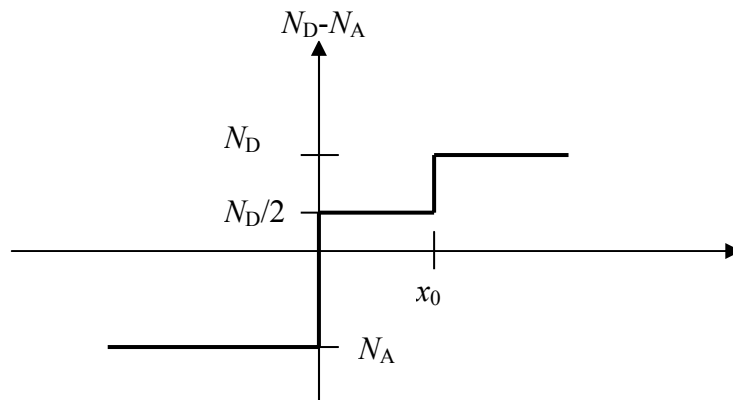


ECSE-2210 Microelectronics Technology Homework 4

Reading list: Chapter 5 (pages 195 - 223. Ignore section 5.2.5).

1. (Problem 5.4 in text) A Si step junction under equilibrium at 300 K has a p-side doping of $N_A = 2 \times 10^{15} \text{ cm}^{-3}$ and n-side doping of $N_D = 10^{15} \text{ cm}^{-3}$. Calculate:
 - (a) The contact potential (also called built-in voltage).
 - (b) The depletion layer width at the p-side and n-sides, and the total depletion layer width.
 - (c) The electric field at the metallurgical junction.
 - (d) The potential at the metallurgical junction.
 - (e) Make sketches of the charge density, electric field and electrostatic potential as a function of position, that are roughly to scale
2. (Problem 5.5 in text) Repeat problem 1 taking $N_A = 10^{17} \text{ cm}^{-3}$ to be the p-side doping. Briefly compare the results here with those obtained in problem 1.
3. (Problem 5.10 in text). A p-n junction diode has the doping profile sketched below. Make the assumption that $x_n > x_0$ for all applied bias of interest. Answer the following:
 - a. What is the built-in voltage across the junction? Justify your answer.
 - b. Sketch the charge density ρ versus x inside the diode
 - c. Sketch the expected electric field as a function of x inside the diode.



4. The p-i-n diode shown above is a three-region device with the middle region that is intrinsic and relatively narrow. Assuming the p- and n-regions to be uniformly doped and $N_D - N_A = 0$ in the i-region:
 - a. Roughly sketch the expected charge density, electric field, and electrostatic potential inside the device. Also, draw the energy band diagram for the device under thermal equilibrium conditions.
 - b. What is the built-in voltage drop between the p- and n-regions? Show how you arrived with your answer.

