ISPSD'08

SCHEDULE AT A GLANCE

SHORT COURSE : SUNDAY, MAY 18, 2008	
7:00-8:00 AM	**Short Course Registration**
	Short Course:
5:00-6:00 PM	**ISPSD'08 Early Registration**
MONDAY , MAY 19, 2008	
7:00 AM	**Registration**
8:30-8:45 AM	Opening Remarks and Announcements
8:45-11:00 AM	**Session 1:** Plenary
8:45-9:30 AM	**Plenary 1:** Environmental Trends and Opportunities for Computer Power Delivery
9:30-10:15 AM	**Plenary 2:** A New AC Current Switch Called MERS with Low On-State Voltage IGBTs (1.54 V) for Renewable Energy and Power Saving Applications
10:15-11:00 AM	**Plenary 3:** From Packaging to "Un"-Packaging – Trends in Power Semiconductor Modules
11:00AM-1:30 PM	Lunch Break
1:30-3:10 PM	**Session 2:** Trench MOSFETS and Lateral IGBT
3:10-3:30 PM	Coffee Break
3:30-5:10 PM	**Session 3:** Novel High Voltage Devices
6:00-8:00PM	**Welcome Reception**
TUESDAY , MAY 20, 2008	
8::00 AM	**Registration**
8:30-10:10 AM	**Session 4:** Integration Technologies
10:10-10:30 AM	Coffee Break
10:30AM-12:10 PM	**Session 5 :** IGBT & Diode
1**2:10-1:00 PM**	**Lunch Reception**
1:00-4:00 PM	**Session 6:** POSTER SESSION
4:15-9:00PM	**Arabian Night Dinner Show**
WEDNESDAY, MAY 21, 2008	
8:30-10:10 AM	**Session 7:** SiC Power Diodes, Switches & Packaging
10:10-10:30 AM	Coffee Break
10:30 AM-12:10 PM	**Session 8:** Integrated LDMOS
12:10-2:00 PM	Lunch Break
2:00-3:15 PM	**Session 9:** GaN Power HEMT/MOS Devices
7:00-9:00PM	**Conference Banquet**
THURSDAY, MAY 22, 2008	
8:30-10:10 AM	**Session 10:** Superjunction & Termination Technology
10:10-10:30 AM	Coffee Break
10:30 A-12:10 PM	**Session 11:** Power IC Applications
12:10-12:30 PM	**Closing Ceremonies/Charitat Award**
6:00-9:00 PM	**Committee Dinner**

CONFERENCE ORGANIZING COMMITTEE

General Chair:

T. P. Chow	Renessalear Polytechnic Institute, USA

Vice General Chair:

J. Millan	CNM, Spain
Y. Seki	Fuji Electric, Japan

Technical Program Committee Chair:

M. Darwish	MaxPower Semiconductor, USA

Program Committee Vice Chair:

H.R. Chang	International Rectifier, USA
D. Disney	Advanced Analogic Technologies, USA
G. Dolny	Fairchild Semiconductor, USA
D. Kinzer	Fairchild Semiconductor, USA

Publicity Chair:

D. Disney	Advanced Analogic Technologies, USA

Local Arrangements Chair:

J. Shen	University of Central Florida, USA

Treasurer:

T. P. Chow	Renessalear Polytechnic Institute, USA

Conference Advisory Members:

M. Adler	IEEE, USA
G. Amaratunga	Cambridge University, UK
B. J. Baliga	N. Carolina State University, USA
T. Efland	Texas Instruments, USA
W. Fichtner	Swiss Federal Institute of Technology, Switzerland
L. Lorenz	Infineon Technologies, Germany
H. Ohashi	Tokyo Institute of Technology, Japan
T. Ohmi	Tohoku University, Japan
M. Okamura	Japan Advanced Institute of Science and Technology, Japan
A. Salama	University of Toronto, Canada
A. Shibib	Agere Systems, USA
Y. Sugawara	Kansai Electric Power, Japan
Y. Uchida	Fuji Electric, Japan
R. Williams	Advanced Analogic Technologies, USA
T. Yachi	Tokyo University of Science, Japan

TECHNICAL PROGRAM COMMITTEE MEMBERS

LOW VOLTAGE AND RF

G. Dolny (Chair)	Fairchild Semiconductor, USA
M. Darwish	MaxPower Semiconductor, USA
P. Hower	Texas Instruments, USA
S. Matsumoto	NTT, Japan
A. Nakagawa	Toshiba, Japan
A. Salama	University of Toronto, Canada
J. Shen	University of Central Florida, USA
Jan Sonsky	NXP Semiconductors, Belgium
A. Strachan	National Semiconductor, USA
A. Tamagawa	NEC Electron Devices, Japan
F. Udrea	Cambridge University, UK
T. Yachi	Tokyo University of Science, Japan

HIGH VOLTAGE

D. Kinzer (Chair)	Fairchild Semiconductor, USA

V. Benda	Czech Technical University, Czech Republic
M.K. Han	Seoul National University, Korea
R. Herzer	Semikron, Germany
T. Kimoto	Kyoto University, Japan
S. Linder	ABB, Switzerland
L. Lorenz	Infineon Technologies, Germany
M. Mori	Hitachi, Japan
D. Pattanayak	Vishay-Siliconix, USA
J.-L. Sanchez	LAAS-CNRS, France
P. Spirito	University of Naples, Italy
Y. Seki	Fuji Electric, Japan

INTEGRATED POWER

D. Disney (Chair)	Advanced Analogic Technologies, USA
S. Banerjee	Power Integrations, USA
C. Contiero	STMicroelectronics, Italy
S. Ekkanath Madathil	De Montfort University, UK
A. Huang	N. Carolina State University., USA
T. Letavic	Philips, USA
P. Moens	AMI Semiconductor
W.T. Ng	University of Toronto, Canada
S. Pendharkar	Texas Instruments, USA
A. Shibib	Fultec Semiconductor, USA
D. Silber	University of Bremen, Germany
J. Sin	Hong Kong University of Science & Technology, China
H. Tadano	Toyota, Japan
R. Zhu	Motorola, USA

WIDE-BANDGAP

H.R. Chang (Chair)	International Rectifier, USA
A. Agarwal	Cree, USA
T. P. Chow	Renessalear Polytechnic Institute, USA
M. Hoshi	Nissan, Japan
T. Kimoto	Kyoto University, Japan
P. Mawby	University of Wales Swansea, UK
J. Millan	CNM, Spain
D. Sheridan	SemiSouth, USA
Y. Sugawara	Kansai Electric Power, Japan
S. Yoshida	Furukawa, Japan

TECHNICAL PROGRAM

Monday May 19, 2008

8:30am-8:45am Opening Remarks and Announcements
ISPSD'06 Best Paper Award

8:45am-11:00am
Session 1 (P1) Plenary
Chairs: T. P. Chow Renessalear Polytechnic Institute, USA
J. Millan CNM, Spain

8:45am-9:30am

P1-1 **Environmental Trends and Opportunities for Computer Power Delivery:**

Edward Stanford, Intel, USA

The Green environmental movements will have
significant impact on the design of future power systems for
computer data centers and computer systems. This paper will
explore some of the trends in future computer systems and data
centers. The impact of new environmental regulations will be
studied in the context of improved power conversion devices.

9:30am-10:15am

P1-2 **A New AC Current Switch Called MERS with Low On-State Voltage IGBTs (1.54 V) for Renewable Energy and Power Saving Applications:**

Ryuichi Shimada[1], Jan A. Wiik[1], Takanori Isobe[1], Taku Takaku[2], Noriyuki Iwamuro[2], Yoshiyuki Uchida[3], Marta Molinas[4] and Tore M. Undeland[4], [1]Tokyo Institute of Technology; [2] Fuji Electric Device Technology Co., Ltd.;[3] Curamik Electronics KK; [4]Norwegian University of Science and Technology

Emergence of new power electronics configurations
have historically been one of the important drivers for improvement
of the IGBT technology. Development of new IGBTs is
said to be a trade-off between saturation voltage, short-circuit
capability and switching losses. With the common applications
requiring high switching frequency and short-circuit capability,
the saturation voltage performance has not been fully optimized.
This paper describes a new configuration called the Magnetic
Energy Recovery Switch (MERS). It is characterized by using
simple control and low switching frequency, where saturation
voltage is the main contributor to losses. The semiconductor
requirements of this configuration have led to the development of
a new low on-state voltage IGBT. Application in the area of wind
power conversion shows potential for efficiency improvements.
Additionally, due to the soft-switching nature of the MERS
application, series connection of the new IGBTs in variable
frequency induction heating application is shown to be easy
without voltage sharing problems.

10:15am-11:00am

***P1-3* From Packaging to "Un"-Packaging – Trends in Power Semiconductor Modules:**

Thomas Stockmeier, SEMIKRON Elektronik GmbH & Co KG, Germany

Power Semiconductor Modules play a key role in many Power Electronic Systems. Their inherent advantage of integrating different power chips, circuits, and sense, drive and protection functions into one sub-system with electrically insulated cooling has lead to a wide range of products, being different in size, power and function.

The power module market has grown to more 2,000 Mio USD and will continue to grow with a two digit rate. The strong growth rate in the traditional power module markets such as industrial drives, process automation, power supplies, traction, and consumer is surpassed by the growth rate in new markets, such as wind power, solar, and hybrid and electric vehicles.

The growing importance of power modules justifies to review today´s power module products and their packaging and interconnect technologies and to point out important trends towards next generations of power modules and power module technologies. Such trends are more intelligent power modules by advanced integration, replacement of the classical solder joints by diffusion sintering, new materials which exhibit properties tailored specifically to the use in power modules, and interconnect technology which will shift from solder and screw type contacts to pressure and spring type contacts.

In the growing market of hybrid and electrical vehicles, products are emerging where power modules are “un-packaged”, meaning that at least the same function as for an intelligent power module can be provided without all the classical metal, plastic, and ceramic contents and quantities. “Un-packaging” leads to functionally integrated, mechanically compact and low weight subsystems with very high power densities which are far better suited for harsh environmental conditions such as shock and vibration, high temperature, high humidity, and extended temperature and load cycling.

11:00am-1:30pm Lunch Break

1:30pm-3:10pm

Session 2 (LV1) Trench MOSFETS and Lateral IGBT

Chairs: **Gary Dolny,** *Fairchild Semiconductor*
Jan Sonsky, *NXP*

1:30pm-1:55pm

LV1-1 A 30V EDMOS with Orthogonal Gate Structure Based on a 0.18µm CMOS Technology :

[1]Hao Wang, [1]H.P. Edward Xu, [1]Wai Tung Ng, [2]Kenji Fukumoto,

[2]*Ken Abe*, [2]*Akira Ishikawa*, [2]*Hisaya Imai*, [2]*imio Sakai* and [2]*Kaoru Takasuka*, University of Toronto[1]; Asahi Kasei EMD[2]

1:55pm-2:20pm

LV1-2 60V Lateral Trench MOSFET in 0.35 µm Technology:

Don Disney, Wilson Chan, Roy Lam, Robert Blattner, Steve Ma, Wesley Seng, Jun-Wei Chen, Michael Cornell and Richard Williams, Advanced Analogic Technologies, Inc.

2:20pm-2:45pm

LV1-3 A Fully Realized 'Field Balanced' TrenchMOS Technology:

Steven T. Peake, Phil Rutter, Steve Hodgskiss, Mark Gajda and Neil Irwin, NXP Semiconductors

2:45pm-3:10pm

LV1-4 Retrograded Channel SOI LIGBTs with Enhanced Safe Operating Area:

David Hongfei Lu, Tomonori Mizushima, Akio Kitamura, Noriyuki Iwamuro and Naoto Fujishima, Fuji Electric Device Technology Co., Ltd.

3:10pm-3:30pm Coffee Break

3:30pm-5:10pm

Session 3 (HV1) Novel High Voltage Devices

Chairs: M.K. Han, *Seoul National University*
Reinhard Herzer, *Semikron International*

3:30pm-3:55pm

HV1-1 An IGCT Chip Set for 7.2 kV (RMS) VSI Application :

[1]*Iulian Nistor*, [1]*Maxi Scheinert*, [2]*Tobias Wikström* and [2]*Mathias Lüscher*, ABB Switzerland Ltd., Corporate Research[1];ABB Switzerland Ltd., Semiconductors[2]

3:55pm-4:20pm

HV1-2 Experimental Study of a 6.5kV MOS Controllable Freewheeling Diode :

J.G. Bauer, T. Duetemeyer, F. Hille and O. Humbel, Infineon Technologies AG

4:20pm-4:45pm

HV1-3 A Trial Simulation on the Cosmic Ray Induced Failure of the Long n¯ Length pin Diodes:

Ikunori Takata, Mitsubishi Electric Corp.

4:45pm-5:10pm

HV1-4 Experimental Demonstration of 3.3kV Planar CIGBT in NPT Technology :

[1]*M. Sweet,* [1]*N. Luther-King,* [1]*S.T. Kong, 1E.M. Sankara Narayanan,* [2]*J. Bruce and* [2]*Shona Ray,* University of Sheffield[1]; Semefab Scotland Ltd.[2]

6:00pm-8:00pm Welcome Reception

Tuesday May 20, 2008

8:30am-10:10am
Session 4 (IP1) Integration Technologies
Chairs: Peter Moens, *AMI Semiconductor*
Sameer Pendharkar, *Texas Instruments*

8:30am-8:55am

IP1-1 High-Voltage Technology Based on Thin Layer SOI for Driving Plasma Display Panels :

Ming Qiao, Bo Zhang, Zhiqiang Xiao, Jian Fang and Zhaoji Li, University of Electronic Science and Technology of China

8:55am-9:20am

IP2-2 HVCMOS8A: 22V-42V Rated MOS Integration in a 0.18µm Technology Platform for High Voltage Applications:

Stephane Bach,Laura Atzeni,Antonio Molfese, Alessandro Dundulachi, Elisabetta Castellana,Giuseppe Croce and Claudio Contiero, STMicroelectronics

9:20am-9:45am

IP2-3 55V Integrated Power and Non-Volatile Technology for Solid State Lighting Applications:

T. Letavic,R. Cook, S. Sharma, R. Brock, C. Mandhare, H. Effing, D. Dormans, B. Daniel, P. Deurenberg, C. Rooijackers and R. de Nie, NXP Semiconductors

9:45am-10:10am

IP2-4 BD180 – A New 0.18 µm BCD (Bipolar-CMOS-DMOS) Technology from 7V to 60V:

Il-Yong Park, Yong-Keon Choi, Kwang-Young Ko, Chul-Jin Yoon, Bon-Keun Jun, Mi-Young Kim, Hyon-Chol Lim, Nam-Joo Kim and Kwang-Dong Yoo, Dongbu HiTek

10:10am-10:30am Coffee Break

10:30am-12:10pm
Session 5 (HV2) IGBT & Diode
Chairs: Stefan Linder, *ABB*
Seki Yasukazu, *Fuji Electric*

10:30am-10:55am

HV2-1 A High Current 3300V Module Employing Reverse Conducting IGBTs Setting a New Benchmark in Output Power Capability :

M. Rahimo, U. Schlapbach, A. Kopta, J. Vobecky, D. Schneider and A. Baschnagel, ABB Switzerland Ltd., Semiconductors

10:55am-11:20am

HV2-2 CSTBT™ (III) as the Next Generation IGBT

Tetsuo Takahashi, Yoshifumi Tomomatsu and Katsumi Sato, *Mitsubishi Electric Corporation*

11:20am-11:45am

HV2-3 Exploring the Silicon Design Limits of Thin Wafer IGBT Technology: The Controlled Punch Through (CPT) IGBT

J, Vobecký, M. Rahimo, A. Kopta and S. Linder, ABB Switzerland Ltd., Semiconductors

11:45am-12:10pm

HV2-4 Development of the 1200V FZ-Diode with Soft Recovery Characteristics by the New Local Lifetime Control Technique

Y. Onozawa,; K. Takahashi,H. Nakano, M. Nemoto, M. Otsuki, O. Ikawa and T. Miyasaka, Fuji Electric Device Technology Co., Ltd.

12:10pm-1:00pm Lunch Reception

1:00pm-4:00pm

Session 6 (P1) Poster Papers

Chairs:

T. Letavic	Philips, USA
A. Strachan	National Semiconductor, USA

LV-P1 μ-Raman Validated Stress-Enhanced Mobility in XtreMOS Transistors:

[1]P. Moens, [1]J. Roig, [1]J. Meersman, [1]J. Baele, [1]B. Desoete,[1]M. Tack and [2]I. De Wolf, AMI Semiconductor[1];IMEC[2]

LV-P2 Scalable Spice Modeling of Integrated Power LDMOS Device Using a Cell-Based Building Block Approach:

Yong Qiang Li, Tracey Krakowski, Pascale Franci and, Linda Smith, National Semiconductor

LV-P3 A Novel Sub-20V Power MOSFET with Improved On-Resistance and Threshold Variation:

Jacky C.W. Ng, Johnny K.O. Sin and Lingpeng Guan Hong Kong University of Science and Technology

LV-P4 High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in a 0.25µm Standard CMOS Process :

Abraham Yoo, Marian Chang, Olivier Trescases and Wai Tung Ng, University of Toronto

LV-P5 Optimization of Body Diode Reverse Recovery Characteristics of Lateral Power MOSFETs for Synchronous Rectifier DC-DC Converters :

[1]Y. Xiong, [1]H. Jia, [1]W. Deschain, [1]S. Sun, [1]X. Cheng, [2]G. Dashney, [2]D. Okada and [1]Z.J. Shen, University of Central Florida[1]; Great Wall Semiconductor[2]

LV-P6 Implementation of 85V High Side LDMOS with n-layer in a 0.35um BCD Process:

Choul-Joo Ko, Sang-Yong Lee, Il-Yong Park, Cho-Eung Park, Bon-Keun Jun, Yong-Jun Lee, Chan-Hee Kang, Jae-O Lee, Nam-Joo Kim and Kwang-Dong Yoo, Dongbu HiTek

LV-P7 High Side n-channel and Bidirectional Trench Lateral Power MOSFETs on One Chip for DCDC Converter ICs:

Mutsumi Sawada, Masaharu Yamaji, Shinichiro Matsunaga, Masanobu Iwaya, Hidenori Takahashi, Tsuyoshi Yoshiki, Akihiro Jonishi, Akio Kitamura and Naoto Fujishima, Fuji Electric Device Technology Co., Ltd.

LV-P8 SJ-FINFET: A New Low Voltage Lateral Superjunction MOSFET:

[1]Y. Onishi, [2]H. Wang, [2]H.P.E. Xu,[2] W.T. Ng, [3]R. Wu and [3]J.K.O. Sin, Fuji Electric Device Technology Co., Ltd[1].; University of Toronto[2]; Hong Kong University of Science and Technology[3]

LV-P9 New Power MOSFET Employing Segmented Trench Body Contact for Improving the Avalanche Energy:

[1]In-Hwan Ji, [1]Kyu-Heon Cho, [1]Min-Koo Han, [2]Seung-Chul Lee, [2]Soo-Seong Kim, [2]Kwang-Hoon Oh and [2]Chong-Man Yun, Seoul National University[1]; Fairchild Semiconductor[2]

LV-P10 An 80V Class Silicon Lateral Trench Power MOSFET for High Frequency Switching Applications:

[1]*K.R. Varadarajan,* [1]*T.P. Chow,* [2]*R. Liu* ,[2]*F. Gonzalez and* [2]*B. Choy,* Rensselaer Polytechnic Institute[1]; Supertex[2]

LV-P11 3D-Resurf: The Integration of a p-Channel LDMOS in a Standard CMOS Process:

V. Vescoli, J.M. Park, S. Carniello and R. Minixhofer, austriamicrosystems AG

LV-P12 Evaluation of Trench-Gate Bipolar-Mode JFETs used as High-Side Transistors in Low-Voltage Buck Converters:

[1]*Yu Wu,* [1]*Bo Tian,* [1]*Huai Huang,* [1]*Dongqing Hu,* [2]*Johnny K.O. Sin and* [1]*Baowei Kang,* Beijing University of Technology[1] ; Hong Kong University of Science and Technology[2]

LV-P13 A Gate-Controllable High-Voltage SCR Device with High Performance in ESD Protection and Latch-Up Immunity:

Tuo-Hsin Chien and Klaus Y.-J. Hsu, National Tsing Hua University

HV-P1 Determination of Manufacturing Resurf Process Window for a Robust 700V Double Resurf LDMOS Transistor:

Zia Hossain, ON Semiconductor

HV-P2 Investigation of Dynamic Avalanche in the Termination Region for FWDs with High Reverse Recovery Capability:

[1]*Satoru Kameyama,* [2]*Takahide Sugiyama,* [1]*Ryuzo Tagami and* [1]*Katsuhiko Nishiwaki,* Toyota Motor Corporation[1]; Toyota Central R&D Labs Inc[2]

HV-P3 700V Lateral DMOS with New Source Fingertip Design:

S.H. Lee, C.K. Jeon, J.W. Moon and Y.C. Choi, Fairchild Korea Semiconductor

HV-P4 The Next Generation of HV-IGBTs with Low Loss and High SOA Capability:

[1]*Katsumi Nakamura,* [1]*Kenji Hatori,* [1]*Yoshiaki Hisamoto,* [1]*Tatsuo Harada,* [2]*Shunsuke Sakamoto,* [1]*Tatsuo Harada and* [1]*Kazunari Hatade,* Mitsubishi Electric Corporation[1]; Fukuryo Semicon Engineering Corporation[2]

HV-P5 A New Optimized 200V Low on-Resistance Power FLYMOSFET:

[1,2,3]*Y. Weber,* [1,2]*F. Morancho,* [3]*J.-M. Reynes,* [3]*E. Stefanov, CNRS;LAAS*[1]*, Université de Toulouse;UPS;LAAS*[2]*; Freescale Semiconducteurs France SAS*[3]

HV-P6 Analysis of a p+p-n-n+ Diode Structure :

[1]*Min Chen,* [1]*Josef Lutz,* [2]*Hans-Peter Felsl and* [2]*Hans-Joachim Schulze,* Chemnitz University of Technology[1]*;* Infineon Technologies AG[2]

HV-P7 JFET Depletion in SuperJunction Devices:

[1]*Don Disney and* [2]*Gary Dolny,* Advanced Analogic Technologies, Inc[1]*.;* Fairchild Semiconductor[2]

HV-P8 The Optimal Profile Design for SJ-MOSFET Fabricated by Double-Ion-Implantation and Multi-Epitaxial Method:

Syotaro Ono, Wataru Saito, Masaru Izumisawa, Yasuto Sumi, Shoichiro Kurushima, Masataka Tsuji, Ken'ichi Tokano and Masakazu Yamaguchi, Semiconductor Company, Toshiba Corporation

HV-P9 Super Junction MOSFETs Above 600V with Parallel Gate Structure Fabricated by Deep Trench Etching and Epitaxial Growth:

A. Sugi, M. Takei, K. Takahashi, A. Yajima, H. Tomizawa and H. Nakazawa, Fuji Electric Device Technology Co., Ltd.

HV-P10 Anode Design Variation in 1200-V Trench Field-Stop Reverse-Conducting IGBTs:

S. Voss, F.J. Niedernostheide and H.J. Schulze, Infineon Technologies AG

HV-P11 The CIBH Diode – Great Improvement for Ruggedness and Softness of High Voltage Diodes:

[1]*H.P. Felsl,* [1]*M. Pfaffenlehner,* [1]*H. Schulze,* [1]*J. Biermann,* [1]*Th. Gutt,* [1]*H.-J. Schulze,* [2]*M. Chen and* [2]*J. Lutz,* Infineon Technologies AG[1];Chemnitz University of Technology[2]

HV-P12 A Study of the Influence of Technology on the Negative Gate Capacitance in 1.2kV IGBTs:

S.T. Kong, L. Ngwendson, M. Sweet and E.M. Sankara Narayanan, University of Sheffield

HV-P13 Thermal and Structural Simulation Techniques for Estimating Fatigue Life of an IGBT Module:

[1]*Koji Sasaki,* [1]*Naoko Iwasa,* [2]*Toshiki Kurosu,* [2]*Katsuaki Saito,* [2]*Yoshihiko Koike,* [2]*Yukio Kamita and* [2]*Yasushi Toyoda,* Mechanical Engineering Research Laboratory, Hitachi, Ltd[1]; Power & Industrial Systems Division, Hitachi, Ltd.[2]

HV-P14 Critical IGBT Design Regarding EMI and Switching Losses:

Masanori Tsukuda, Ichiro Omura, Yoko Sakiyama, Masakazu Yamaguchi, Ken'ichi Matsushita and Tsuneo Ogura, Semiconductor Company, Toshiba Corporation

HV-P15 A Study on the Reliability of the Chip Surface Solder Joint :

[1]*Yoshinari Ikeda,* [1]*Yuji Iizuka,* [2]*Tatsuhiko Asai,* [1]*Tomoaki Goto,* [1]*Yoshikazu Takahashi, Fuji Electric Device Technology Co., Ltd*[1]*.; Fuji Electric Advanced Technology Co., Ltd*[2]

HV-P16 New Oscillation Circuit Discovered in Switching-Mode Power Supplies:

T. Fujihira,; T. Yamada, Y. Minoya, T. Kobayashi, Y. Niimura, T. Kuboyama, R. Araki and H. Ota, Fuji Electric Device Technology Co., Ltd.

IP-P1 Chipset for Flexible and Scalable High-Performance Gate Drivers for 1200V- 6500V IGBTs :

Jan Thalheim, CT-Concept Technologie AG

IP-P2 Self-Triggered SCR in Output Driver for Enhanced ESD Robustness :

[1]*TaegHyun Kang,* [1]*JunHyeong Ryu,* [1]*MoonHo Kim,* [2]*EuiYong Chung and* [1]*Donna Robinson-Hahn,* Fairchild Semiconductor[1]; Yonsei University[2]

IP-P3 Time Dependent Isolation Capability of High Voltage Deep Trench Isolation:

[1]*Ralf Lerner,* [1]*Uwe Eckoldt,* [1]*Klaus Schottmann,* [2]*Steffen Heinz,* [2]*Klaus Erler,* [2]*Andre Lange and* [2]*Gunter Ebest,* X-FAB Semiconductor Foundries AG[1]; Chemnitz University of Technology[2]

IP-P4 Measurement and Simulation of Self-Heating in DMOS Transistors up to Very High Temperatures:

Martin Pfost, Joachim Joos and Matthias Stecher, Infineon Technologies AG

IP-P5 Integrated Photoreceiver for an Isolated Control Signal Transfert in Favour of Power Transistors:

Nicolas Rouger and Jean-Christophe Crébier, University of Grenoble

IP-P6 Sense Device Structure in Hybrid IGBT with Constant Current Sense Ratio for Entire Collector Current Range:

H. Yamagiwa, T. Saji, S. Kaneko, S. Takahashi, T. Uno and K. Sawada, Matsushita Electric Industrial Co., Ltd.

IP-P7 ESD Protection of NDMOS in 0.18µm High-Voltage CMOS Technology for Automotive Applications:

[1]*L. Steinbeck,* [1]*U. Pröhl,* [2]*M. Frank,* [2]*A. Konrad,* [1]*C. Ellmers,*[1] *T. Uhlig, X-FAB Dresden GmbH & Co. KG*[1] *; X-FAB Semiconductor Foundries AG*[2]

WB-P1 High-Voltage AlGaN/GaN Schottky Barrier Diodes on Si Substrate with Low-Temperature GaN Cap Layer for Edge Termination:

[1]*A. Kamada,* [1]*K. Matsubayashi,* [1]*A. Nakagawa,* [2]*Y. Terada and* [2]*T. Egawa,* New Japan Radio Co., Ltd[1].; Nagoya Institute of Technology[2]

WB-P2 High Frequency Switching of SiC High Voltage LJFET:

Kuang Sheng, Yongxi Zhang, Ming Su, Liangchun Yu and Jian H. Zhao, Rutgers University

WB-P3 Integration of 1200V SiC BJT with SiC Diode:

[1]*Yan Gao,* [1]*Alex Q. Huang,* [2]*Anant K. Agarwal and* [2]*Qingchun Zhang,* North Carolina State University[1]; Cree Inc.[2]

WB-P4 The Effect of the Temperature on the Bipolar Degradation of 3.3 kV 4H-SiC PiN Diodes:

[1]*P. Brosselard,* [1]*A. Perez-Tómas,* [1]*N. Camara,* [2]*J. Hassan,* [1]*X. Jordà,* [1]*M. Vellvehi,* [1]*P. Godignon,* [1]*J. Millán and* [2]*J.P. Bergman,* CNM-CSIC[1]; Norstel AB[2]

WB-P5 High Breakdown Voltage AlGaN/GaN HEMTs by Employing Proton Implantation:

[1]*Kyu-Heon Cho,* [1]*In-Hwan Ji,* [1]*Young-Hwan Choi,* [1]*Jiyong Lim,* [1]*Young-Shil Kim,* [2]*Kye-Ryung Kim,* [1]*Min-Koo Han,* Seoul National University[1] ; Korea Atomic Energy Research Institute[2]

WB-P6 Surge Current Ruggedness of Silicon Carbide Schottky- and Merged-PiN-Schottky Diodes:

[1]*Birk Heinze,* [1]*Josef Lutz,* [2]*Matthias Neumeister,* [3]*Roland Rupp and* [3]*Matthias Holz,* Chemnitz University of Technology[1]; Siemens AG[2]; Infineon Technologies AG[3]

WB-P7 High Conductivity δ-Doped Single Crystal Diamond Schottky m-i-p+ Diodes:

[1]*S.J. Rashid,* [1]*F. Udrea,* [2]*D.J. Twitchen,* [2]*R. S. Balmer,* [1]*G.A.J. Amaratunga, University of Cambridge*[1]; *Element Six Ltd*[2].

WB-P8 State of the Art 10 kV NMOS Transistors:

Mrinal K. Das,; Robert Callanan, D. Craig Capell, Brett Hull, Fatima Husna, James Richmond, Michael O'loughlin, Michael J. Paisley, Adrian Powell and Qingchun Zhang, Cree, Inc.

4:15-9:00pm Arabian Night Dinner Show

Wednesday May 21, 2008

8:30am-10:10am

Session 7 (WB1) SiC Power Diodes, Switches & Packaging

Chairs: **Masakatsu Hoshi,** *Nissan Motor Co. Ltd.*
Jose Millan, *Centro Nacional de Microelectrónica*

8:30am-8:55am

WB1-1 Heavily Electron-Irradiated High Resistive 4H-SiC Pin Diode for Turn-On Snubber of 200kVA Class High Power SiCGT Inverter:

1Katsunori Asano, Yoshitaka Sugawara, Atsushi Tanaka, Yoichi Miyanagi, Koji Nakayama, Shuji Ogata, Shinichi Okada, Toru Izumi and Ryosuke Ishii, Kansai Electric Power Company, Inc.

8:55am-9:20am

WB1-2 Normally-Off SiC VJFETs for 800V and 1200V Power Switching Applications:

I. Sankin, D.C. Sheridan, W. Draper, V. Bondarenko, R. Kelley, M.S. Mazzola and J.B. Casady, SemiSouth Laboratories, Inc.

9:20am-9:45am

WB1-3 4H-Sic Double RESURF MOSFETs with a Record Performance by Increasing RESURF Dose:

Masato Noborio, Jun Suda and Tsunenobu Kimoto, Kyoto University

9:45am-10:10am

WB1-4 4.5 kV 1000 A Class SiC pn Diode Modules with Resin Mold Package and Ceramic Flat Package:

Y. Sugawara, S. Ogata, S. Okada, T. Izumi, Y. Miyanagi, K. Asano, K. Nakayama and A. Tanaka, Kansai Electric Power Co.

10:10am-10:30am Coffee Break

10:30am-12:10pm

Session 8 (LV2) – Integrated LDMOS

Chairs: **Vishnu Khemka,** *Freescale Semiconductor*
Akio Nakagawa, *Toshiba*

10:30am-10:55am

LV2-1 Innovative Lateral Field Plates by Gate Fingers on STI Regions in Deep Submicron CMOS:

[1]A. Heringa, [1]J. Šonský, [1]J. Perez-Gonzalez, [2]R.Y. Su and [3]P.Y. Chiang, NXP-TSMC Research Center[1]; National Tsing Hua University[2];

TSMC[3]

10:55am-11:20am

LV2-2 High Voltage P-Channel MOS Breakdown Voltage Instability During High Temperature Gate Stress Induced by Pre-Metal Nitride Layers:

G. Marchesi, J. Cambieri, A. Dundulachi, G. Pizzo, F. Pozzobon, M. Annese, A. Andrein and G. Croce, STMicroelectronics

11:20am-11:45am

LV2-3 Incremental FRESURF LDMOSFET Structure for Enhanced Voltage Blocking Capability on a 0.13µm, SOI Based Technology:

Tahir Khan, Vishnu Khemka and Ronghua Zhu, Freescale Semiconductor

11:45am-12:10pm

LV2-4 High Doped Drain Double-Resurf 100V P-Channel MOS on SOI 0.35 µm BCD Technology:

Vincenzo Palumbo, Mirko Venturato, Michele Gallo, Fiorella Pozzobon, Maria Paola Galbiat and Claudio Contiero, STMicroelectronics

12:10pm-2:00pm Lunch Break

2:00pm-3:15pm

Session 9 (WB2) GaN Power HEMT/MOS Devices

Chairs: Hsueh-Rong Chang, *International Rectifier*
Seikoh Yoshida, *Furukawa Electric*

2:00pm-2:25pm

WB2-1 High Power AlGaN/GaN HFET with a High Breakdown Voltage of Over 1.8 kV on 4 Inch Si Substrates and the Suppression of Current Collapse:

Nariaki Ikeda, Syuusuke Kaya, Jiang Li, Yoshihiro Sato, Sadahiro Kato and Seikoh Yoshida, Furukawa Electric Co., Ltd.

2:25pm-2:50pm

WB2-2 Lateral Implanted RESURF GaN MOSFETs with BV Up to 2.5kV:

[1]W. Huang, [1]T.P. Chow, [2]Y. Niiyama, [2]T. Nomura and [2]S. Yoshida, Rensselaer Polytechnic Institute[1]; Furukawa Electric Co., Ltd[2]

2:50pm-3:15pm

WB2-3 Enhancement-Mode GaN Hybrid MOS-HEMTs with Ron,sp of 20 mΩ-cm2 :

[1]W. Huang, [1]Z. Li, [1]T.P.Chow, [2]Y. Niiyama, [2]T. Nomura and [2]S. Yoshida, Rensselaer Polytechnic Institute[1]; Furukawa Electric Co., Ltd[2].

7:00-9:00pm Conference Banquet

Thursday May 22, 2008

8:30am-10:10am
Session 10 (HV3) Superjunction & Termination Technology
Chairs: Deva Pattanayak, *Vishay*
J.-L. Sanchez, *LAAS CNR*
8:30am-8:55am
HV3-1 600V-Class Super Junction MOSFET with High Aspect Ratio P/N Columns Structure:
[1]*Jun Sakakibara,* [1]*Yoshitaka Noda,* [1]*Takumi Shibata,* [2]*Shoji Nogami,* [2]*Tomonori Yamaoka and* [1]*Hitoshi Yamaguchi,* DENSO Corporation[1]; SUMCO Corporation[2]

8:55am-9:20am
HV3-2 Feasibility Study of a Junction Termination Using Deep Trench Isolation Technique for the Realization of DT-SJMOSFETs:
[1]H. Mahfoz-Kotb, [1,2]L. Théolier, [1]F Institute for Physics of Electrotechnology
cho, [1,2]*K. Isoird,* [1]*P. Dubreui and ,* [1]*T. Do Conto,* LAAS-CNRS[1]; Université de Toulouse[2]

9:20am-9:45am
HV3-3 Time-Periodic Avalanche Breakdown at the Edge Termination of Power Devices:
[1]*U. Knipper,* [1]*G. Wachutka,* [2]*F. Pfirsch,* [2]*T. Raker and* [2]*J. Niedermeyr,* Institute for Physics of Electrotechnology-Munich University of Technology[1];Infineon Technologies AG[2]

9:45am-10:10am
HV3-4 The 2nd Generation Divided RESURF Structure for High Voltage ICs :
Kazuhiro Shimizu and Tomohide Terashima, Mitsubishi Electric Corporation

10:10am-10:30am Coffee Break

10:30am-12:10pm

Session 11 (IP2) Power IC Applications
Chairs: **Sujit Banerjee,** *Power Integrations*
Wai Tung Ng, *University of Toronto*

10:30am-10:55am

IP2-1 System in Package with Mounted Capacitor for Reduced Parasitic Inductance in Voltage Regulators:

[1]*T. Hashimoto,* [1]*T. Kawashima,* [2]*T. Uno,* [2]*Y. Satou and* [2]*N. Matsuura,* Hitachi Ltd[1]; Renesas Technology Corp.[2]

10:55am-11:20am

IP2-2 1700V Fully Coreless Gate Driver with Rugged Signal Interface and Switching-Independent Power Supply :

Sascha Pawel and Jan Thalheim, CT-Concept Technology Ltd.

11:20am-11:45am

IP2-3 Three-Input Type Single-Chip Inverter IC Including a Function to Generate Six Signals and Dead Time

Kenji Sakurai, Daisuke Maeda and Hiroyuki Hasegawa, Hitachi Ltd.

11:45am-12:10pm

IP2-4 Thick Silicon Membrane Technology for Reliable and High Performance Operation of High Voltage LIGBTs in Power ICs

T. Trajkovic, F. Udrea, C. Lee, N. Udugampola, V. Pathirana, A. Mihaila and G.A.J. Amaratunga, Cambridge Semiconductor Ltd.

12:10pm-12:30pm
Closing Ceremonies
Chairs:

Charitat Award