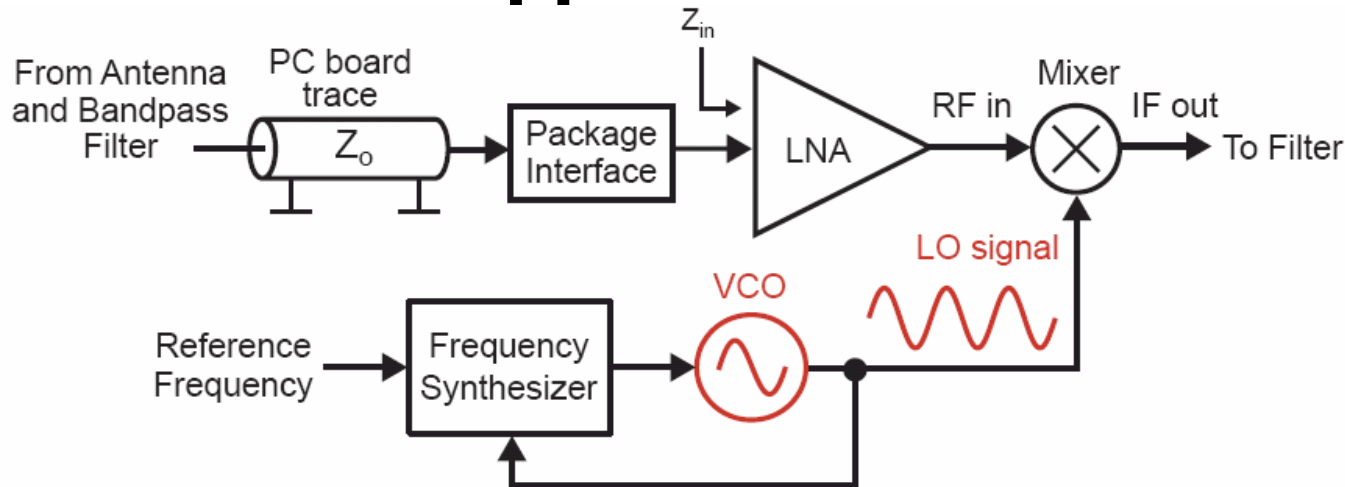


# Lecture 13: Voltage-Controlled Oscillator-Part III

## Tutorial (For more details, please refer to the LC-Oscillator tutorial on the class website)

# VCO Design Issues for Narrowband Applications



- **Tuning Range** –need to cover all frequency channels
- **Noise** –impacts receiver sensitivity performance
- **Power** –want low power dissipation
- **Isolation** –want to minimize noise pathways into VCO
- **Sensitivity to process/temp variations**

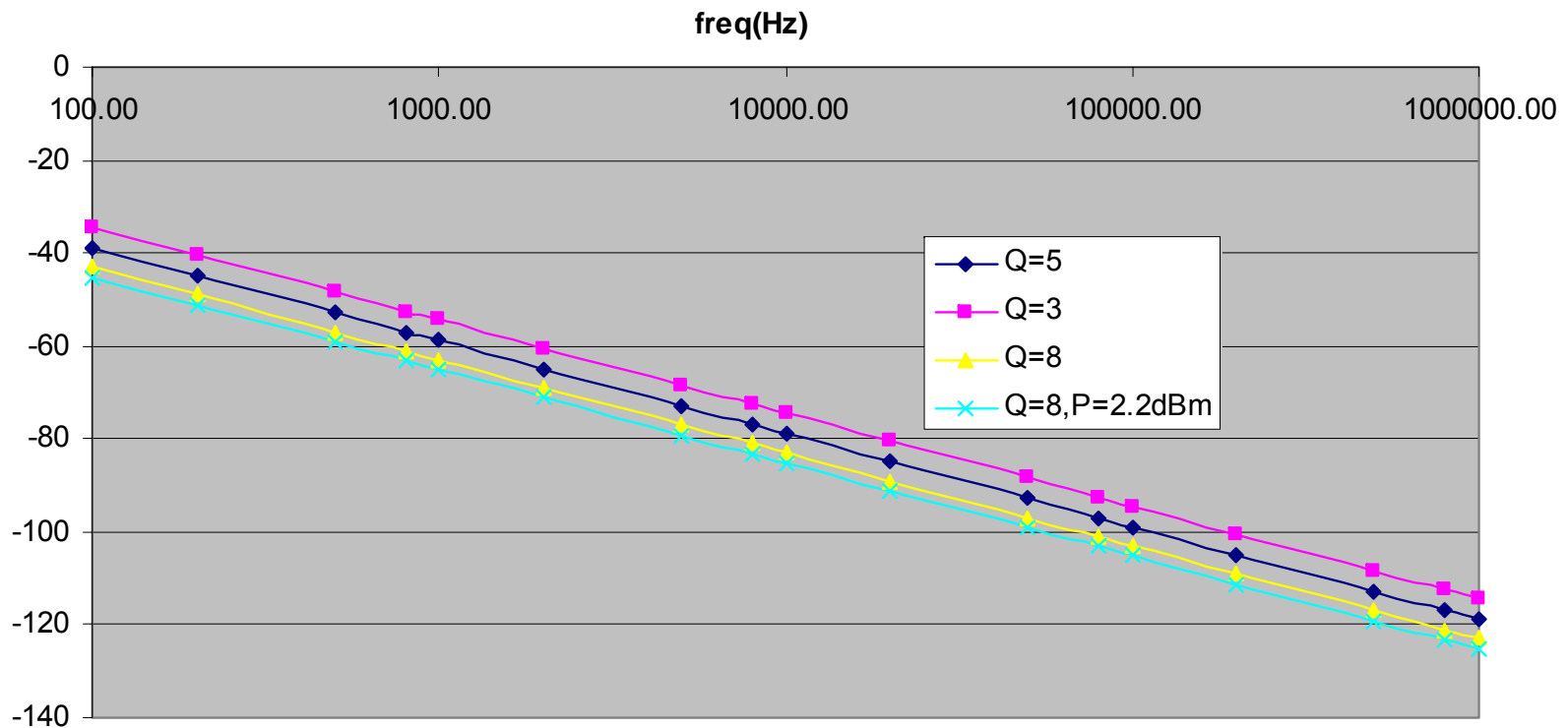
# Specifications

Parameter	Specification	Units
Center Frequency	2.4G	GHz
Tuning bandwidth	500	MHz
Ko	>100	MHz/V
Phase Noise	<-70 @ 10KHz	dBc/Hz
Supply	2.5	V
Power Consumption	<100	mW

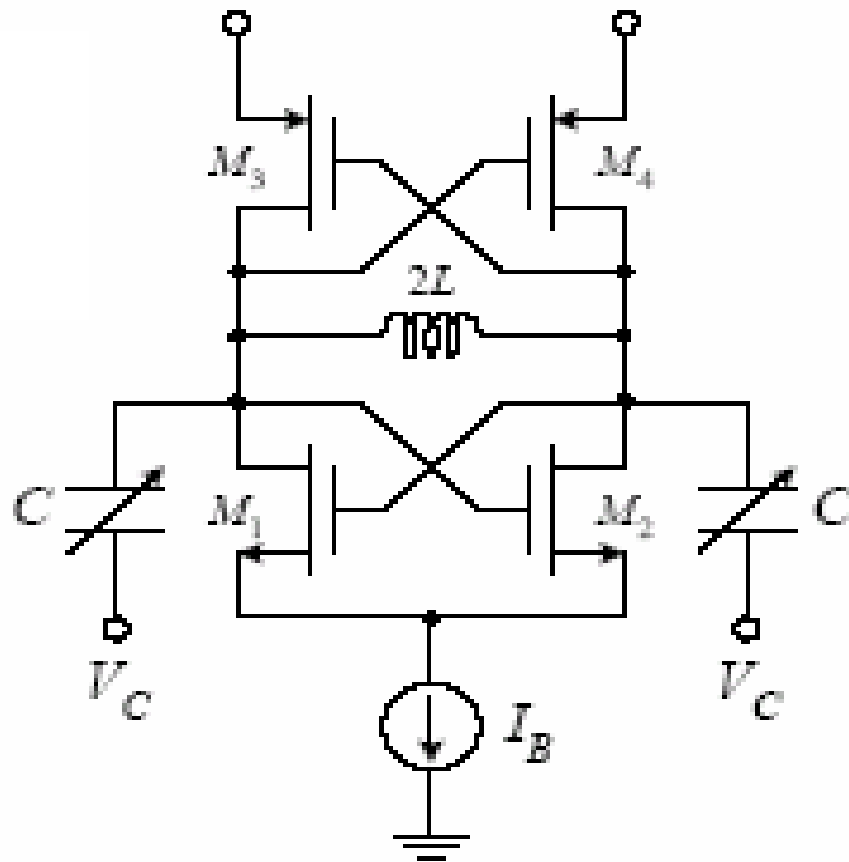
# Phase Noise as function of loaded quality factor

$$PN = \left( \frac{f_o}{2Q\Delta f} \right)^2 \frac{F.KT}{2P_{sig}} \left( 1 + \frac{f_c}{\Delta f} \right)$$

Assume  
Noise Figure (F)=10dB



## Architecture Choice



$$g_{m,active} = \frac{g_{m,n} + g_{m,p}}{2}$$

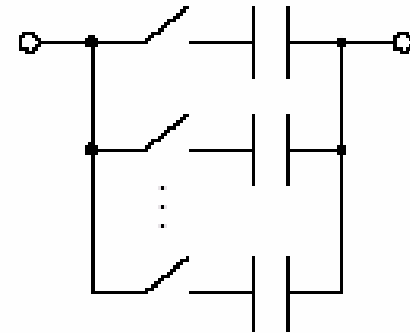
$$g_{m,active} \approx \alpha / R_P$$

$$\alpha \approx 2 - 3$$

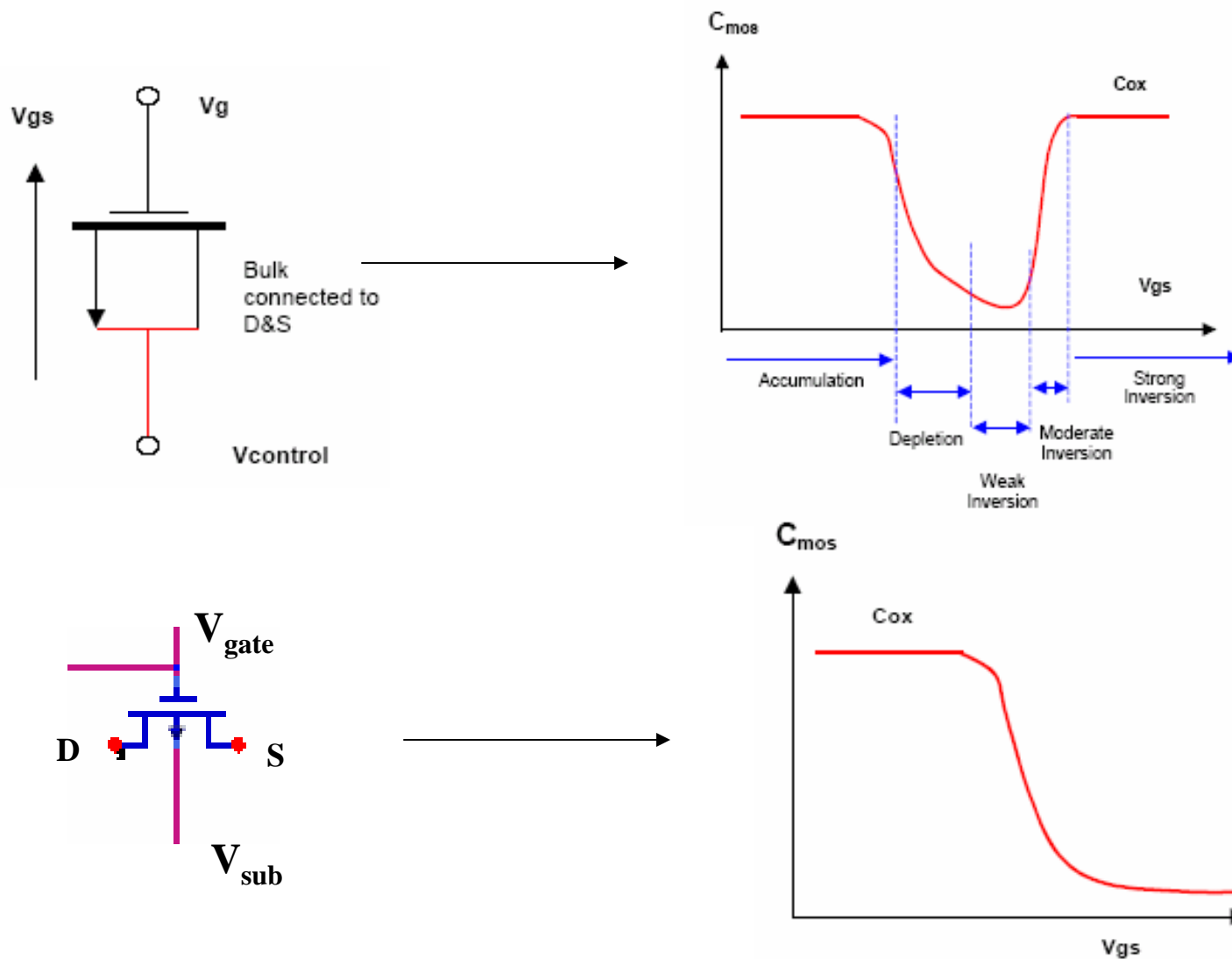
$$R_P = \text{Losses in the tank}$$

# Varactor in LC Oscillators

- Switched-capacitor array
  - High tuning range
  - Discrete capacitance
  - Q depends on switches
- PN diode
  - Good linearity
  - High Q value
- MOS Varactor
  - High tuning range
  - Q depends on process technology

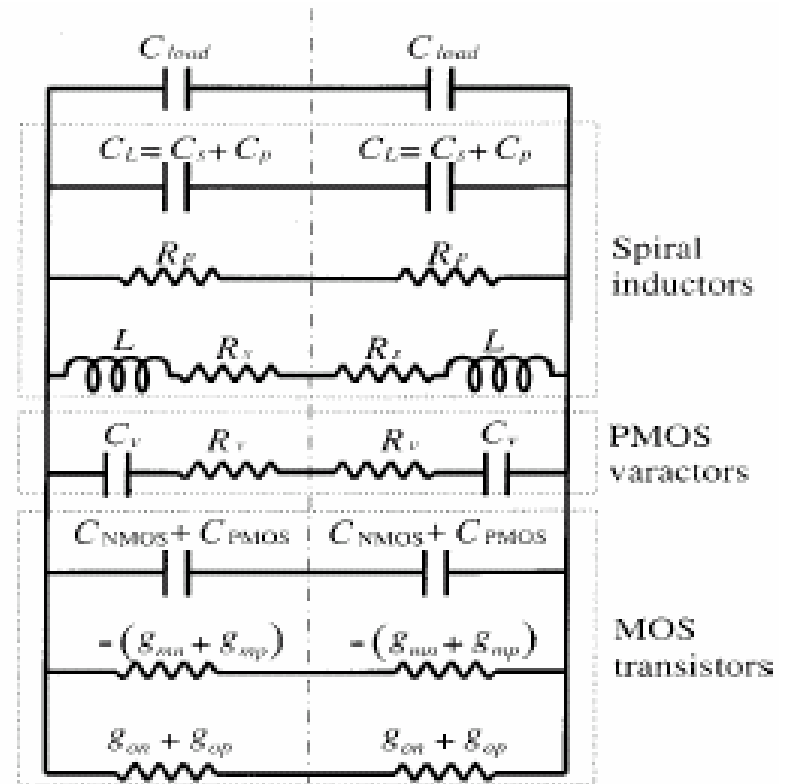
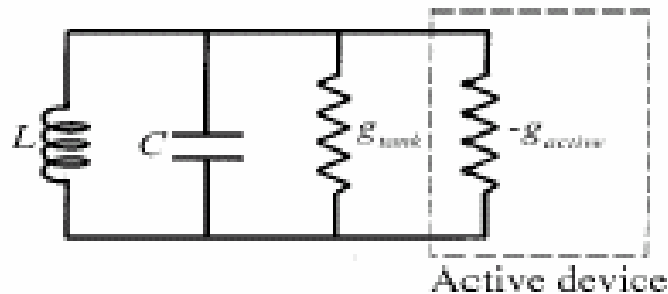


# Varactor Implementation



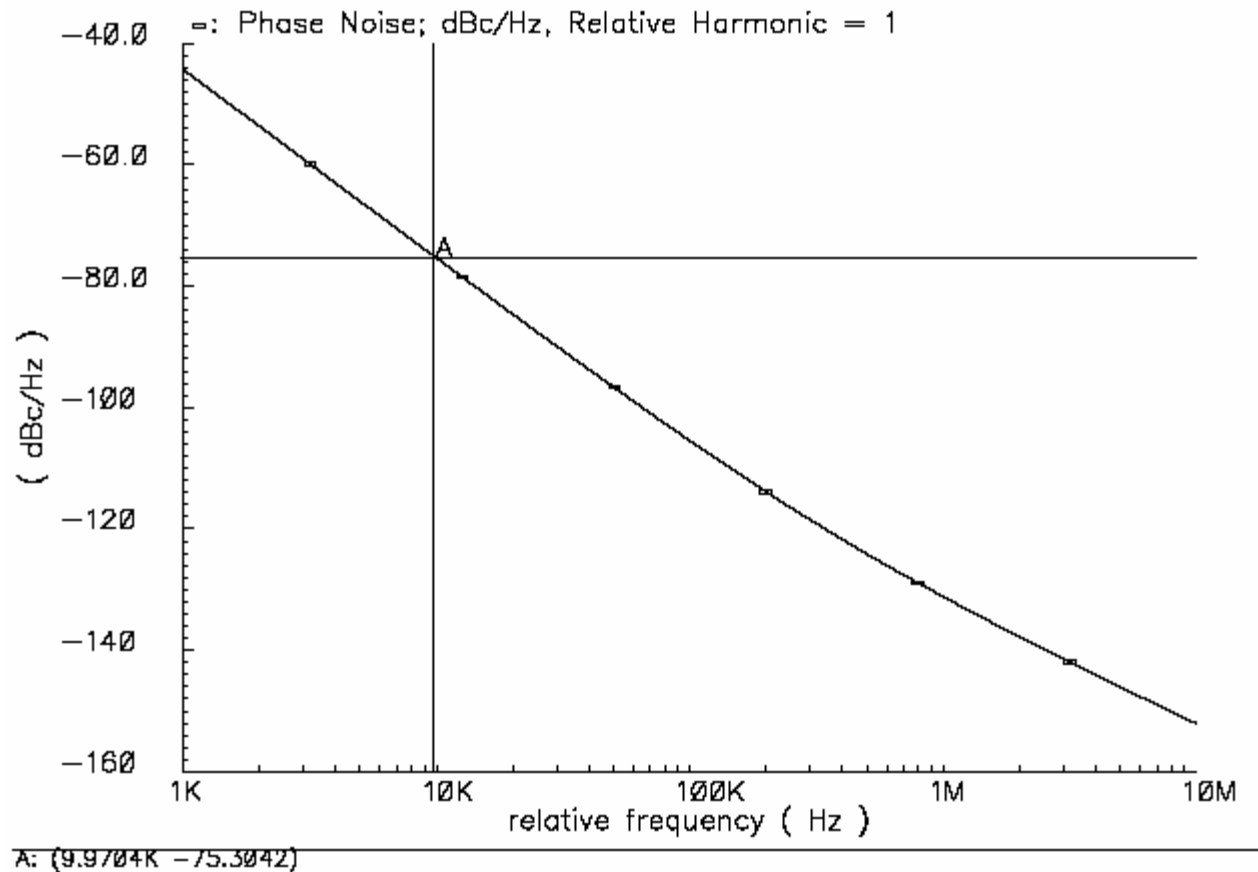


# Transistor Biasing and Sizing

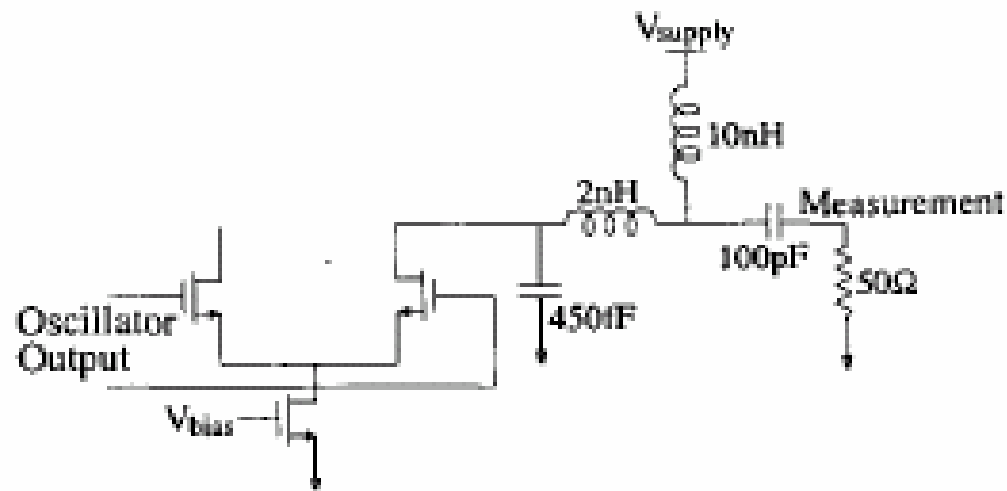


Equivalent Circuit Model for the VCO Core

# Phase Noise Simulation (Using PSS and PNOISE)

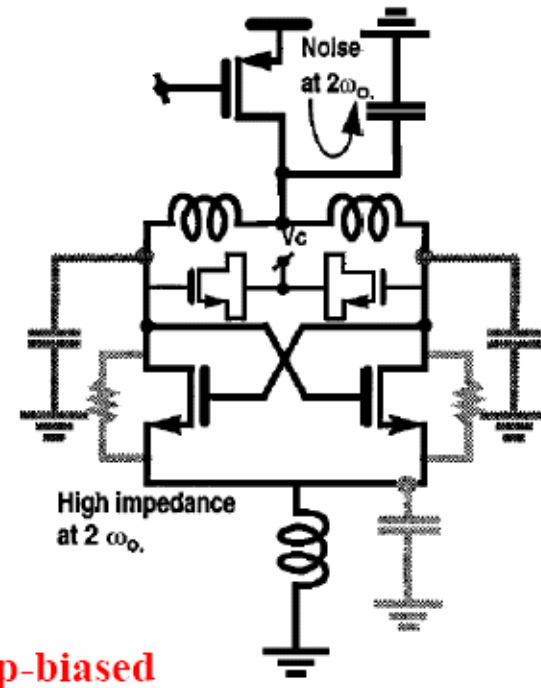
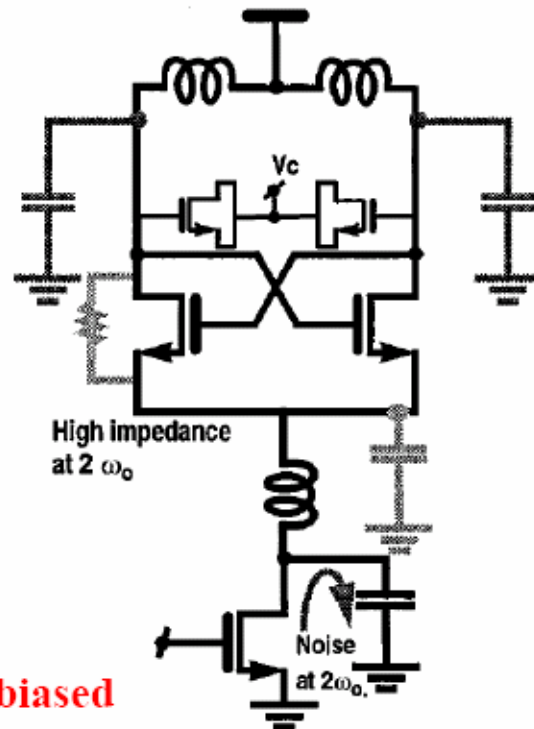


# An Example of connection to the 50-Ohm measurement equipment [2]



# 1.1 GHz VCO in *JSSC'01*

- 0.35  $\mu\text{m}$  CMOS technology; 2.5 V / 3.7 mA

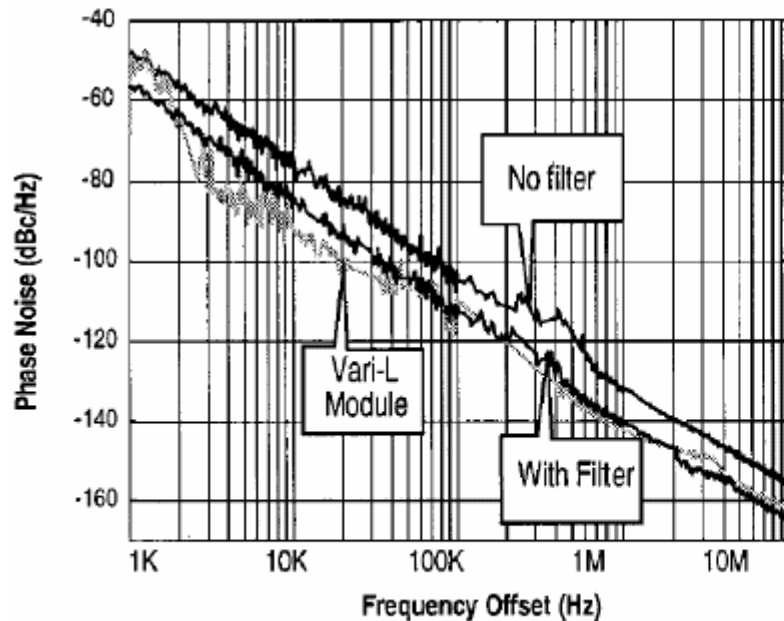


- E. Hegazi, H. Sjolund, and A. Abidi, "A filtering technique to lower oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921-1930, Dec. 2001.

# 1.1 GHz VCO in *JSSC'01*

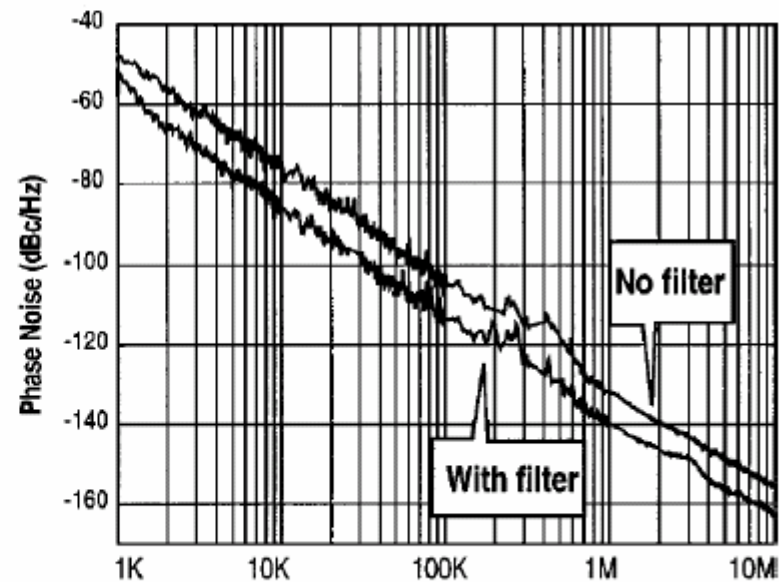
- **Tail-biased VCO**

- PN@3 MHz = -153 dBc/Hz



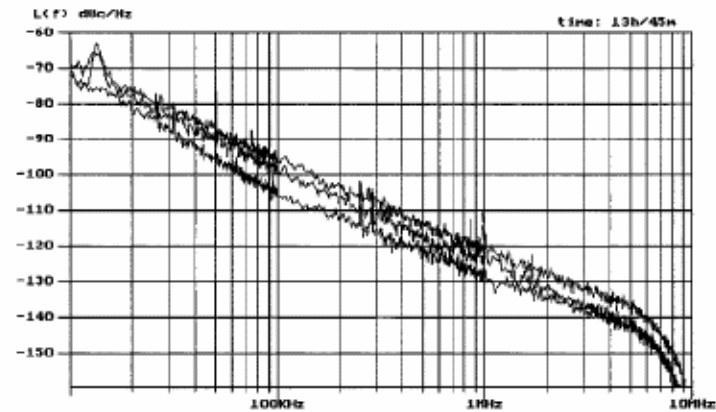
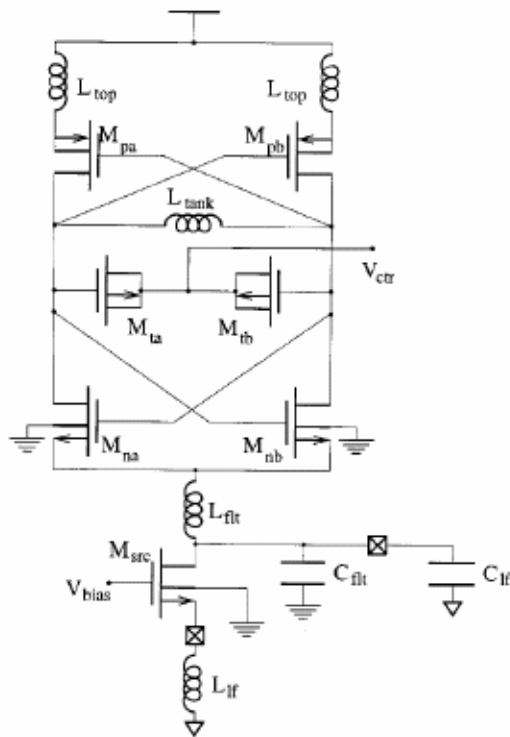
- **Top-biased VCO**

- PN@3 MHz = -152 dBc/Hz



# 1.96 GHz VCO in JSSC'02

- 0.35  $\mu\text{m}$  CMOS technology; 2 V / 6 mA



Offset frequency	$L_f = 0$ $C_f = 0$	$L_f = 0$ $C_f = 30 \text{ nF}$	$L_f = 100 \text{ uH}$ $C_f = 0$
100 kHz	-95.5	-98.0	-105.5
600 kHz	-116.0	-120.0	-123.5
3 MHz	-131.5	-136.5	-138.5

- P. Andreani and H. Sjolund, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, pp. 342-348, March 2002.

# References

1. D. Ham, and A. Hajimiri, “Concepts and Methods in Optimization of Integrated LC VCOs, *IEEE J. of Solid-State Circuits*, June 2001, pp. 896-909.
2. D. Ham and A. Hajimiri, “Design and Optimization of a Low Noise 2.4GHz CMOS VCO with Integrated LC tank and Moscap tuning,” *IEEE Int. Sump. Circuits and Systems*, Vol. 1, Geneva, Switzerland, May 2000, pp. 331-334