Smart Power MOS-Gated GaN Devices and ICs

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Goal

- Study, optimize and integrate various GaN MOS-gated devices for smart power devices and ICs

Why GaN ?

- Silicon power devices cannot operate properly when the temperature exceeds 200 °C
- GaN is suitable for high temperature, high voltage power applications due to its wide band gap and large critical electric field
- GaN power devices can be integrated with optoelectronics, microwave and control components and can be grown on silicon and sapphire substrates

Research Approach and Impact

Approach

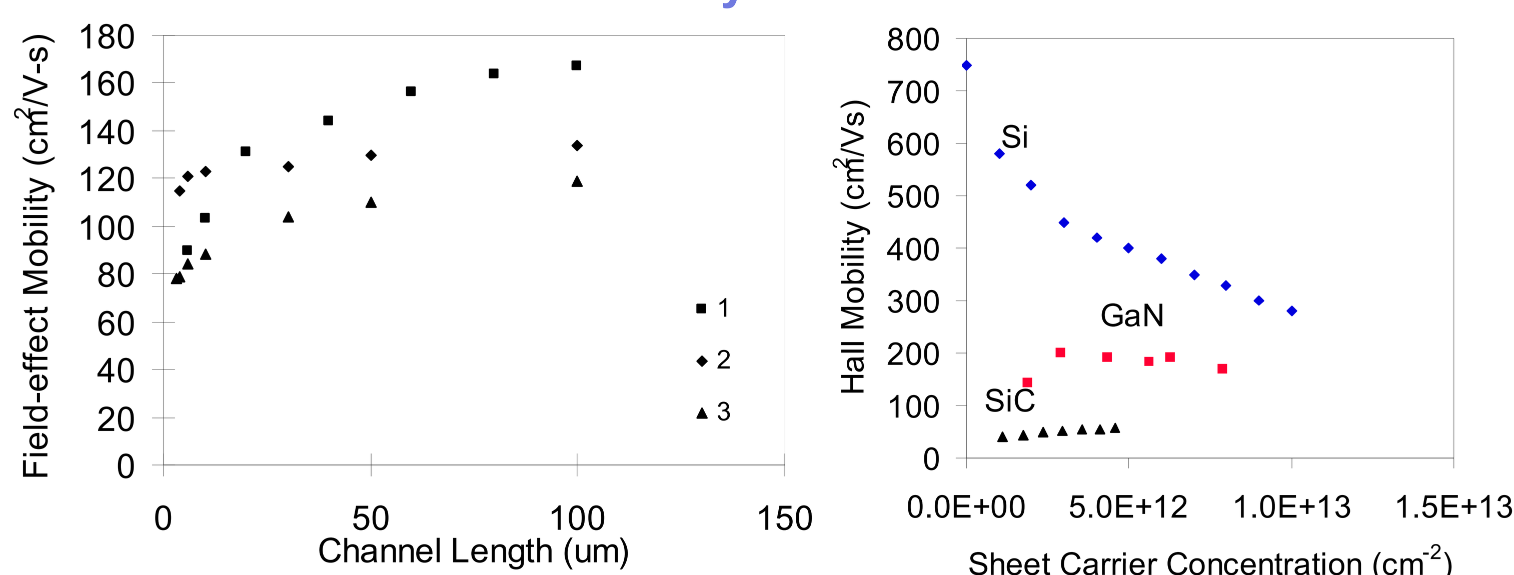
- Optimize experimentally GaN MOS process and incorporate it into integrated MOSFET process flow
- Demonstrate GaN lateral implanted/epilayer RESURF MOSFETs and lateral GaN hybrid MOS-HEMTs
- Project and evaluate the performance of high-voltage GaN MOSFETs with design and numerical simulations

Impact

- Make possible cost-effective, high-performance, smart power MOS-Gated GaN devices and ICs for demanding defense applications

Key Accomplishments

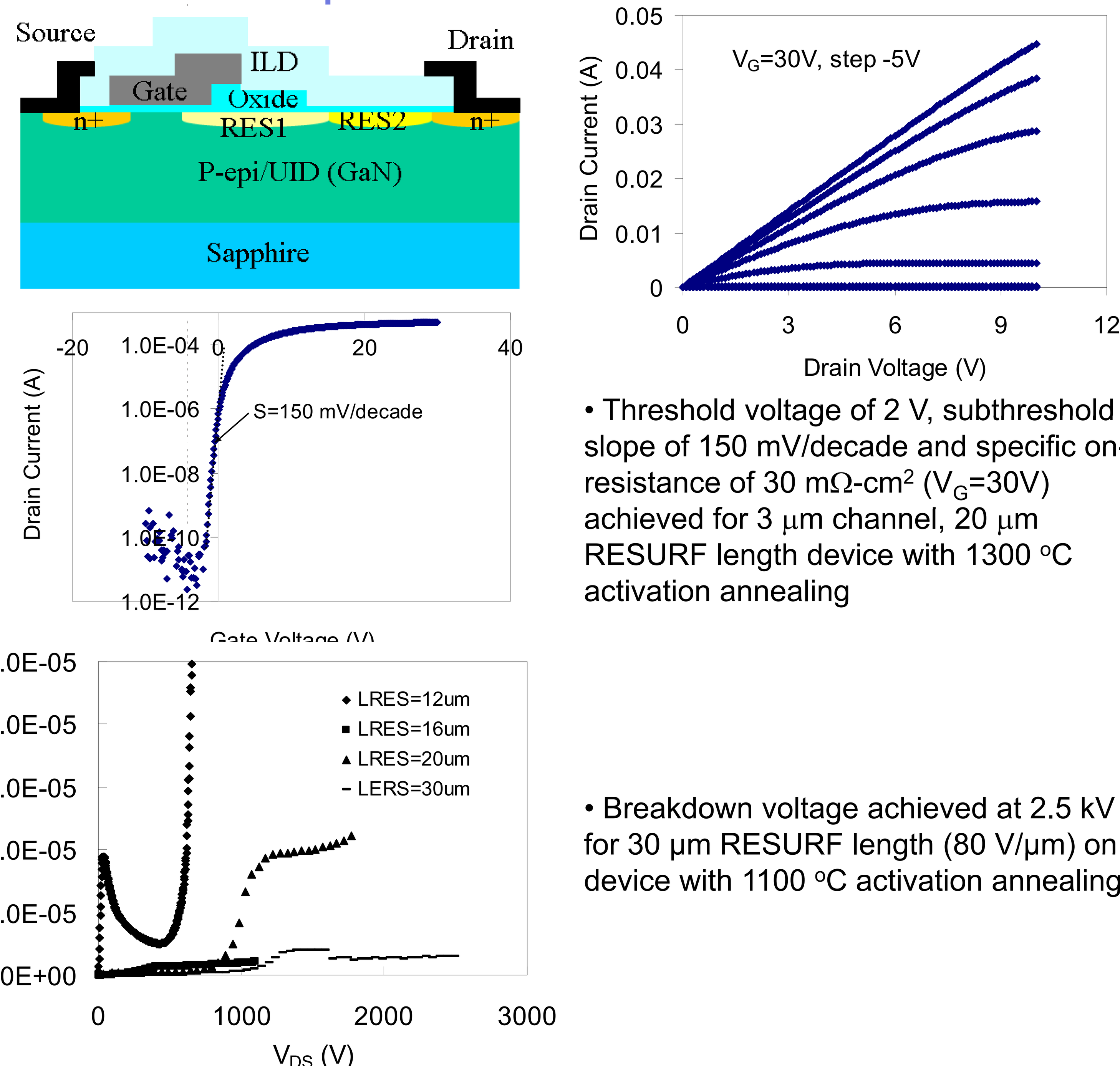
Field-effect Mobility and Hall Measurements



- Maximum field-effect mobility:
  "1" as-grown: 167 cm²/V-s
  "2" after1300 °C anneal: 132 cm²/V-s
  "3" Dry/wet-etched: 119 cm²/V-s

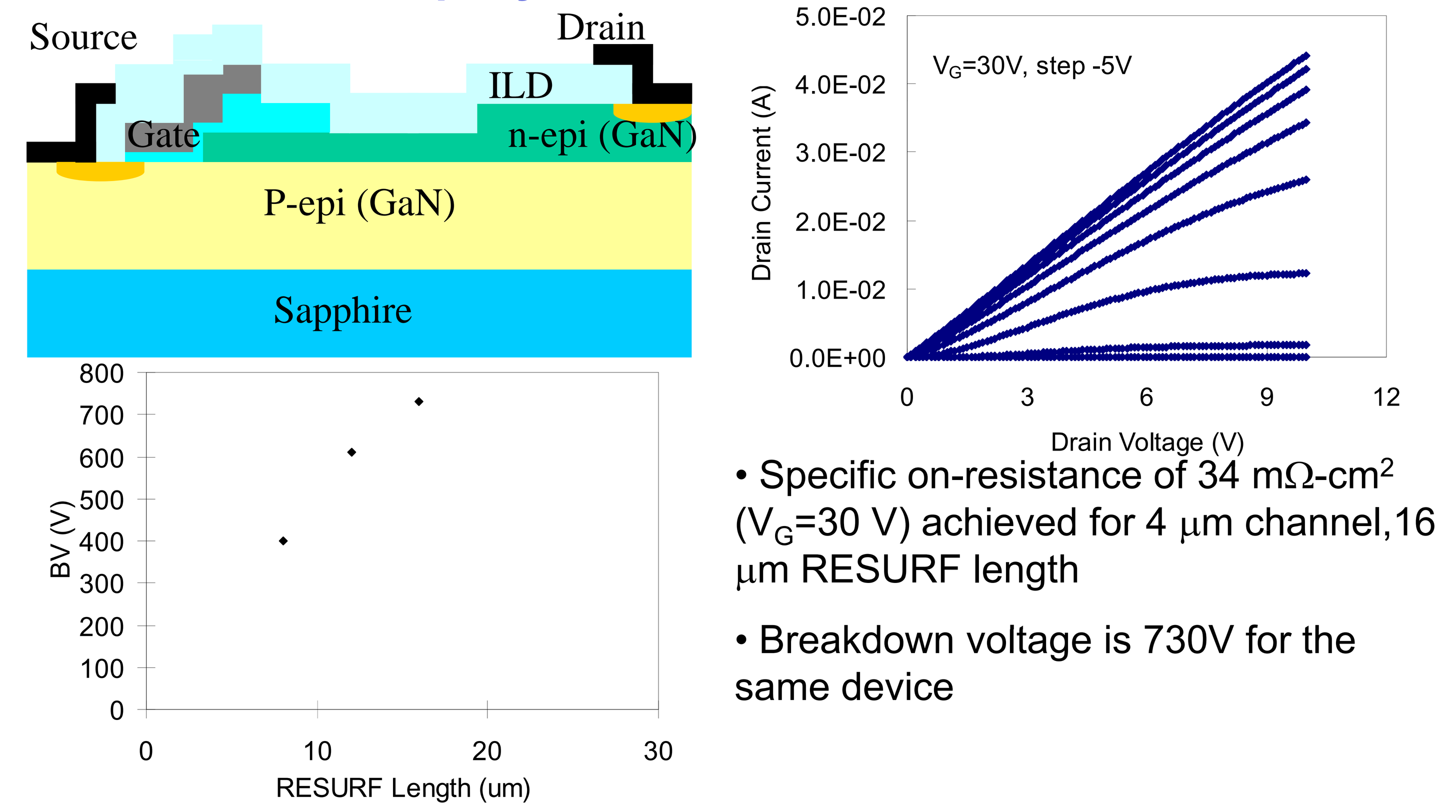
- Maximum field-effect mobility is 20% of bulk Hall mobility (900 cm²/V-s)
- Both high temperature anneal and dry/wet etch degrade field-effect mobility

Lateral Implanted RESURF GaN MOSFETs



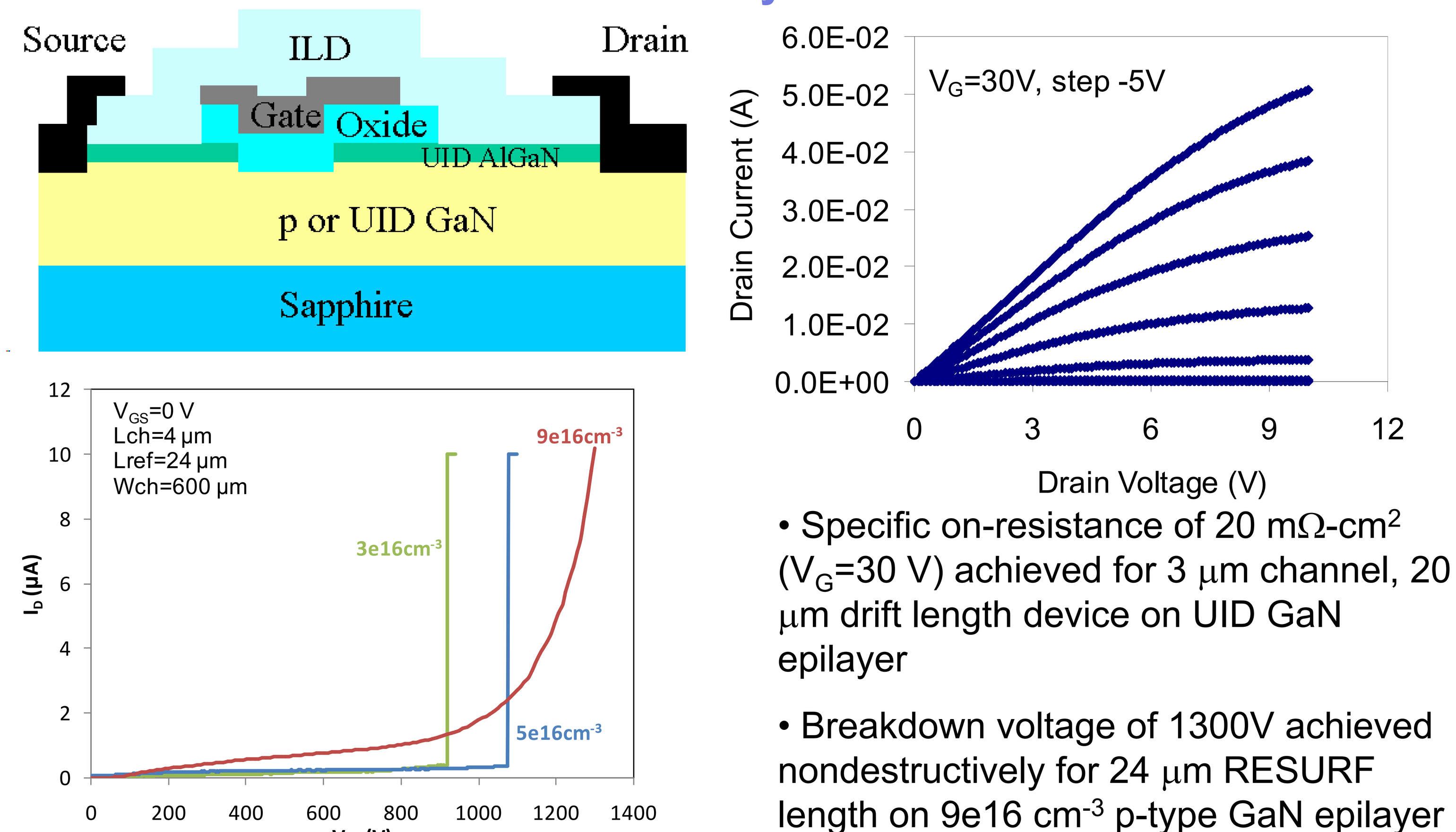
- Threshold voltage of 2 V, subthreshold slope of 150 mV/decade and specific on-resistance of 30 mΩ-cm² (V_G=30V) achieved for 3 μm channel, 20 μm RESURF length device with 1300 °C activation annealing
- Breakdown voltage achieved at 2.5 kV for 30 μm RESURF length (80 V/μm) on device with 1100 °C activation annealing

Lateral Epilayer RESURF GaN MOSFETs



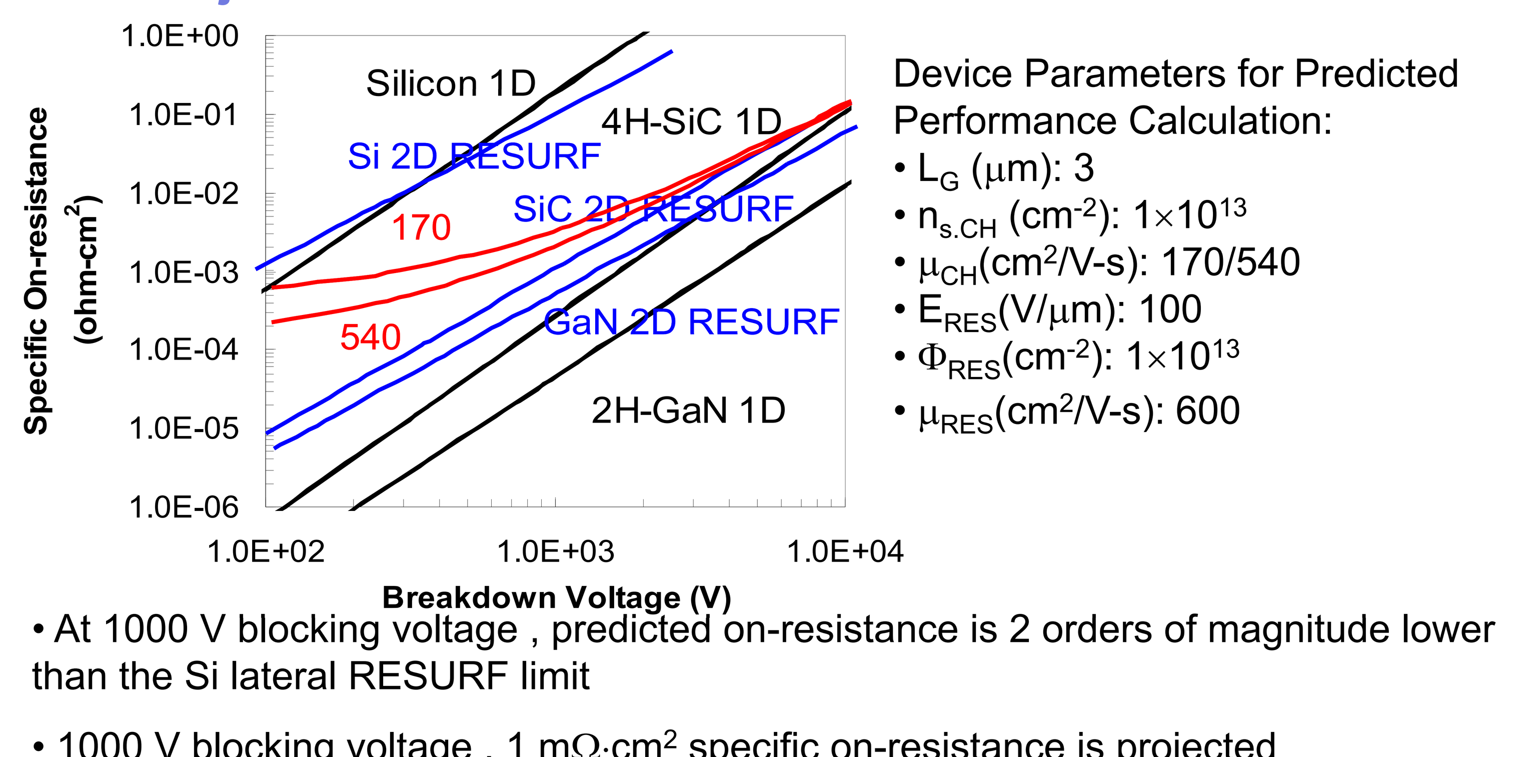
- Specific on-resistance of 34 mΩ-cm² (V_G=30 V) achieved for 4 μm channel,16 μm RESURF length
- Breakdown voltage is 730V for the same device

Lateral RESURF GaN Hybrid MOS-HEMTs



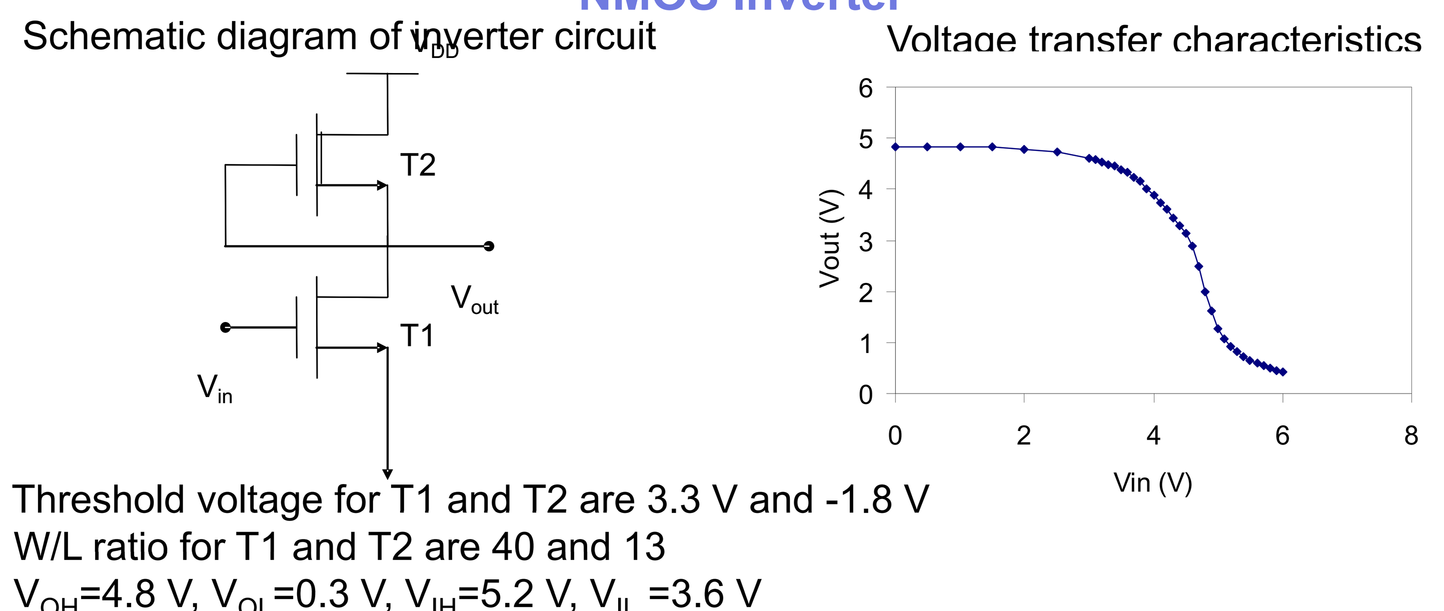
- Specific on-resistance of 20 mΩ-cm² (V_G=30 V) achieved for 3 μm channel, 20 μm drift length device on UID GaN epilayer
- Breakdown voltage of 1300V achieved nondestructively for 24 μm RESURF length on 9e16 cm⁻³ p-type GaN epilayer

Projected Performance of GaN lateral RESURF MOSFET



- At 1000 V blocking voltage , predicted on-resistance is 2 orders of magnitude lower than the Si lateral RESURF limit
- 1000 V blocking voltage , 1 mΩ·cm² specific on-resistance is projected

NMOS Inverter



- Threshold voltage for T1 and T2 are 3.3 V and -1.8 V
- W/L ratio for T1 and T2 are 40 and 13
- V_{OH}=4.8 V, V_{OL}=0.3 V, V_{IH}=5.2 V, V_{IL} =3.6 V

Future Directions

- Continue refining basic GaN MOS process to ensure high quality, reliable gate dielectric
- Fully activate moderately doped n-type GaN for RESURF region
- Integrate RESURF GaN MOS FETs with lateral JBS rectifier to form a MOS-gated bi-directional switch in GaN
- Scale up GaN device current rating, evaluate impact of high temperature packaging on device performance

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