ECSE 2610 Mid-Term Exam, Spring, 2002

Duration 7 - 9 pm

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<th>Student Name</th>
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Exam Rules:

- This is a 2 hours exam.
- This is an Open Book and Notes exam.
- You are not allowed to consult with other students.
- You may not use a calculator, laptop, palmtop, PDA, or such computer.
- If you need more space, continue on the back sides of pages, but make sure to indicate the continuation.

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<td>10 points</td>
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1. Given a 7-bit binary number 1111001, determine (10 points)
   - its decimal value if it represents an unsigned number
   - its decimal value if it represents a two’s complement number
   - its HEX representation
   - its BCD representation as an unsigned number
   - the ASCII character if it represents a character
2. Sketch gate-level schematic for the following VHDL program. Label input and output appropriately (10 Pts).

LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY xgate IS
  PORT(X: IN STD_LOGIC_VECTOR (1 downto 0):
       F: OUT BIT
  );
END xgate;
ARCHITECTURE Behavior OF xgate IS
BEGIN
  with X select F <=
    0 when "00"
    0 when "11"
    1 when "01"
    1 when "10"
END Behavior
3. Given the following function (10 points)

\[ F = (A + B + C + D')(A + C + D)(A' + B + C)(C' + D) \]

(a) Express the function in the canonical sum of products form (5 points).

(b) Re-express the function in minimized product of sum form (5 points).
4. Given A=FE and B=7E, both represented as two’s complement, compute A-B and B-A and indicate if overflow occurs for each case. Justify your answer (10 points).
5. Simplify the following expressions, using Boolean algebra (15 points).

- \( AC' + AB' + (AC)' + A'B'C \) (7 points)

- \(((ABC')' (BC)'(A'C)'(A'B'))'\) (8 points)
6. Consider the following functions (10 points)

- $F_1 = X(Y + Z) + X'Y'Z$
- $F_2 = X + Y' + Z'$

Implement these two functions using a single $74 \times 138$, one NAND gate.
7. Consider a 2-bit binary subtracter defined as follows. The inputs A, B and C, D form the two 2-bit numbers \( N_1 \) and \( N_2 \). The circuit will compute the difference \( N_1 - N_2 \) on the output bits \( F \) (most significant) and \( G \) (least significant). Assume the circuit never sees an input combination in which \( N_1 \) is less than \( N_2 \). The output bits are don’t care in these cases (20 points).

(a) Fill in the 4-variable truth table for \( F \) and \( G \).

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<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>F</th>
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(b) Derive the minimum SOP for \( F \) and \( G \) using K-map.

(c) Implement the sum of products expression from (b) using two 8:1 mux for both \( F \) and \( G \). Draw the schematics and clearly label the inputs and outputs of each pin of the mux.

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8. The following logic circuit consists of a 2-4 decoder and a 4-1 multiplexer. Its inputs are X, Y, S0, and S1 (where X is MSB and and S0 is LSB), and its output is F (15 points).

- Derive the truth table of the logic diagram.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>S1</th>
<th>S0</th>
<th>F</th>
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- Find the minimal sum of products expression for the diagram using K-map.

- [Diagram of K-map]