1. Mark each of the following statements as TRUE or FALSE (10 points)

- An NAND gate is the same as an OR gate with its two inputs complemented.
- Any canonical sum can be implemented using NAND gates only.
- \( F(A, B, C) = \Sigma m(1, 2, 3) \) represents the same expression as \( F(C, B, A) = \Sigma m(2, 4, 6) \).
- In a signed n-bit binary number represented using two's complement, there are more negative numbers than positive numbers.
- While performing binary addition, overflow occurs when there is a carry out for the most significant bit.
- In two's complement system, 1111010 and 1010 represent the same decimal number.
- FF is like a latch except that FF's output changes only at a clock event (rising or falling edge).
- For a Mealy machine, the output is a function of both input and current state, but input affects output only during a clock event.
- Bcc (branch on condition) and BSR can both be used to transfer to a subroutine except that BSR saves the returning address automatically.
- When servicing an interrupt, the CPU can be interrupted by another interrupt only if the new interrupt has higher priority than the one being serviced.
2. **Do the followings** (15 points)
   - Give the 8-bit two’s complement representations of the following decimal numbers (4 points).

   121

   -38

   - Perform the following additions (note the subscript represents the base and $2^r$ stands for two’s complement) (3 points).

   $10110101_2 \ + \ 1111_2$

   $11110101_2 \ + \ 1111_2$

   $F35_{16} \ + \ 27E_{16}$
• Using theorems of Boolean algebra to simplify the following function (3 points)

\[ f(A, B, C) = (A'B'C')(BC')(A'C')(A'B)' \]

• List three metrics that measure the complexity and performance of a digital circuit. What does each metric measure and how they can improve the circuit complexity and performance (5 points).
3. Consider a 2-bit binary subtracter defined as follows. The inputs A, B and C, D form the two 2-bit numbers \( N_1 \) and \( N_2 \). The circuit will compute the difference \( N_1 - N_2 \) on the output bits F (most significant) and G (least significant). Assume the circuit never sees an input combination in which \( N_1 \) is less than \( N_2 \). The output bits are don't care in these cases (15 points)

(a) Fill in the 4-variable truth table for F and G
(b) Derive the minimum SOP and POS for F and G using K-map
(c) Does static hazard-1 exist for the minimum SOP? If yes, how to avoid.
(d) Implement the static-hazard 1 free sum of products expression from (c) using a 4:1 mux. Draw the schematics and clearly label the inputs and outputs of each pin of the mux.
4. In this problem, you will design a combinational circuit that takes an 8 bit number \( A \) and calculates \( Y = A - 1 \). For example, if the input \( A=00001100_2 \), then \( Y = 00001011_2 \). The circuit is built from 1 bit modules connected in cascade. The 1 bit module is as follows

\[
\begin{array}{c}
A_n \\
\text{Borrow In}
\end{array} \quad \begin{array}{c}
\text{A}_n \quad \text{Y}_n \\
\text{Bl} \quad \text{BO}
\end{array} \quad \begin{array}{c}
\text{Borrow out}
\end{array}
\]

where \( A_n \) and \( Y_n \) represent the \( n \)th bit of \( A \) and \( Y \) respectively (10 points).

- Complete the truth table for the 1-bit module (5 points, Hint: \( Y_n = A_n - 0 \))

- Give the logical expressions for \( Y_n \) and Borrow Out (5 points)

- Show how the 1-bit modules would be interconnected to create an 8-bit subtract 1 circuit (2 points).
5. Do the following (10 points)

- Given the input and clock transition waveform below, draw a waveform for the output of a J-K device, assuming
  (a) it is a positive J-K FF
  (b) it is a negative J-K FF
  (c) it is a latch

assuming setup time, hold time, and propagation times are all 0 (5 points).

![Waveform Diagram]
• Given the following timing chart for a negatively edge-triggered sequential network, where $X_1$ and $X_2$ are inputs, $Q_1$ and $Q_2$ are state variables, and $Z_1$ and $Z_2$ represent two outputs, construct as much of the state diagram as possible. Is this a Moore or Mealy machine (5 points)?
6. Derive the excitation equation, state transition equation, state/output transition table, and the state diagram for the schematic implementation of the finite state machine in the Figure below. The next state and output functions are implemented by a PLA structure. The machine has one input I and one output Z (10 points).
7. A FSM has one input X and one output Z. The output Z is asserted whenever the input sequence ends in 1001. Draw the state diagram for the FSM as both a Mealy machine and then as a Moore machine. Identify the states involved and indicate what they represent (10 points).