

ABET COURSE SYLLABUS

ECSE-4962 VLSI Architectures for Signal Processing and Communications

Course Catalog Description: This course will introduce approaches and methodologies for VLSI design of signal processing and communication systems, and provide VLSI system design experience using hardware description language (HDL) and commercial EDA tools (SYNOPTSYS). One key issue will be the choice of the architecture for various signal processing and communication applications and the impact on performance, area and energy efficiencies. Basic building blocks in wireless communication system will be used as real-life case studies. Course projects will span the design hierarchy from signal processing and communication algorithm design to application-specific integrated circuit (ASIC) design, where MATLAB and SYNOPTSYS tools will be used. Prerequisites: ECSE-2610 CC&O and ECSE-2410 Signals and Systems (Preferred but NOT required: ECSE-4220 VLSI Design and ECSE-4510 Discrete Time System). *3 credit hours*

Pre-Requisite Courses: ECSE 2610 Computer Components and Operations and ECSE 2410 Signals and Systems

Co-Requisite Courses:

- Prerequisites by Topic:**
1. Basics of digital CMOS logic circuit design
 2. Linear discrete time system theory
 3. Finite impulse filter
 4. Infinite impulse filter
 5. Linear algebra

Textbook: Keshab K. Parhi “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley & Sons, 1999
(and/or other required material)

References:

Course Coordinator: Tong Zhang, Assistant Professor, Electrical, Computer and Systems Engineering

Overall Educational Objective: To introduce the basic methodologies and techniques in VLSI architectures for digital signal processing and communication systems

- Course Objectives:**
1. To introduce the basic approaches and methodologies for VLSI design of signal processing and communication systems;
 2. To provide hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys);
 3. To present real-life case studies of communication system integrated circuit (IC) design and implementations.

- How Course Objectives are Assessed:**
- Homework: 25%
 - Project proposal & presentation: 5%
 - Project report & presentation: 35%
 - Midterm: 15%
 - Final: 20%

Relation to EE/CSE/EPE Outcomes

Outcome	Level	Demonstrate Proficiency
	N, M, H	e.g. Exams, projects, HW
Mathematics, science and engineering	H	Exams, Project, HW
Basic disciplines in Electrical Engineering	H	Exams, Project, HW
Depth in Electrical Engineering	M	Exams, Project, HW

N = none

M = moderate

H = high

Basic disciplines in Computer & Sys. Eng.	H	Exams, Project, HW
Depth in Computer and Systems Eng.	H	Exams, Project, HW
Basic disciplines in Electric Power Eng.	N	
Conduct experiments and interpret data	M	Project
Identify, formulate and solve problems	H	Project, HW, Exams
Design a system, component or process	M	Project, HW, Exams
Communicate in written and oral form	M	Project
Function as part of a multi-disciplinary team	N	
Preparation for life-long learning	M	Project
Ethical issues; safety, health, public welfare	N	
Humanities and social sciences	N	
Laboratory equipment and software tools	H	Project, HW
Variety of instruction formats	M	Lecture, studio

Topics Covered:
(number of hours or classes for each)

1. VLSI architecture design fundamentals – 12 classes
2. High performance FIR and IIR filter design – 6 classes
3. Case study in digital communication – 5 classes
4. Synopsys tutorial – 6 classes

Computer Usage:

Students use MATLAB/C for system modeling, and use Synopsys to design, simulate, and synthesis the system.

Laboratory Experiences:

Design Experiences:

Independent Learning Experiences:

1. A significant literature survey and research required for project

Class/Lab Schedule:

Monday and Thursday Lectures from 10 – 11:20 am

Contribution to the Professional Component:

- (a) College-level mathematics and basic sciences: 0 credit hours
 (b) Engineering Topics (Science and/or Design): 3 credit hours
 (c) General Education: 0 credit hours

Prepared by:	Tong Zhang
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