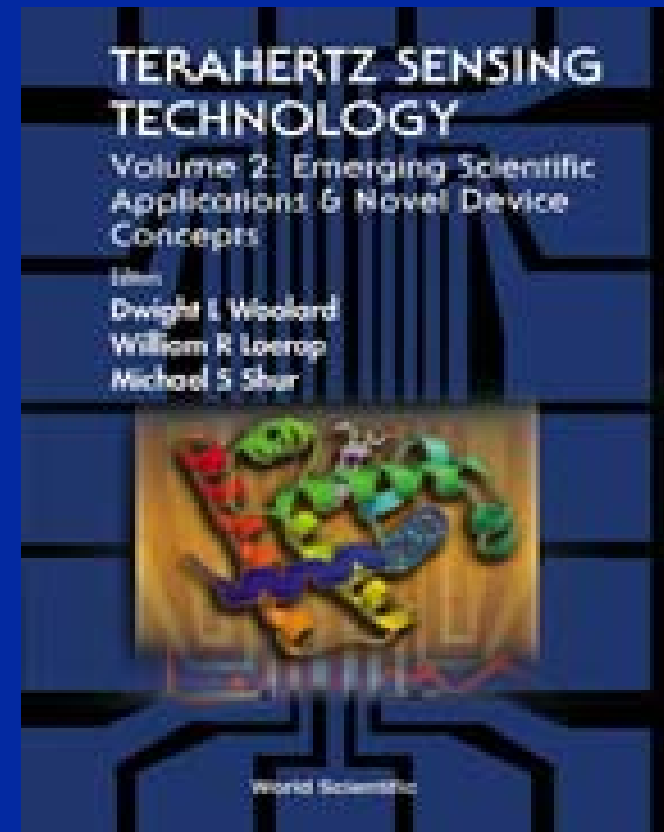
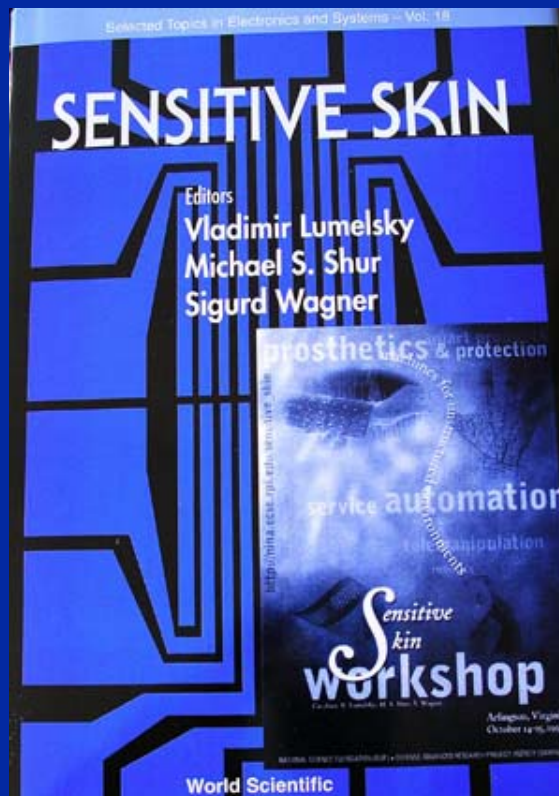


# BiCMOS



	Description	Comments	Applications
MOSFET	Metal Oxide Field Effect Transistor	The most important solid-state device. Almost all MOSFETs are made from Si and utilize the Si-SiO <sub>2</sub> interface	All electronics circuits, Very Large Scale Integrated Circuits (VLSI). Integration scale is up to 10 <sup>8</sup> transistors per chip or higher
CMOS	Complementary Metal Oxide Field Effect Transistor	The most important solid-state technology utilizing both <i>n</i> -channel and <i>p</i> -channel Si MOSFETs	Primarily low power VLSI. Short channel CMOS exhibits fairly high speed of operation
BiCMOS	Bipolar CMOS technology	Technology utilizing both CMOS and Bipolar Junction transistors integrated on the same semiconductor chip	High speed and high performance VLSI
a-Si TFTs	Amorphous Silicon Thin Film Transistors	Cheap and reliable technology for very large area integrated circuits (up to a square foot or larger), which uses thin a-Si films deposited on inexpensive glass substrates	Typical gate sizes 3 to 15 μm – an order of magnitude larger than for other FETs. Very slow technology. Applications include flat panel displays, imagers, printers, copiers, consumer products. Probably the second most important semiconductor technology (after CMOS and MOS technology)
poly-Si TFTs	Polysilicon Thin Film Transistors	Much better performance and higher speed than for a-Si TFTs but a much more expensive technology requiring higher processing temperatures	Applications include high-resolution projection displays. In the future, this technology may challenge a-Si TFTs
MESFETs	Metal Semiconductor Field Effect Transistors	Primarily made from GaAs, which is a higher speed material than Si. Also, GaAs substrates are highly resistive, which makes this technology suitable for microwave and millimeter wave applications	Applications include microwave and millimeter wave devices and integrated circuits and, more recently, optoelectronic circuits. Digital GaAs MESFET integrated circuits exhibit higher speed and/or lower power consumption than comparable Si integrated circuits. Integration scale up to 10 <sup>5</sup> transistors per chip or higher

From M. S. Shur,  
Introduction to Electronic Devices,  
John Wiley (1996)

# IBM Blue Logic™ BiCMOS 6HP

- IBM Semiconductor 0.18 Micron 7HP SiGe BiCMOS Process
- MOSIS is offering access to the IBM 0.18 micron SiGe BiCMOS 7HP technology for prototype and low volume fabrication. C4 (IBM's flip chip bumping) is available at an additional cost.

This BiCMOS SiGe process has 5 metal layers and other options for the standard MPW runs. Other configurations are available for dedicated runs or on MPW runs at an additional cost.

To insure that submitted data is on a 20 nm grid, please stream-out at 1 DBU = 20 nm (Cadence 0.020, not 0.001). Supply voltages are 1.8 V core and 2.5/3.3 V I/O. For reference, see the SiGe process comparison.

<http://www.mosis.org/products/fab/vendors/ibm/7hp/>

# IBM 6HP BiCMOS Process

## HP 70.18 micron

### Specifications

#### SiGe HBT NPNs

	High-Speed Device	High-Voltage Device
Beta	100	88
$f_t$ (@ $V_{cb} = 1\text{ V}$ )	47 GHz	27 GHz
$f_{max}$	65 GHz	55 GHz
$V_{early}$	75 V	180 V
$BV_{ceo}$	3.35 V	5.4 V

#### FETs

	NFET		PFET	
	2.5 V	3.3 V	2.5 V	3.3 V
$T_{ox}$	5.0 nm	7.0 nm	5.0 nm	7.0 nm
$L_{eff}$	0.18 $\mu\text{m}$	0.26 $\mu\text{m}$	0.18 $\mu\text{m}$	0.265 $\mu\text{m}$
$I_{Dsat}$	595 $\mu\text{A}/\mu\text{m}$	580 $\mu\text{A}/\mu\text{m}$	280 $\mu\text{A}/\mu\text{m}$	285 $\mu\text{A}/\mu\text{m}$

<http://www.mosis.org/products/fab/vendors/ibm/6hp/>

# IBM 6HP BiCMOS Process

## Capacitors

MOS Cap	310 fF/ $\mu\text{m}^2$
MIM Cap	0.70 fF/ $\mu\text{m}^2$

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## Resistors

Polysilicon 1	3600 ohms/sq
Polysilicon 2	210 ohms/sq
Silicon 1	100 ohms/sq
Silicon 2	63 ohms/sq

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## Diodes

VARactor	1.14 fF/ $\mu\text{m}^2$ @ 0 V $V_f = 810$ mV@100 $\mu\text{A}$
ESD	4000 V HBM

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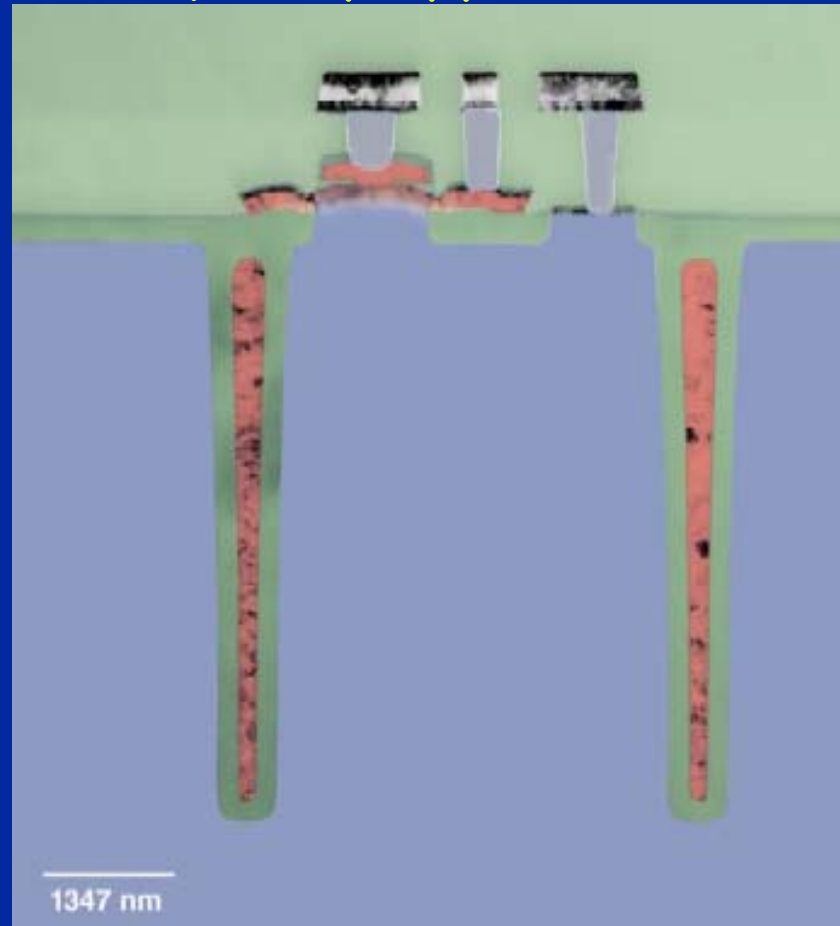
## Analog Metal Spiral Inductors

Inductance values range from 0.28 nH to 83 nH with outer dimensions between 100  $\mu\text{m}$  and 450  $\mu\text{m}$ . Example: Q value of 19 @ 10 GHz for a 0.6-nH inductor.

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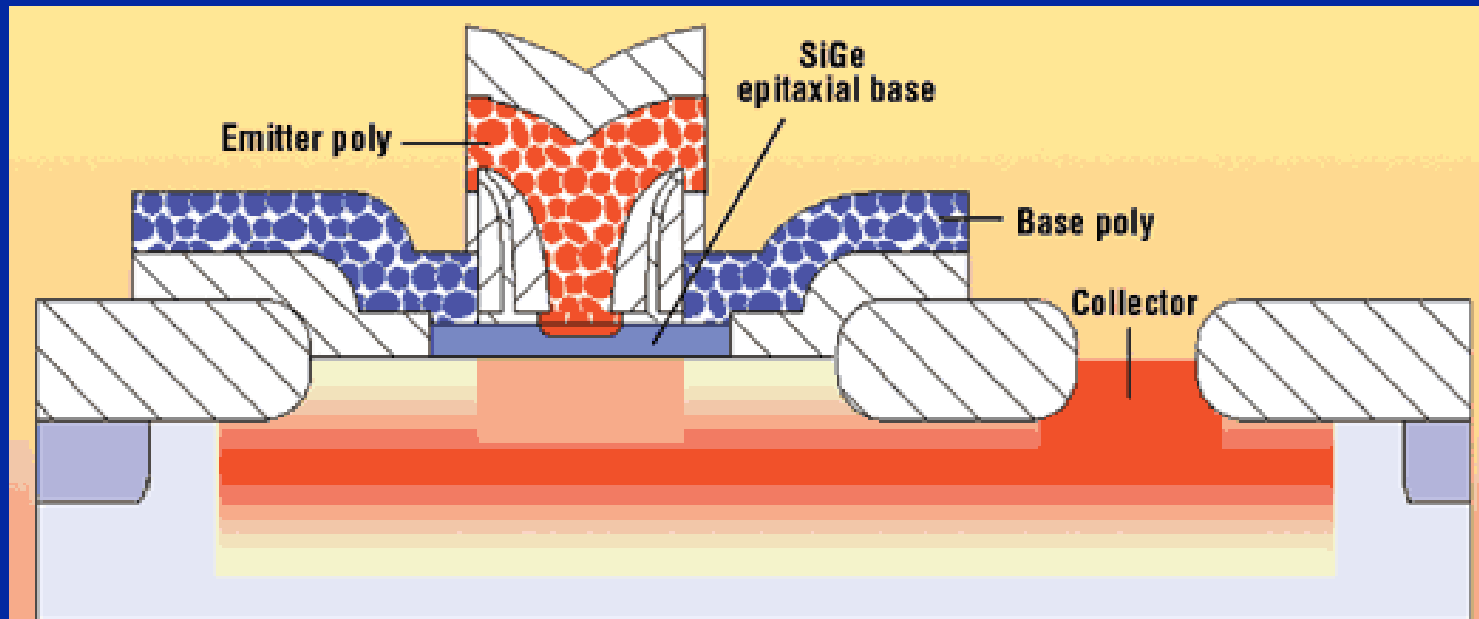
<http://www.mosis.org/products/fab/vendors/ibm/6hp/>

SiGe NPN transistors have a minimum 0.30- $\mu\text{m}$ -wide emitter and deep trench isolation for optimal performance in high-frequency applications



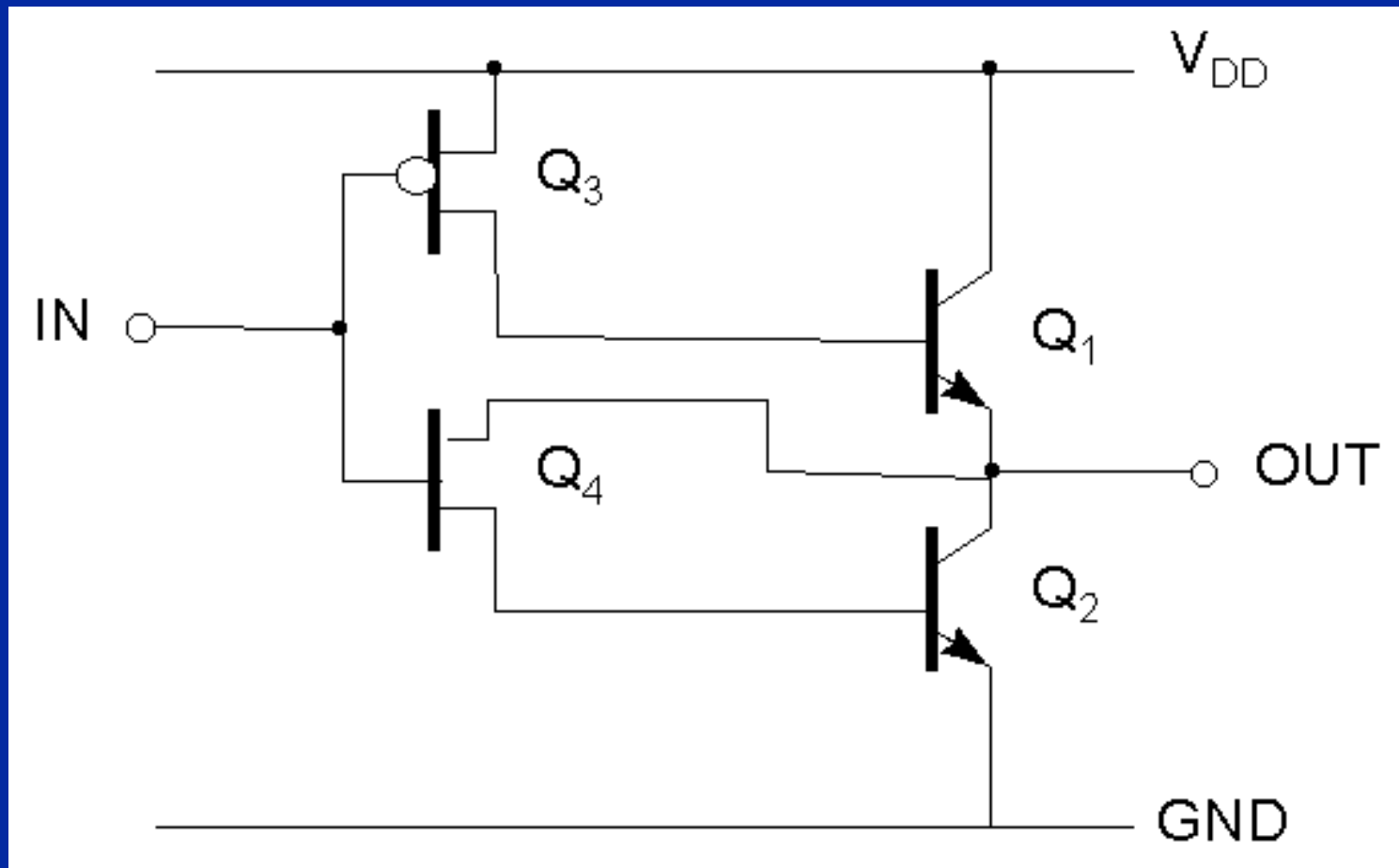
<http://www.mosis.org/products/fab/vendors/ibm/6hp/>

From  
[http://www.elecdesign.com/Files/29/1006/Figure\\_01.gif](http://www.elecdesign.com/Files/29/1006/Figure_01.gif)



With just four additional mask steps over the core 0.25- $\mu\text{m}$  CMOS process, Bell Laboratories' researchers developed a high-performance, super-self-aligned (SSA), graded-base silicon-germanium bipolar transistor. The end result was the creation of a low-cost modular biCMOS process. The device offers a peak cutoff,  $f_T$ , of 51 GHz and a maximum oscillation frequency,  $f_{MAX}$ , of 53 GHz.

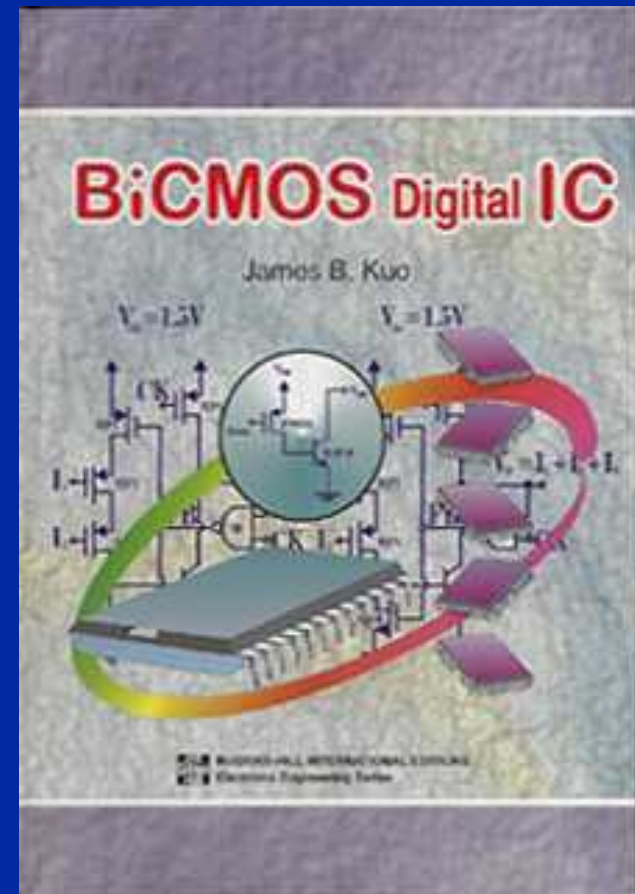
# Circuit Example



# Example: Inverter Driving 50 pF load

<http://www2.eng.cam.ac.uk/~dmh/3b2/bicmosinv.htm>

## BiCMOS Book



# 200 GHz BiCMOS

Jazz Semiconductor (Newport Beach, CA) has announced a complete design platform in concert with its new 200-GHz SiGe BiCMOS technology, the SBC18H2 process, which is well suited for RF, microwave, and millimeter-wave integrated analog and mixed-signal semiconductor chips. The company has validated key circuit building blocks for next-generation products, including 60-GHz wireless data and collision avoidance radars. As a companion to the 200-GHz SiGe process, the new design environment supports fully scalable device models for SiGe bipolar and RF CMOS, statistical simulation with mismatch capabilities, an integrated inductor design toolbox, and other features that enhance predictability for first-time manufacturing success.

From August 31, 2004 [Jazz Semiconductor Unleashes 200-GHz SiGe BiCMOS Process](#)  
[Microwaves & RF](#) - *Jack Browne*

CMOS/BiCMOS ULSI: Low Voltage, Low Power  
by Kiat-Seng Yeo, Samir S. Rofail, and Wang-Ling Goh  
(Dec 27, 2001)

