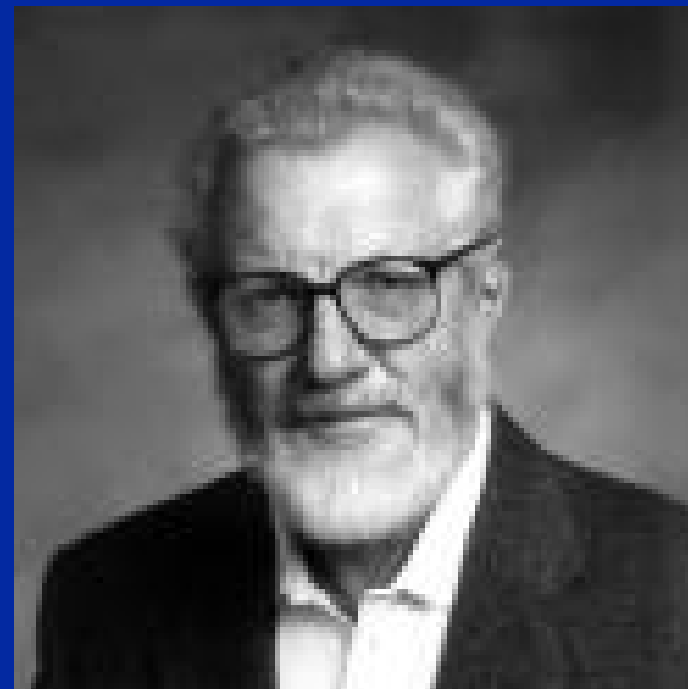


# Heterojunction Bipolar Transistors

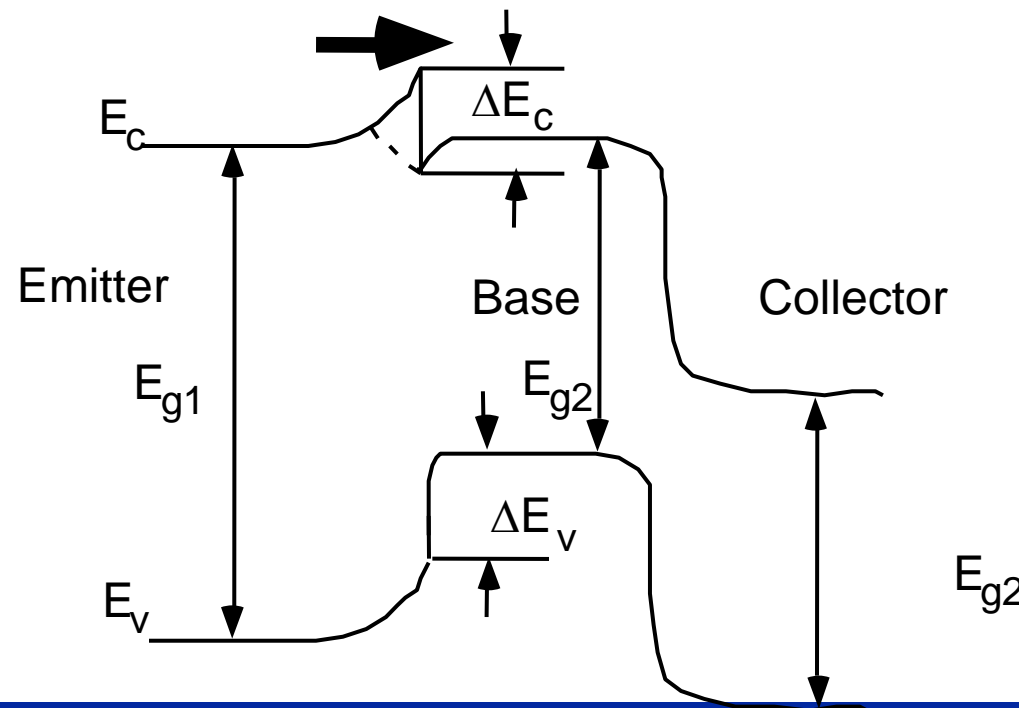


# Outline

- HBT advantages
- Principle of operation.
- HBT and material systems
- HBT device structures
- HBT design, modeling, and characterization.
- HBT scaling and performance limits.
- Ballistic effects in HBTs?
- Tunneling Emitter Bipolar Transistors.
- HBT applications in systems.

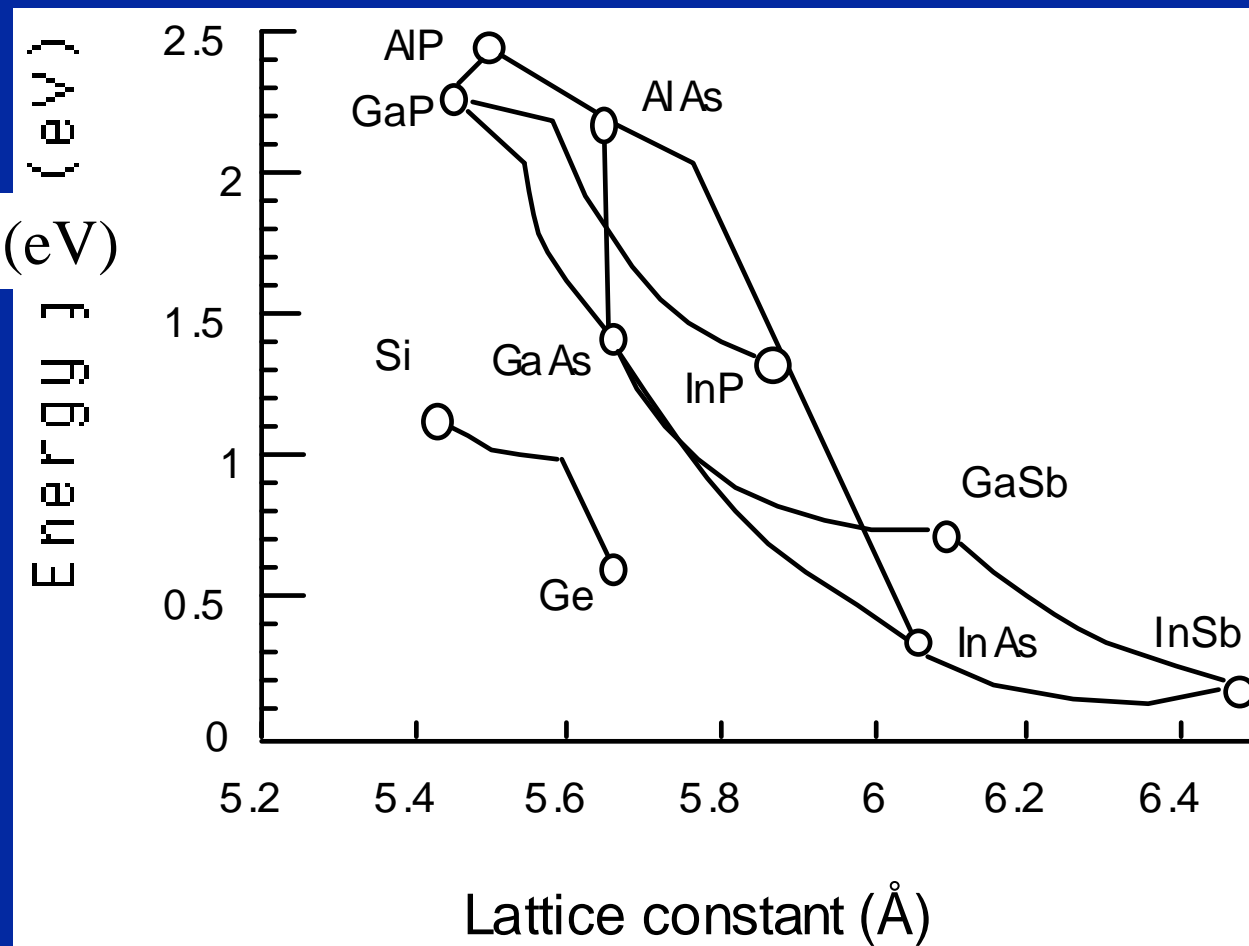
# Principle of operation

$$\beta = \frac{I_c}{I_b} < \beta_{max} = \frac{D_n N_{de} X_e}{D_p N_{ab} W} \exp\left(-\frac{\Delta E_g}{k_B T}\right)$$



# Heterostructure Materials Systems

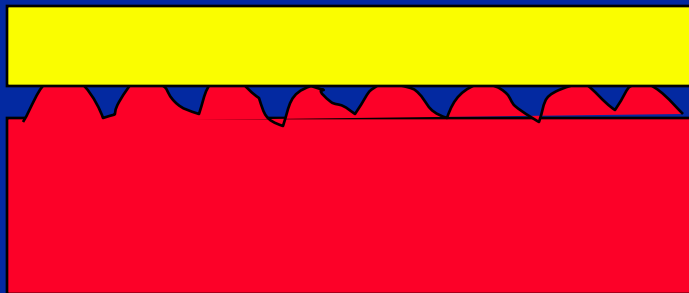
Energy gap (eV)



# Novel Substrates for Heteroepitaxy

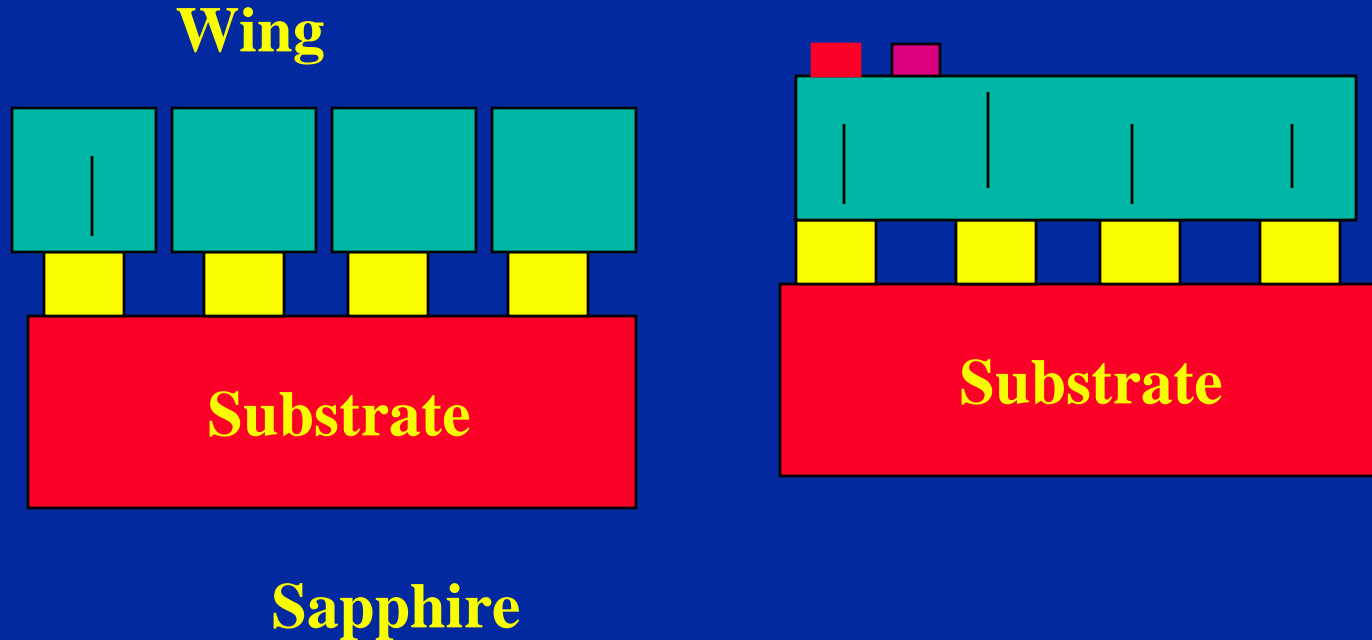


Epitaxial layer  
Buffer  
Substrate



Patterned Substrate  
(Porous substrate)

# Lateral Epitaxial Overgrowth



## Conduction band discontinuities

- AlGaAs/GaAs  $\Delta E_c = 0.65 \Delta E_g$
- InGaP/GaAs  $\Delta E_c < 0.1 \Delta E_g$
- AlInAs/InGaAs  $\Delta E_c = 0.15 \text{ to } 0.5 \Delta E_g$
- InP/InGaAs  $\Delta E_c = 0.24 \Delta E_g$

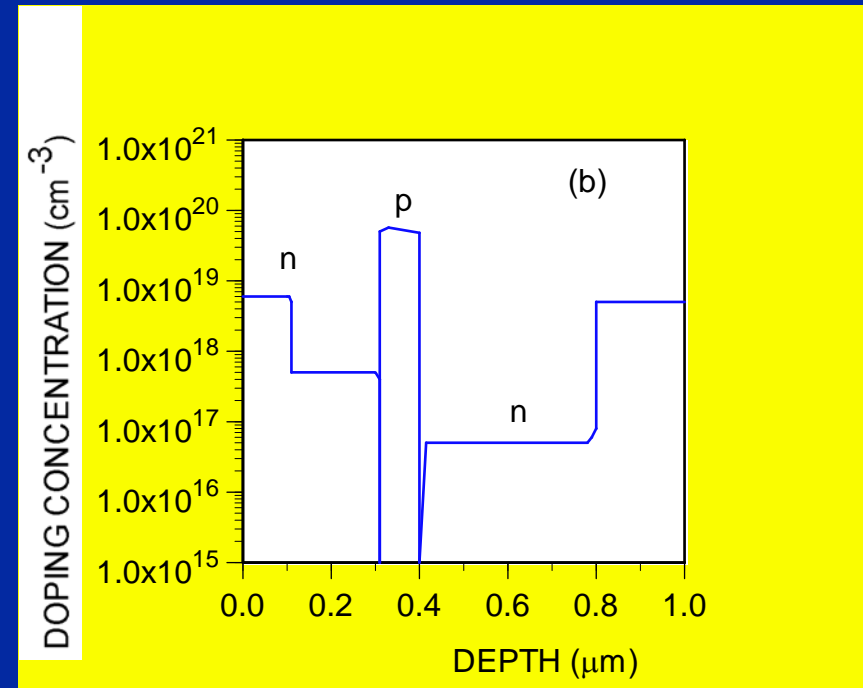
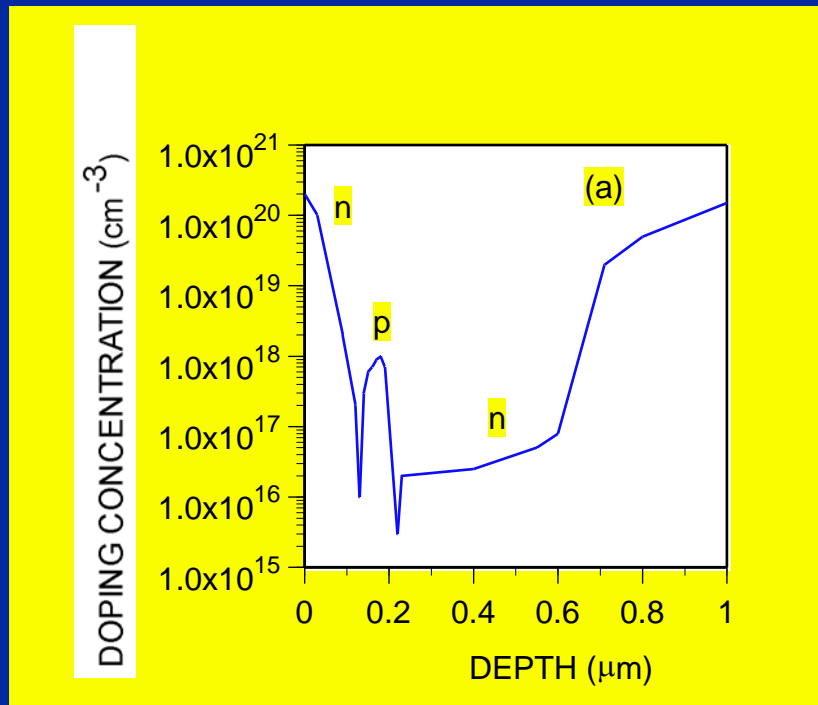
After G. B. Gao et al. in "Compound Semiconductor Technology. The Age of Maturity", World Scientific, 1996, pp. 85-173  
ed. M. S. Shur, ISBN 981-02-2325

See <http://www.eecs.umich.edu/dp-group/developments/HBTs.html>  
for GaAs and InP based HBT research

## HBT advantages

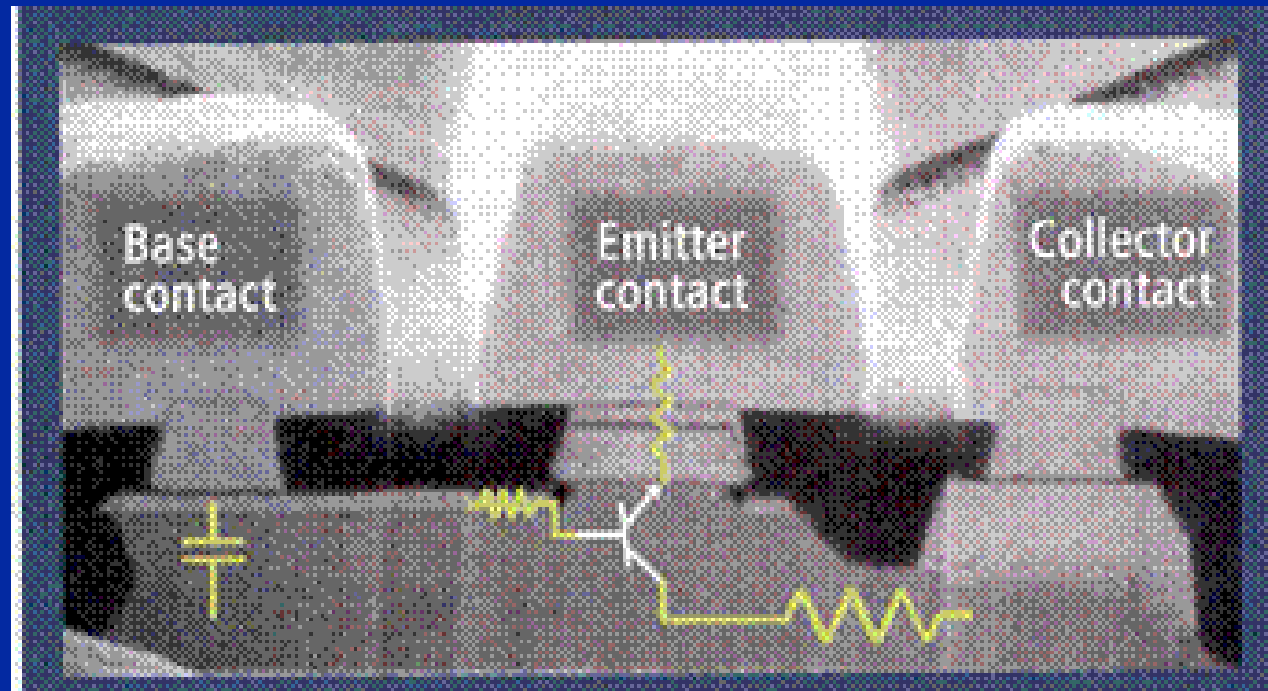
- Low base spreading resistance
- High electron mobility (for compound semiconductors) and ballistic and overshoot effects
- Can be integrated with HEMTs, MESFETs, Schottky diodes
- Low  $1/f$  noise

# Typical BJT and HBT Doping Profiles



Impurity profile in homojunction (a) and heterojunction (b) bipolar transistors. (After Gao et al., *Compound Semiconductor Electronics: The Age of Maturity*. Ed. M. S. Shur, (World Scientific, New Jersey, 1996), p. 89.)

## Parasitic elements in HBTs



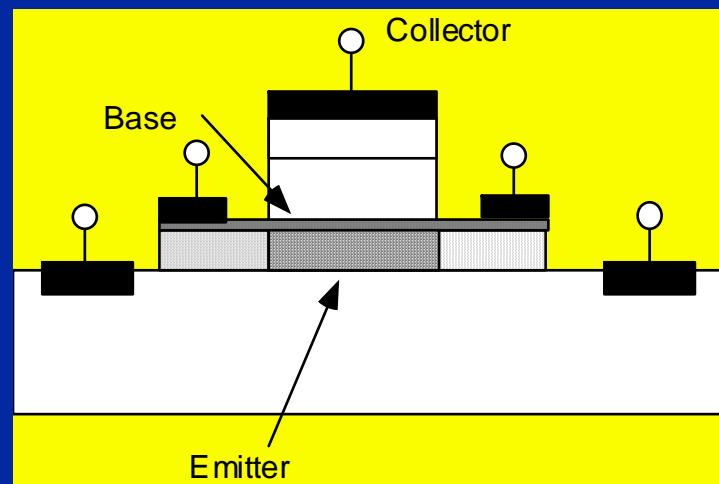
From: Gopal Raghavan, Marko Sokolich, William E. Stanchina,  
*"Indium Phosphide ICs unleash the high-frequency spectrum"*,  
IEEE Spectrum, October 2000, p. 47-52.

## Concerns

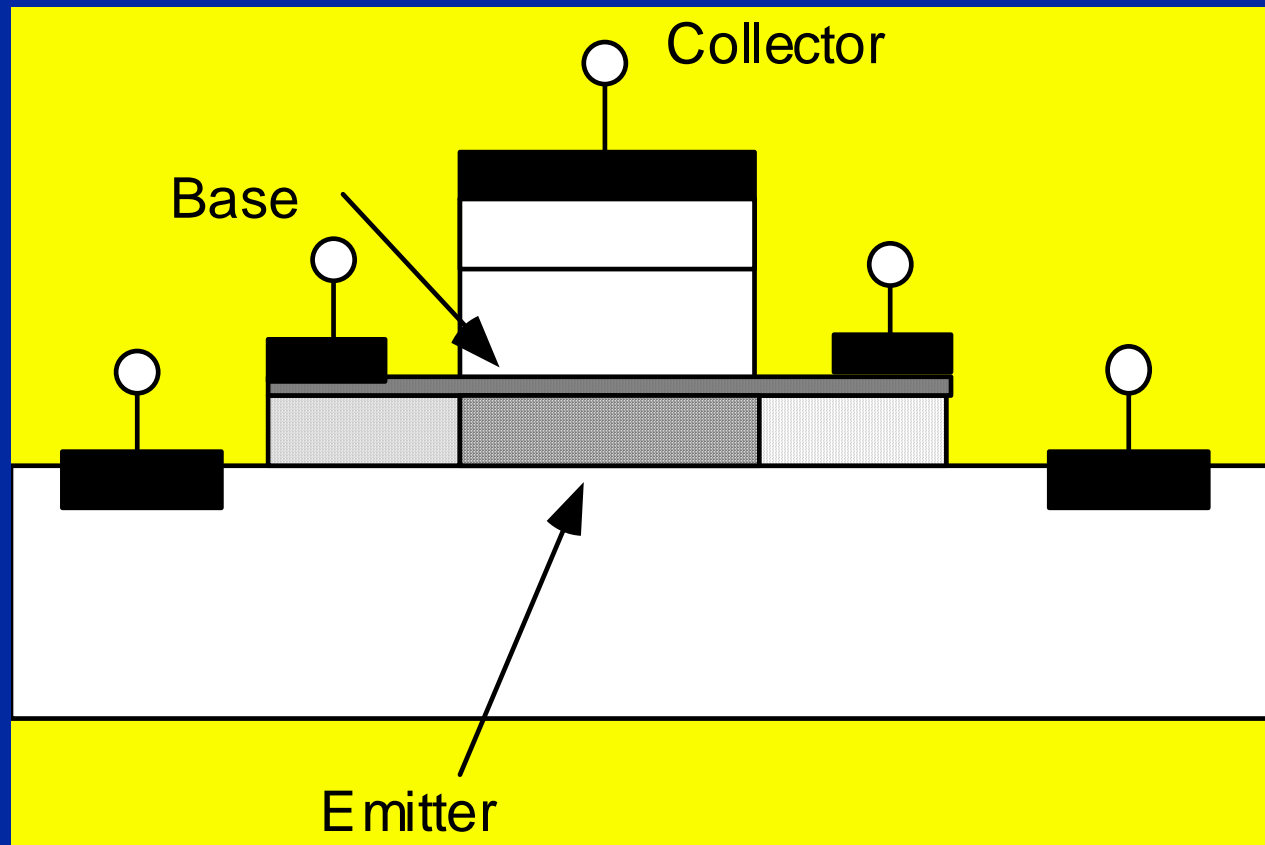
- Reliability
- Relatively high operating voltage

# Collector on Top

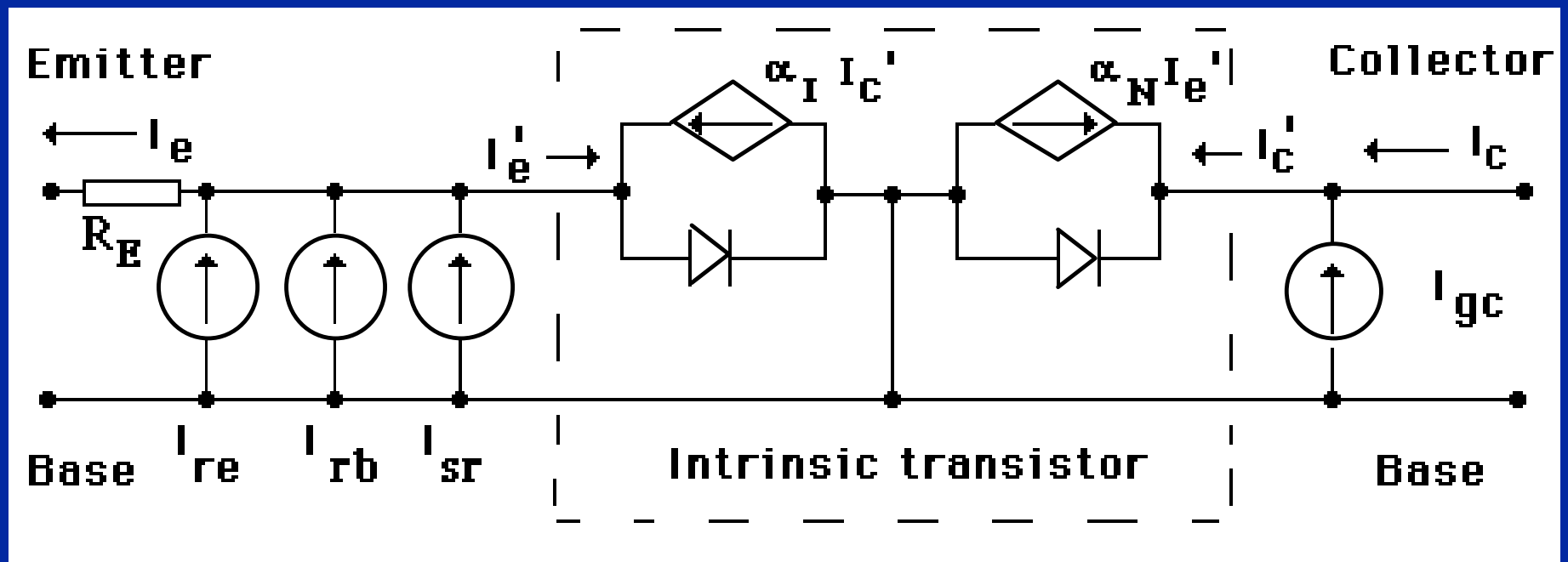
Most HBTs are emitter-on-top structures). However, as was pointed out by Kroemer (1982), (1983) the collector capacitance may be substantially smaller for the collector-on-top configuration. This was confirmed by the circuit simulation of HBTs reported by Akagi et al. (1986) who predicted a higher speed for collector-on-top configurations when comparing non-self-aligned structures. The figure below (after S. Yamahata et al. (1993)) shows the collector-up design



# Collector on Top Structure



# Equivalent Circuit

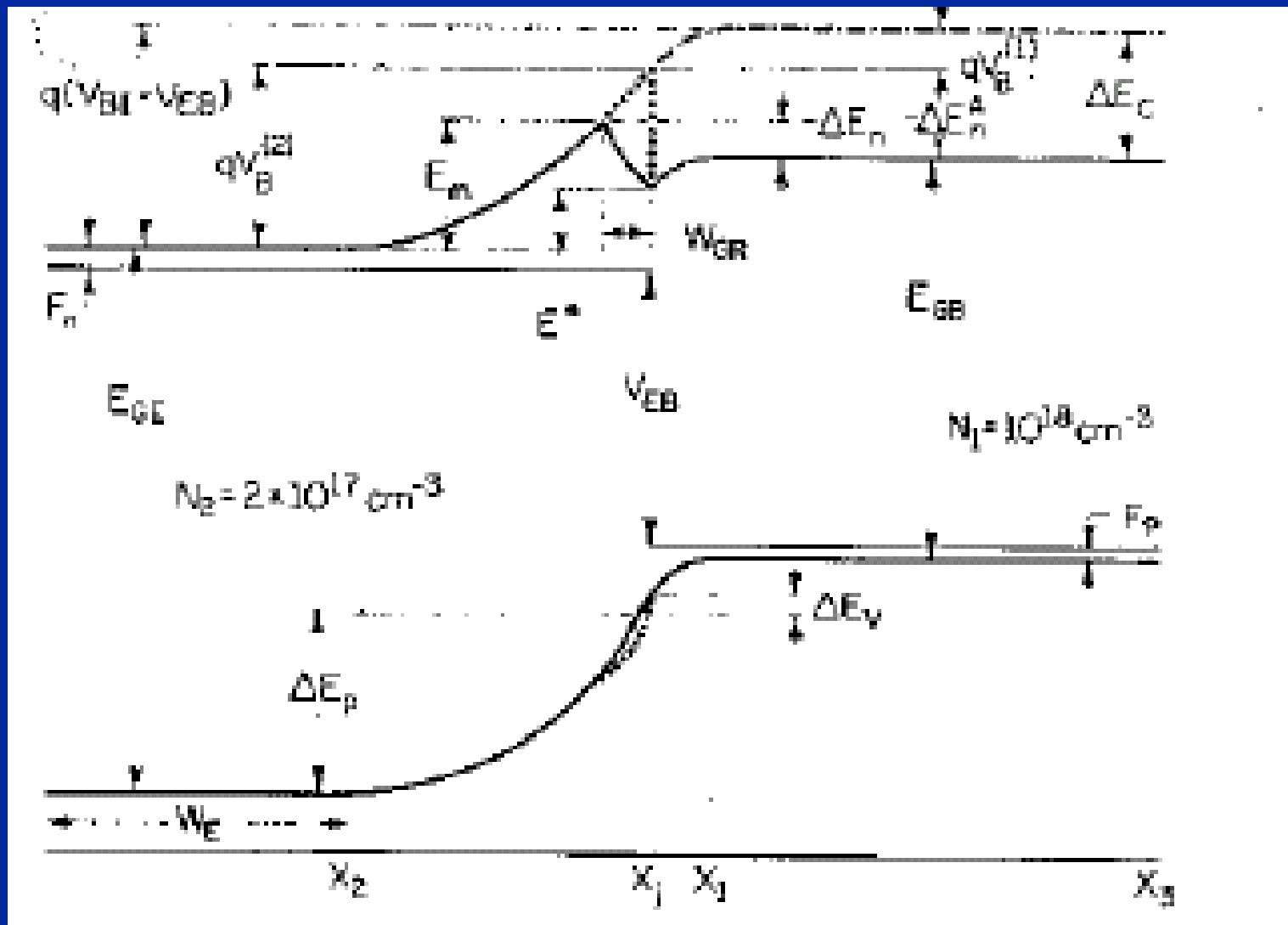


## HBT modeling

- Thermionic-Emission-Diffusion model.
- Thermionic-Field-Emission-Diffusion Model.
- Thermionic-field-diffusion model for an HBT with a graded emitter

Slides 17 – 23 are from A. A. Grinberg, M. S. Shur, R. Fisher, and H. Morkoc,  
An Investigation of the Effect of Graded Layers and Tunneling on the Performance of AlGaAs/GaAs Heterojunction Bipolar Transistors,  
IEEE Trans. on Electron Devices, Vol. ED-31, No. 12, pp. 1758-65, December (1984)

# Band Diagram at Heterointerface



# Current across abrupt heterointerface

$$J_n(X_j) = -q \frac{v_n}{4} \{n(X_j^-) - n(X_j^+) \exp(-\Delta E_c/kT)\} \quad (1)$$

where  $\Delta E_c$  is the conduction band discontinuity at the heterointerface

$$v_n = \left( \frac{8kT}{\pi m_n^*} \right)^{1/2}$$

## Carrier concentrations at heterointerface

$$\begin{aligned}
 n(X_j^-) &= n(X_2) \exp(-qV_B^{(2)}/kT) \\
 n(X_j^+) &= n(X_1) \exp(+qV_B^{(1)}/kT)
 \end{aligned}
 \tag{2}$$

where

$$\begin{aligned}
 V_B^{(1)} &= (V_{BI} - V_{EB}) \xi \\
 V_B^{(2)} &= (V_{BI} - V_{EB}) (1 - \xi)
 \end{aligned}
 \tag{3}$$

$$\xi = N_2 \epsilon_2 / (N_1 \epsilon_1 + N_2 \epsilon_2).
 \tag{4}$$

## Current should be equal to the diffusion current

$V_{BF}$  is the built-in potential and  $V_{EB}$  is the applied forward bias voltage. The electron current density given by (1) should be equal to the electron current density due to diffusion  $J_n(X_1)$  at the boundary of the space-charge region in the base ( $X_1$  in Fig. 1).

$$J_n(X_1) = - \frac{qD_{n1}}{L_1} \frac{(n(X_1) - n_1) \cosh(W_B/L_1) - (n(X_3) - n_1)}{\sinh(W_B/L_1)} \quad (5)$$

Here  $n_1$ ,  $D_n$ , and  $L_1$  are the equilibrium concentration, diffusion coefficient and diffusion length of the electrons in the base, respectively,  $W_B$  is the base width and  $X_3$  is the boundary coordinate of the base-collector space-charge region in the base.

# Results

$$J_E = A_{11} (\exp(qV_{EB}/kT) - 1) \\ + A_{12} (\exp(-qV_{CB}/kT) - 1) - J_{RG}^E$$

$$J_C = A_{21} (\exp(qV_{EB}/kT) - 1) \\ + A_{22} (\exp(-qV_{CB}/kT) - 1)$$

# Where

where

$$A_{11} = - \left\{ \frac{J_{nE}}{R_n} \cosh \left( \frac{W_B}{L_1} \right) + \frac{-J_{pE}}{R_p} \cosh \left( \frac{W_E}{L_2} \right) \right\}$$

$$A_{22} = \left\{ \frac{J_{nE}}{R_n} \left[ \cosh \left( \frac{W_B}{L_1} \right) + \eta_n \sinh^2 \left( \frac{W_B}{L_1} \right) \cdot \exp \left( - \frac{\Delta E_n}{kT} \right) \right] + J_{pc} \cdot \cosh \left( \frac{W_c}{L_3} \right) \right\}$$

$$A_{12} = - A_{21} = + J_{nE}/R_n \quad (18)$$

# Thermionic Diffusion Model and Thermionic Field Diffusion Model

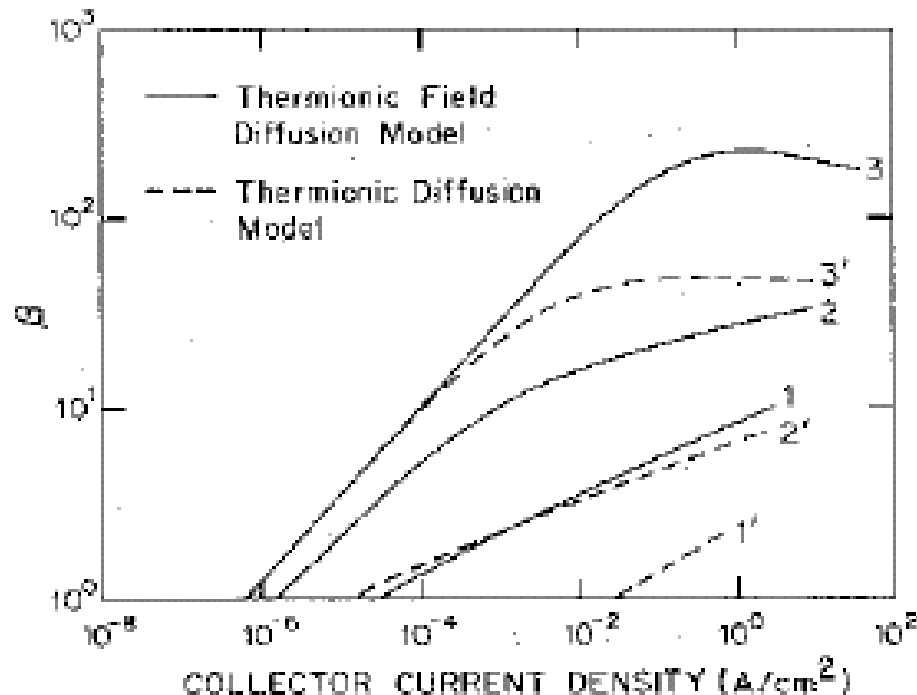
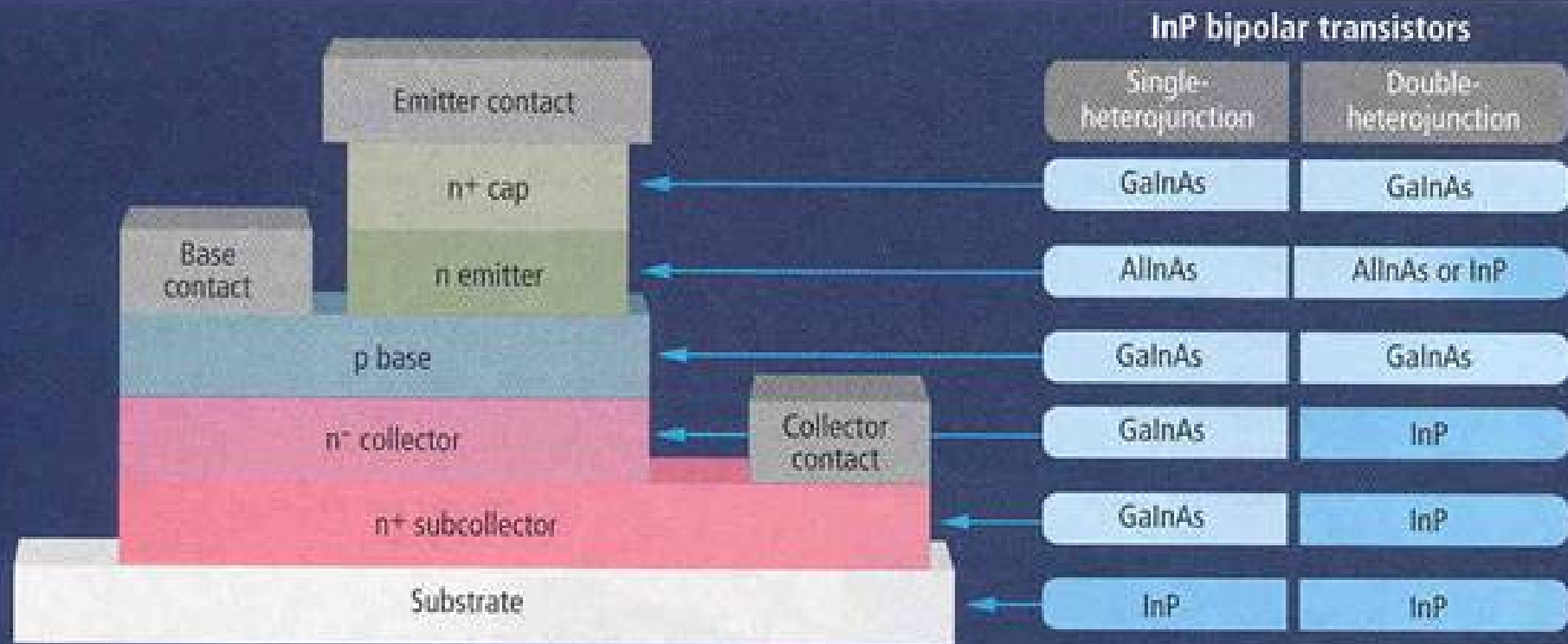


Fig. 2. Common emitter current gain  $\beta$  as function of the collector current for the abrupt heterojunction  $N_2 = 2 \times 10^{17} \text{ cm}^{-3}$ ,  $T = 300 \text{ K}$ . For 1 and 1',  $N_1 = 4 \times 10^{17} \text{ cm}^{-3}$ ; for 2 and 2',  $N_1 = 3 \times 10^{17} \text{ cm}^{-3}$ ; and in 3 and 3',  $N_1 = 2 \times 10^{17} \text{ cm}^{-3}$ .

# InGaAs/AlInAs and InGaAs/InP HBTs



[2] Single- and double-heterojunction bipolar transistors (SHBTs and DHBTs, respectively) are made using a combination of materials, but start with an indium phosphide substrate. The ratio of gallium to indium in these transistors is 47:53, and the ratio of aluminum to indium is 48:52.

From: Gopal Raghavan, Marko Sokolich, William E. Stanchina, *"Indium Phosphide ICs unleash the high-frequency spectrum"*, IEEE Spectrum, October 2000, p. 47-52.

## HBTs with InGaP Emitters (instead of AlGaAs)

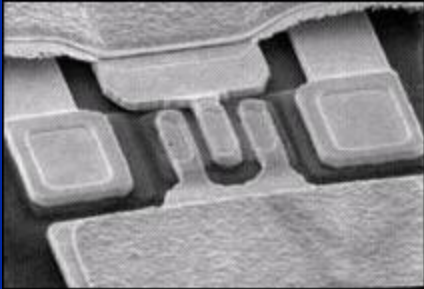
### Advantages:

- Higher yield
- Better reliability
- Higher etch selectivity
- Large valence band discontinuity with GaAs (0.3 eV)
- Low surface recombination velocity

### Companies involved

- Nortel
- GEC
- HP
- TriQuint

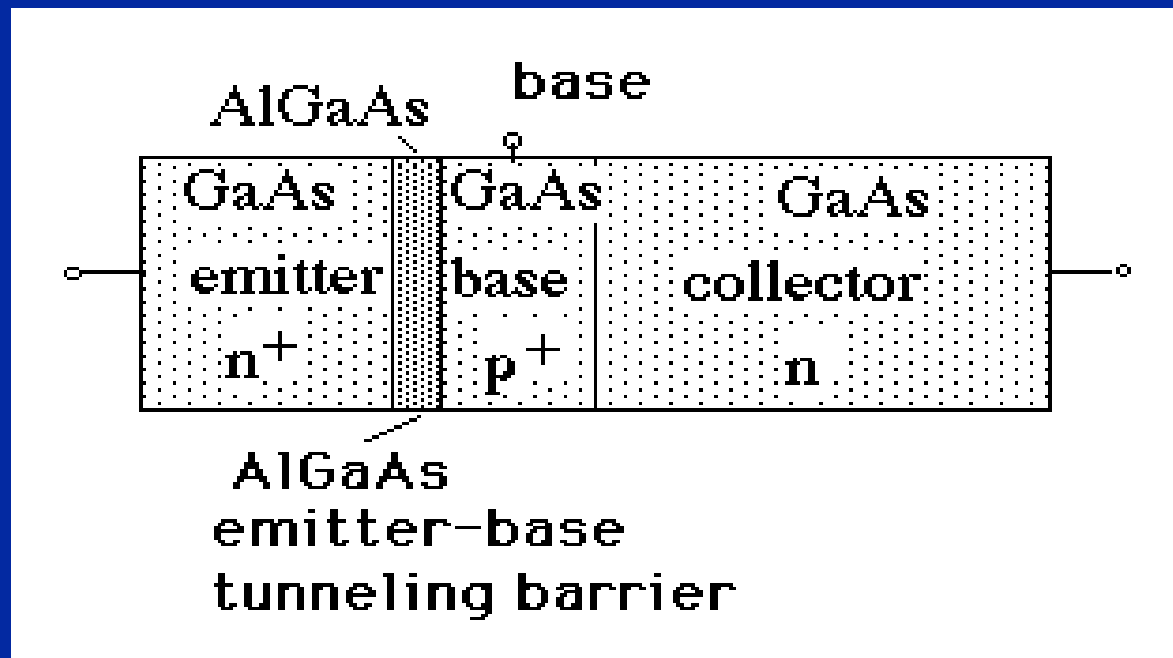
# InGaP/GaAs HBT



From [www.cen.uiuc.edu/~gstill/fab.html](http://www.cen.uiuc.edu/~gstill/fab.html)

Layer	InGaP/GaAs HBT	InP/InGaAs HBT
Emitter Cap	InGaAs/GaAs	InGaAs
Emitter	InGaP	InP
Base	GaAs	InGaAs
Collector	GaAs	InGaAs
Subcollector	GaAs	InGaAs
Substrate	GaAs	InP

# Tunneling Emitter Bipolar Transistor



Schematic diagram of Tunneling Emitter Bipolar Transistor (TEBT) (from Xu and Shur (1986)).

# TEBT operation

A new type of a heterojunction bipolar transistor - a Tunneling Emitter Bipolar Transistor (TEBT) - was proposed by Xu and Shur (1986) and fabricated by Najjar et al. (1986). In this device a wide band gap AlGaAs emitter is replaced by a conventional  $n^+$  GaAs emitter but a thin compositionally graded AlGaAs layer is inserted between the emitter and base regions (see Fig. 3-14-5). This layer has vastly different tunneling rates for electrons and holes, so electrons can easily go through but holes are prevented from being injected into the emitter region. This is reminiscent of a "mass filtering" idea proposed by Capasso et al. (1985) for superlattice devices. The TEBT should have smaller emitter contact resistance, higher gain, fewer traps, and higher speed of operation than a conventional HBT.

## References.

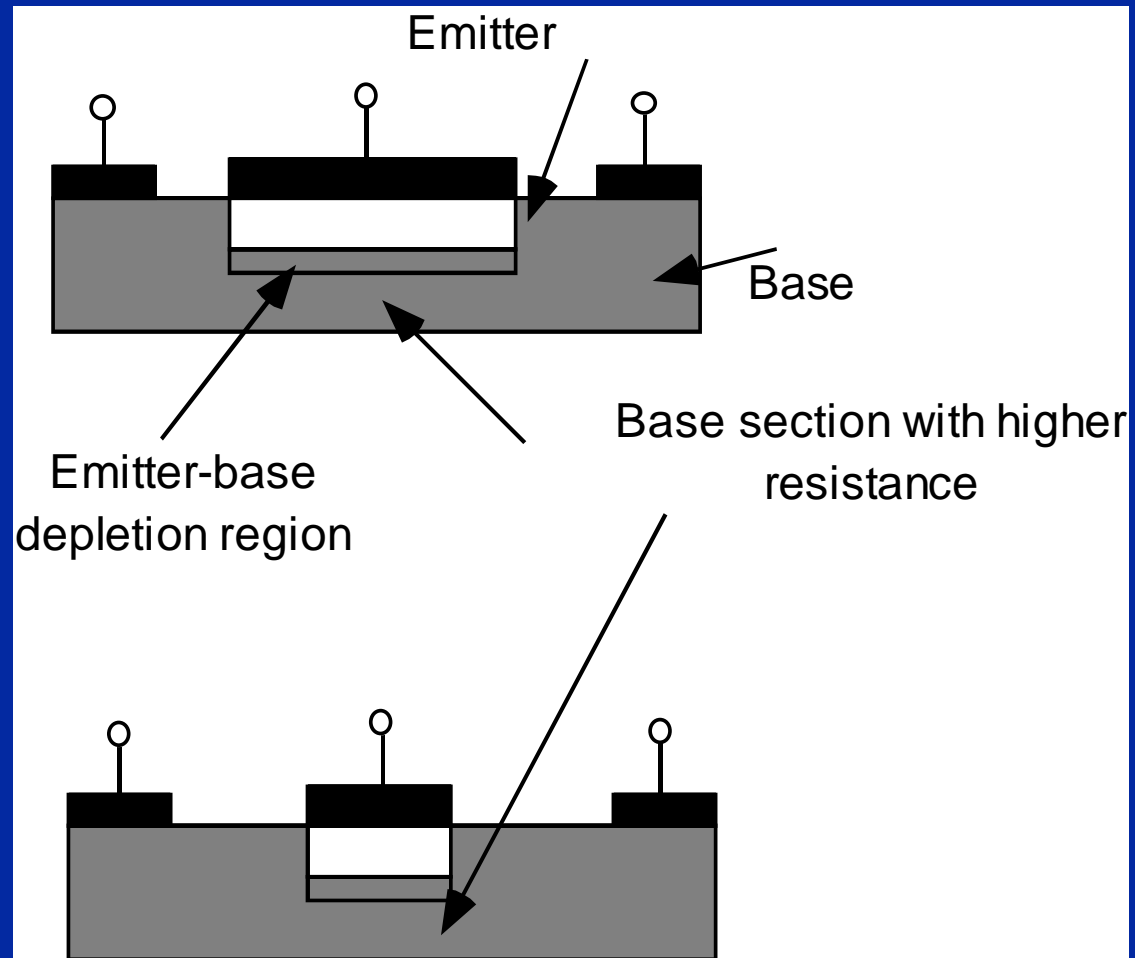
- F. Capasso, K. Mohammed, A. Y. Cho, R. Hull, and A. L. Hutchinson, "Effective Mass Filtering: Giant Quantum Amplification of the Photocurrent in a Semiconductor Superlattice," *Appl. Phys. Lett.*, 47 (4), pp. 420-422 (1985)
- J. Xu and M. Shur, "Tunneling Emitter Bipolar Junction Transistor," *IEEE Electron Device Letters*, EDL-7, pp. 416-418 (1986)
- F. E. Najjar, D. C. Radulescu, Y. K. Chen, G. W. Wicks, P. J. Tasker, and L. F. Eastman, "DC Characterization of the AlGaAs/GaAs Tunneling Emitter Bipolar Transistor," *Appl. Phys. Lett.*, 50, p. 1915 (1987)

# HBT performance

Materials System	Current Gain	$f_T$ (GHz)	$f_{max}$ (GHz)
AlGaAs/GaAs	12,500	171	350 *
AlGaAs/Ge/GaAs	300		
InP/InGaAs	49,000	175	180
InP/InGaAsP	112,000		
GaInP/GaAs	2,690	50	116
InAlAs/InGaAs	39	130	230
InGaAlAs/InGaAs	15,000		
$\beta$ -SiC/Si	300	30	
poly-Si/Si		74	
poly-Si/SiGe			53
Si/SiGe	5,000	116	120

Data taken from G. B. Gao, S. N. Mohammad, G. A. Martin, and H. Morkoç, in "Compound Semiconductor Electronics. The Age of Maturity", M. Shur, Editor, World Scientific (1996)., pp. 85-173

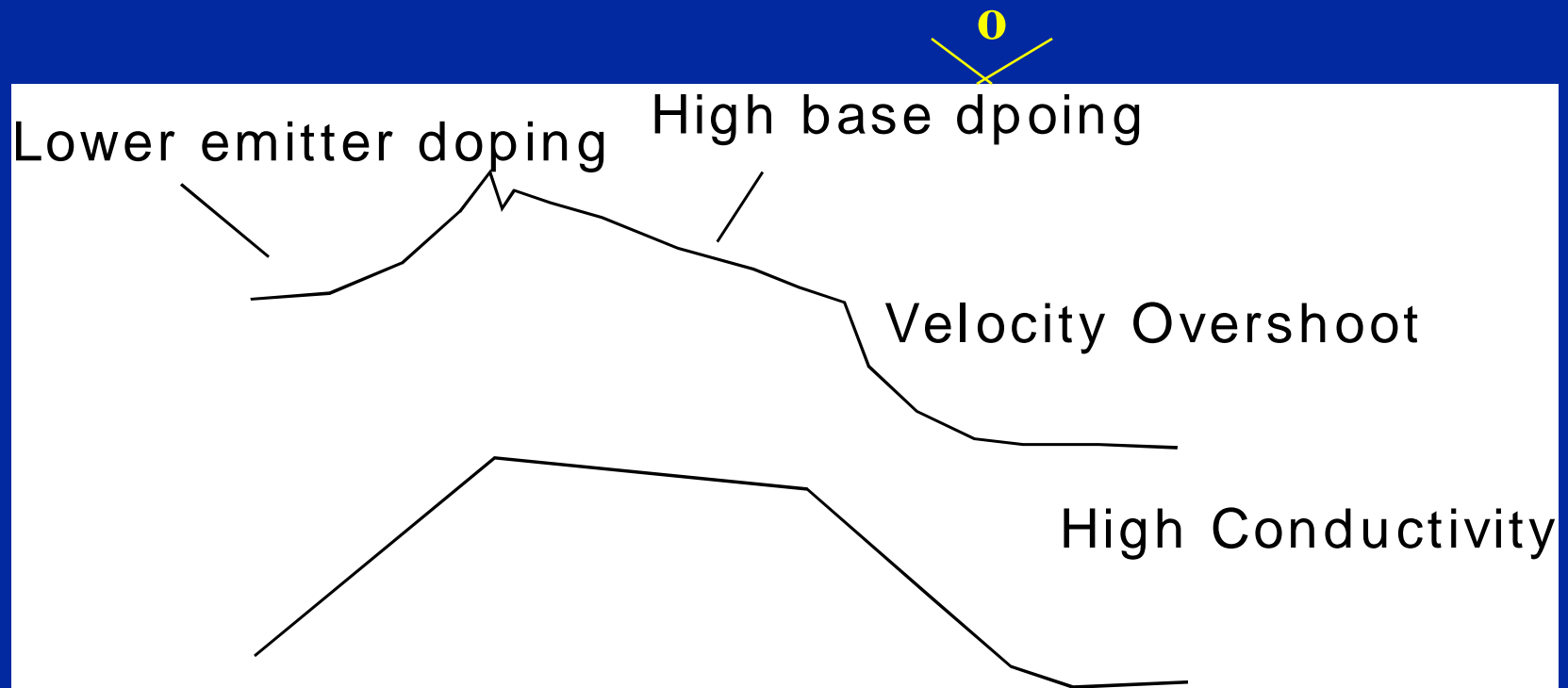
# HBT scaling



Parameter	Constant Power Scaling	Constant Power Density Scaling
Lithography scaling factor	S	S
Base thickness	$S^{0.8}$	Unchanged
Base doping	$1/S^2$	Unchanged
Collector doping	$1/S^2$	Unchanged
Emitter doping	Unchanged	Unchanged
Current density	$1/S^2$	Unchanged
Power supply voltage	Unchanged	Unchanged
Wiring capacitance	$1/S$	$1/S$
Logic propagation delay	S	$1 - S$
Power Dissipation	Unchanged	$1 - 1/S$

(from P. M. Asbeck, M. F. Chang, and K. Pedrotti,  
 Future Directions for HBT Development, IJHSES, vol. 5,  
 No. 3, Sep. 1994, pp. 493-527)

# Ballistic Transport in HBTs



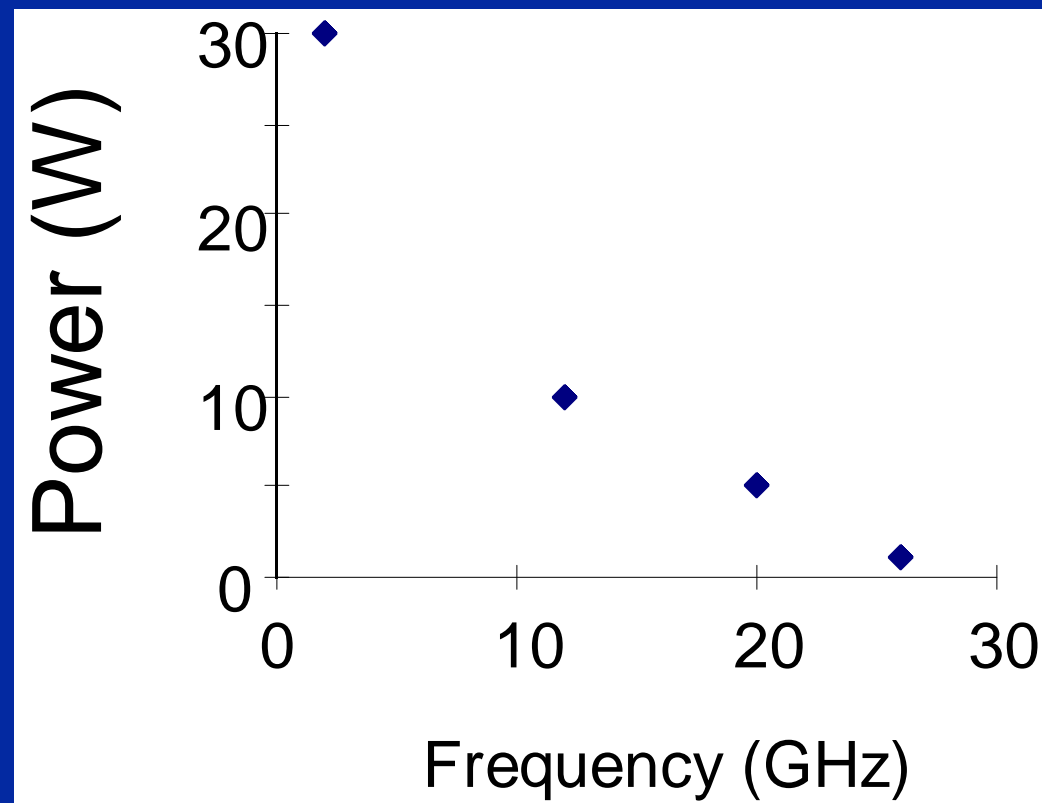
## Explanation

Ishibashi and Yamaguchi (1987) reported an HBT with a new device structure. They replaced an n-type GaAs collector layer by a double layer that included a relatively thick i-GaAs layer (2000 Å in their devices) and a thin p<sup>+</sup> GaAs layer (200 Å thick doped at  $2 \times 10^{18} \text{ cm}^{-3}$ ). The p<sup>+</sup> layer is totally depleted and introduces a potential drop and electric field in the i-layer resulting in a near ballistic collection of electrons in a certain voltage range. They obtained a very high cutoff frequency of 105 GHz.

T. Ishibashi and Y. Yamauchi, "A Novel AlGaAs/GaAs HBT Structure for Near Ballistic Collection," in Program of 45th Annual Device research Conference, June 22-24, Santa Barbara, p. IV-A6 (1987)

## Required output microwave power with linear amplifier gain for satellite communications systems.

(data from K. Friske, G. Gatti, H. Hartnagel, V. K. Rozer, and J. Wurfl, IEEE Trans. MTT, 40, pp. 1205-1214 (1992))



## GaN-based BJTs and HBTs

- Hole lifetime in GaN is  $\sim 7$  ns. GaN/AlGa<sub>N</sub> thyristors might support up to 5 kV operating voltages with current densities of 200 A/cm<sup>2</sup> and operate at frequencies exceeding 2 MHz, see
  - Z. Z. Bandic, E. C. Piquette, P. M. Bridger, T. F. Kuech, and T. C. McGill, Design and Fabrication of Nitride Based High Power Devices, in Proceedings of Materials Research Society Conference, December 1997, Boston, MA
- Pankove et al. reported on a new Heterojunction Bipolar Transistor that used a heterojunction between GaN and SiC. The transistor exhibited an extremely high gain of ten million at room temperature, decreasing to 100 at 535°C.
  - High-Power High-Temperature Heterobipolar Transistor With Gallium Nitride Emitter, MRS Internet J. Nitride Semicond. Res. Vol. 1, 39 (1996).
- UCSB first demonstration of an AlGa<sub>N</sub>/GaN HBT.
  - U. Mishra, was presented at International Workshop on Compound Semiconductors, Japan, October (1998)

# HBT applications in systems

- Analog and data conversion circuits
  - differential amplifiers
  - logarithmic amplifiers
  - direct-coupled wide band-width amplifiers.
- Microwave ICs
  - Low phase noise high frequency oscillators (lower  $1/f$  noise than for MESFETs)

## Digital Applications

A to D Converters

Track and hold circuits

Quantizers

Voltage comparators

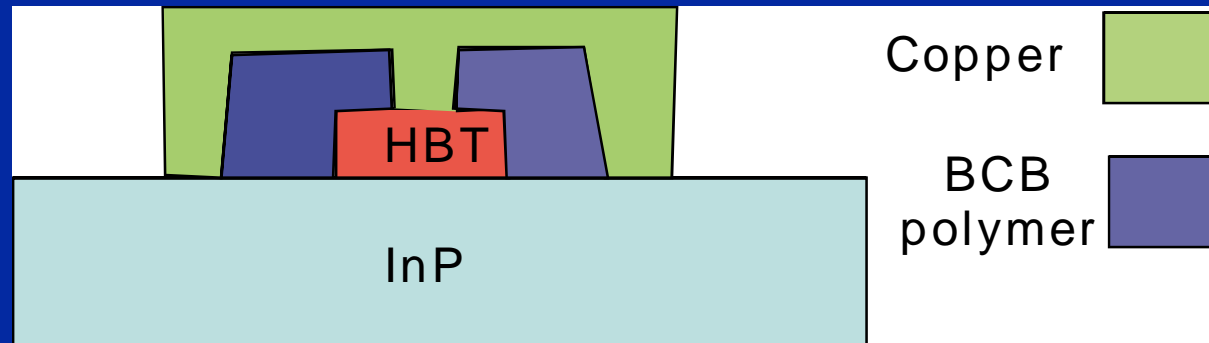
ECL/CML for optical fiber communications

HBT-diode logic

Microprocessors

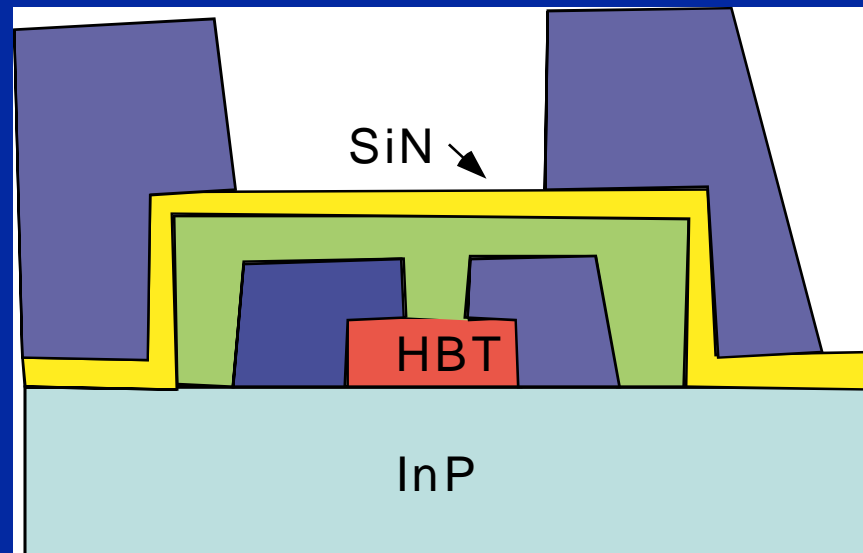
# UCSB Transferred Substrate HBT

M. Rodwell et al., 48 GHz Digital Ics Using Transferred Substrate HBTs, Proceedings of GaAs IC Symposium, p. 117 (1998)



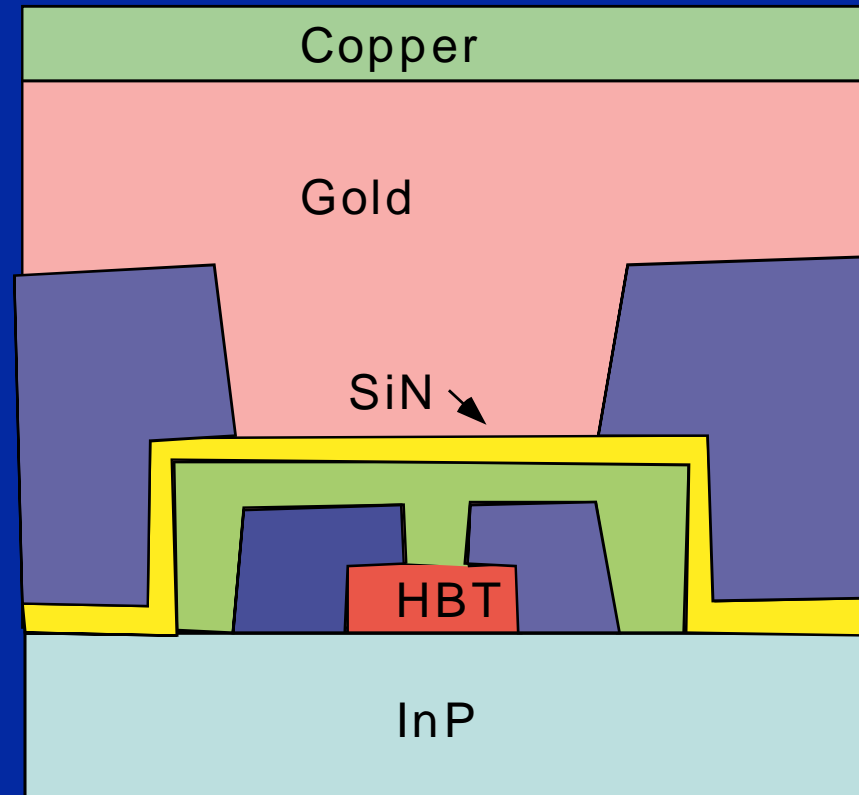
Step 1: Fabricate InP-based HBT (no collector, emitter on top)

## Step 2



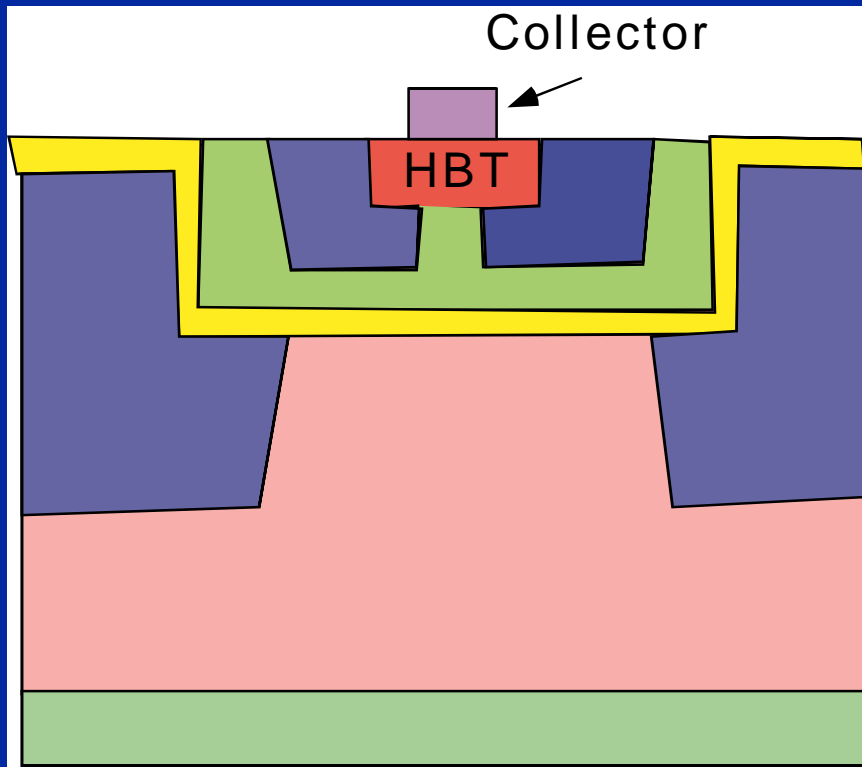
Deposit SiN insulation, coat with BCB polymer, and etch vias

# Step 3



Step 3 - electroplate gold and copper substrate

## Step 4



**Advantages:**  
**Small collector capacitance -**  
**High speed!**  
**( $f_{max}$  up to 800 GHz)**

Finish: remove InP substrate, deposit collector

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