Compound semiconductor digital integrated circuits

Device and Circuit Speed

C = Cdevice + Cinterconnect + Cfanout

fT = gm/(2πCdevice) – frequency where the short circuit current gain is unity

fTe = gm/(2πC)

gm = eps vsat W/d

Cdevice = eps WL/d

fT = vsat/(2πL)

SiGe

f_T = 124 GHz

f_{max} = 174 GHz

"Using this technology, it will now be possible to integrate high-speed HBT and 0.1 μm CMOS. This ultra-high-speed high-functional device technology is expected to play an important role in supporting next-generation information technology such as multi-media services offered by next-generation backbone transmission systems, large-capacity radio communication systems, and intelligent traffic control systems using millimeter-wave bands".

(from http://global.hitachi.com/New/cnews/E/2001/1205a/)

Noise performance

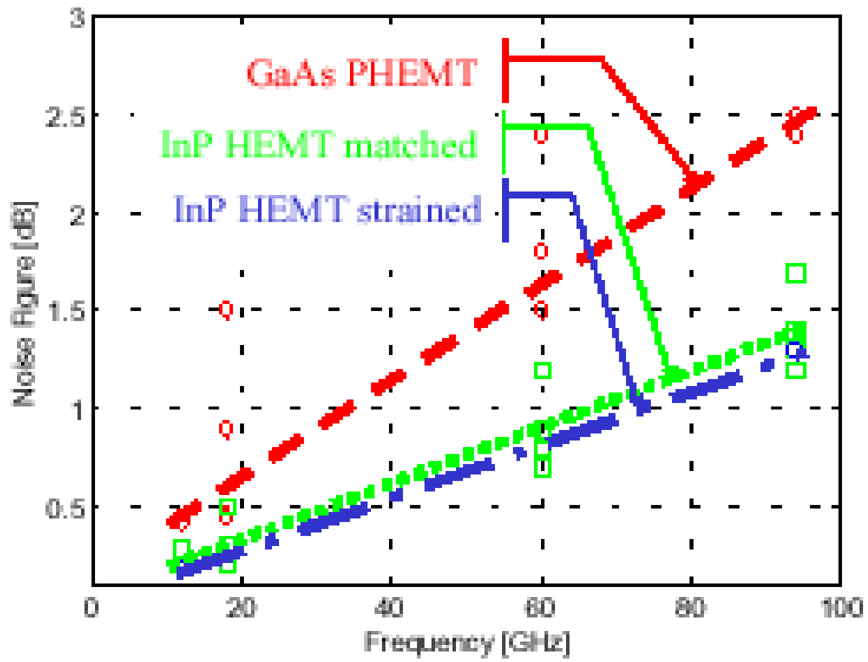


Fig. 1 Noise performance of GaAs- and InP-based HEMTs as a function of frequency

From D. Pavlidis, http://www.gaasmantech.org/digest/1999/PDF/42.pdf

Power performance

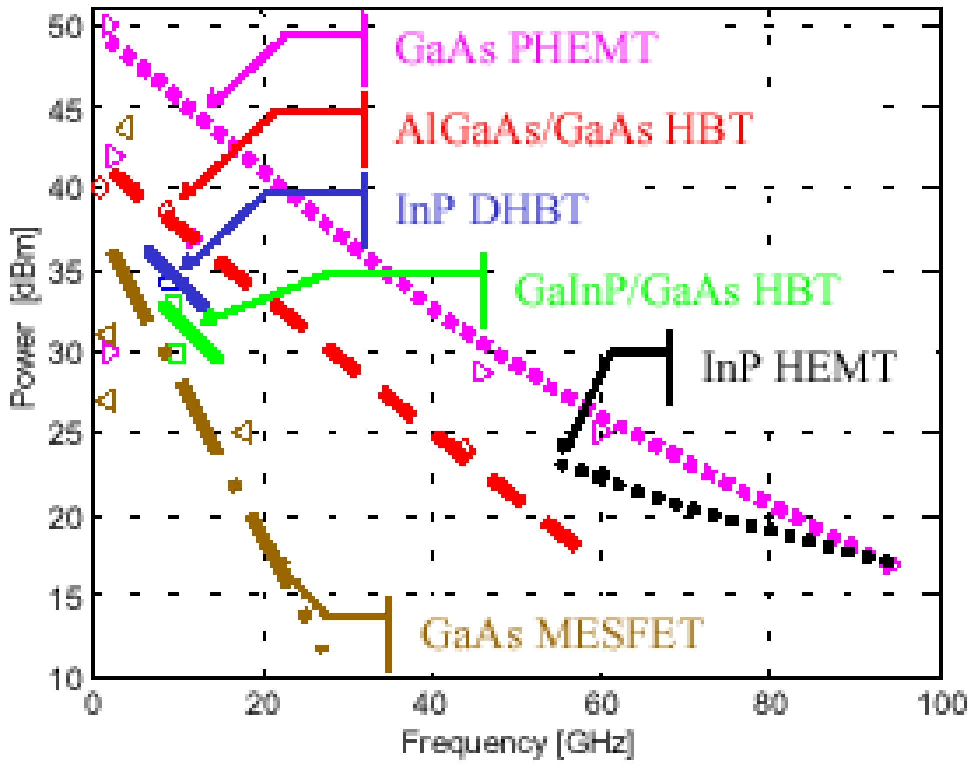
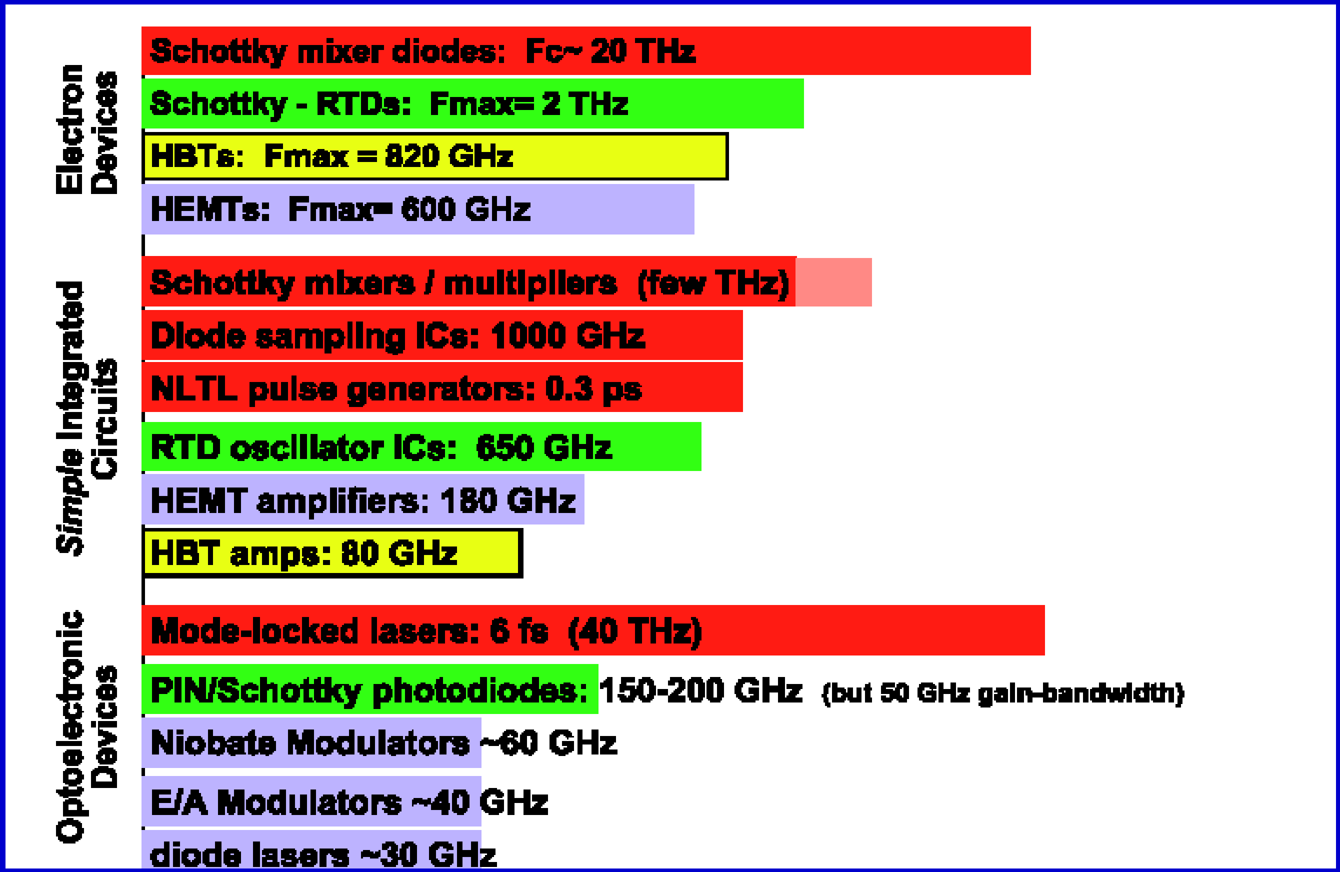


Fig. 2 Power performance of HEMTs, MESFETs and HBTs as a function of frequency.

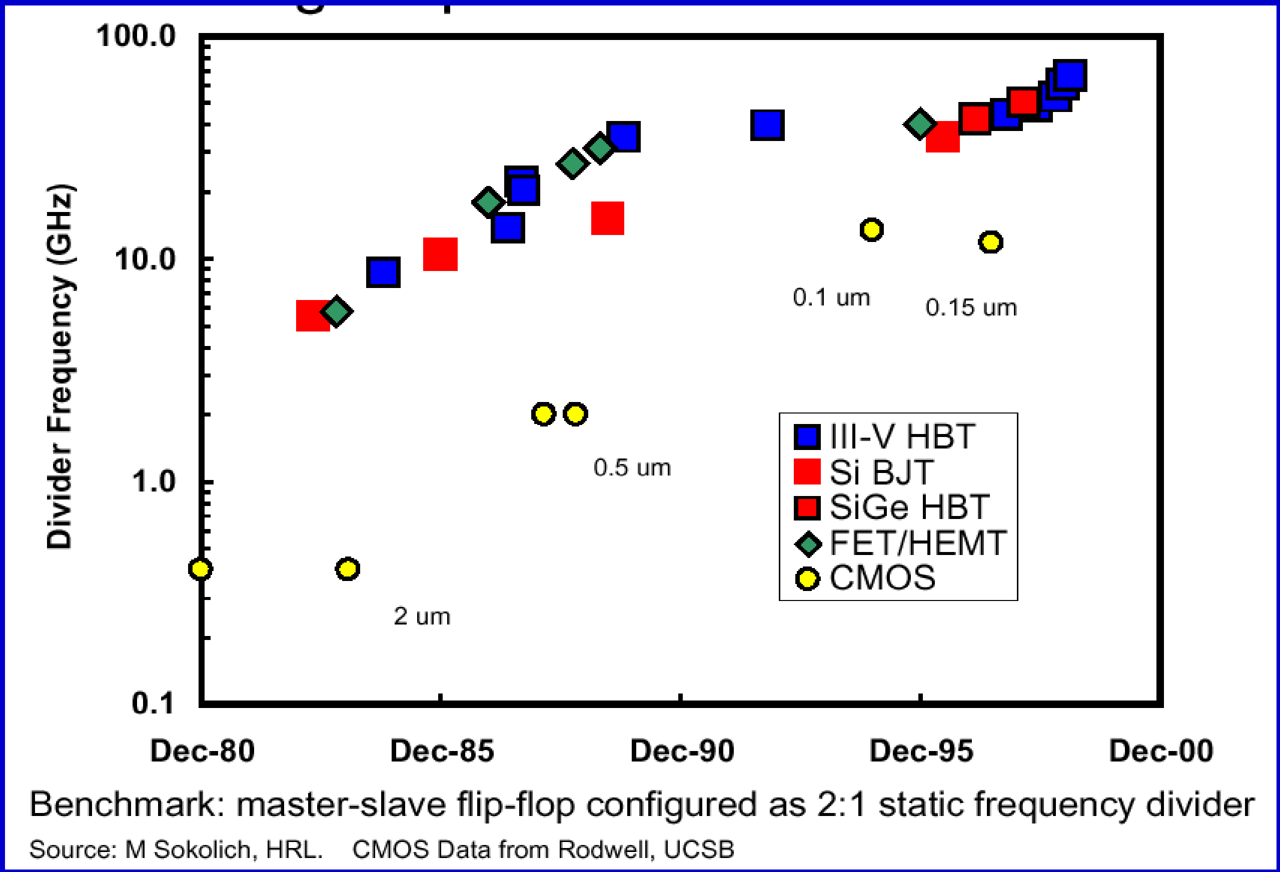
From D. Pavlidis, http://www.gaasmantech.org/digest/1999/PDF/42.pdf

High Speed according to Prof. Mark Rodwell of UCSB



From http://soliton.ucsd.edu/ihsds/santafe99/presentations/mark_rodwell.pdf

Divider Speed



From http://soliton.ucsd.edu/ihsds/santafe99/presentations/mark_rodwell.pdf

General issues in LSI and VLSI technology

on-to-off ratio

subthreshold leakage

power supplies

power dissipation

interconnects

yield

reliability

packaging.

MESFET and HFET digital technologies

Circuit families: BFL, SDFL, DCFL, CDFL, SCFL.

Complementary technology and low power circuits.

Circuit layout and design rules.

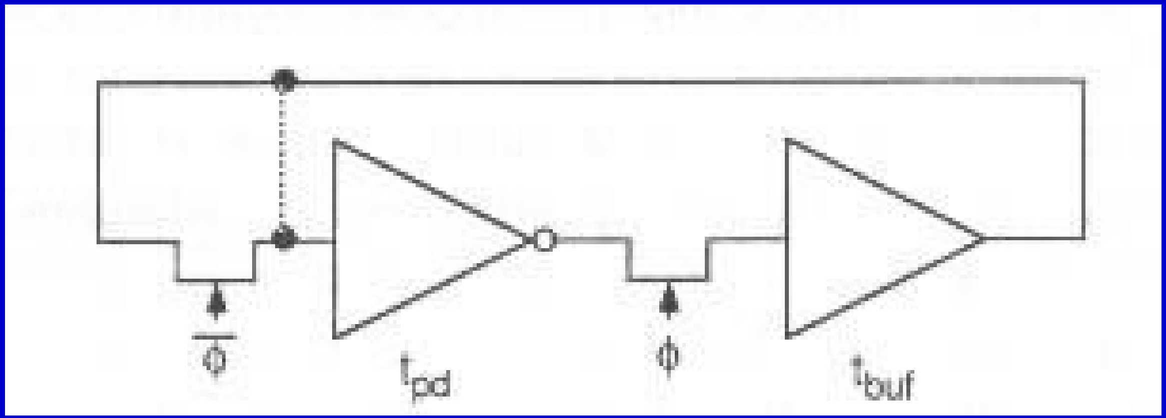
Circuit design, simulation and parameter extraction.

Overview of the state-of-the-art and comparison with ECL.

Technology bottlenecks and cost issues.

GaAs digital technology in systems.

Example of High-Speed Digital Circuits (I)

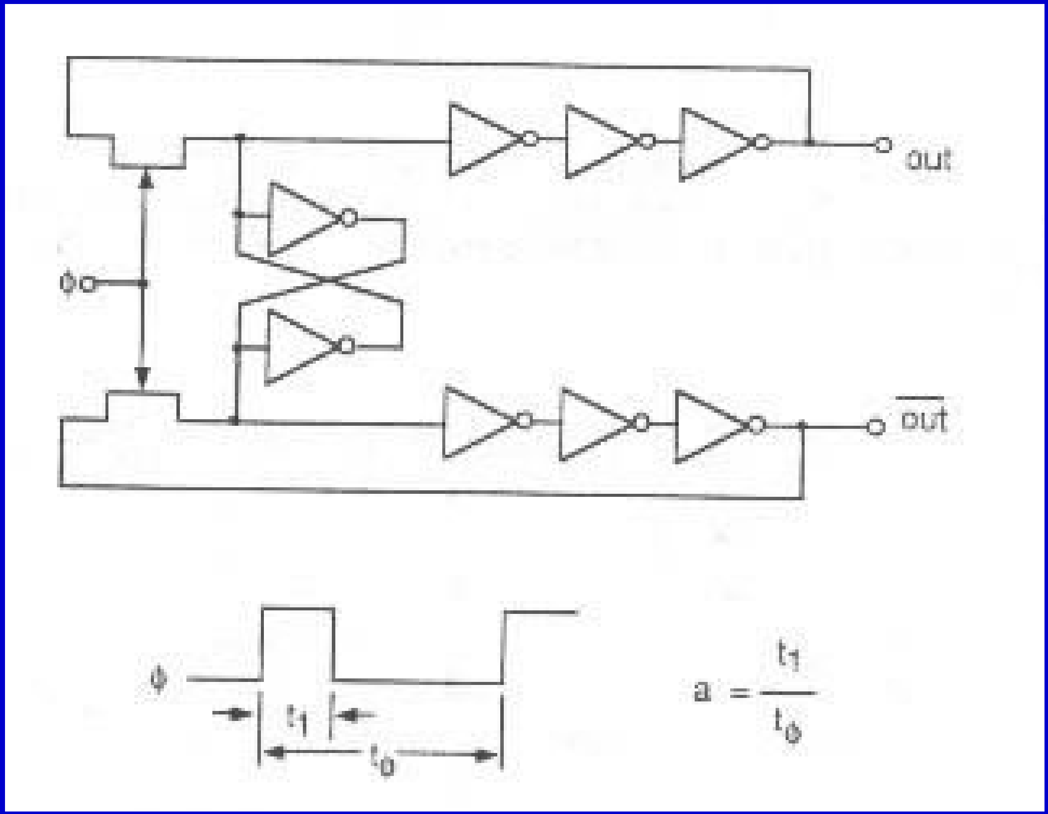


Compared with Simple diagram (dotted line): More complicated but higher stability

Disadvantage: non-overlapping two-phase clock. Difficult to provide at high operating frequencies

After S. Long, High Speed Digital Circuit Technology, in Compound Semiconductor Technology. The Age of Maturity. M. S. Shur., Editor, World Scientific, 1996,p. 268

Example of High-Speed Digital Circuits (II)



Advantage: Single phase clock

Number of inverters decide the minimum and maximum clock frequency

>50GHz reported

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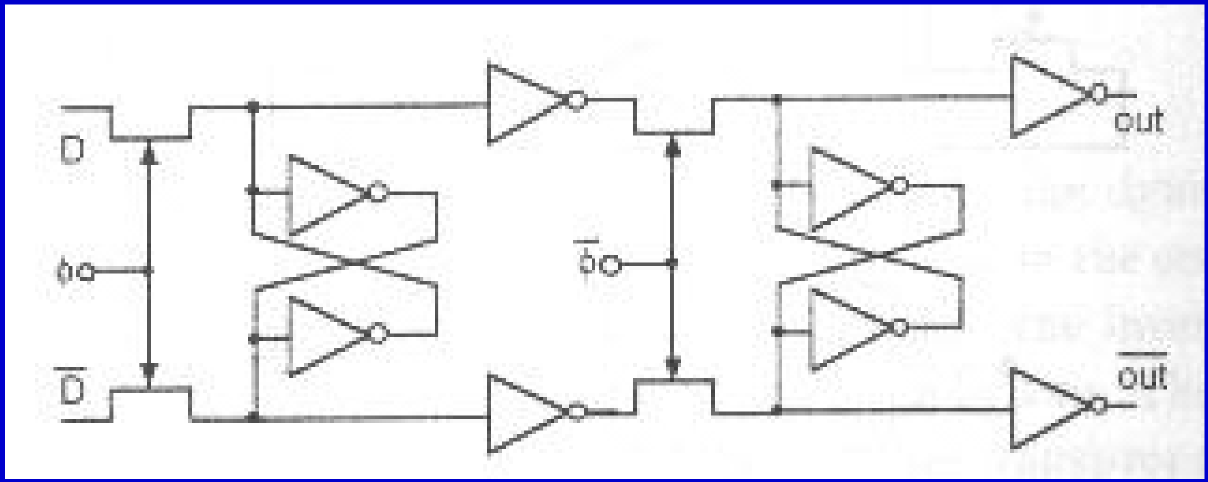
Example of High-Speed Digital Circuits (III)



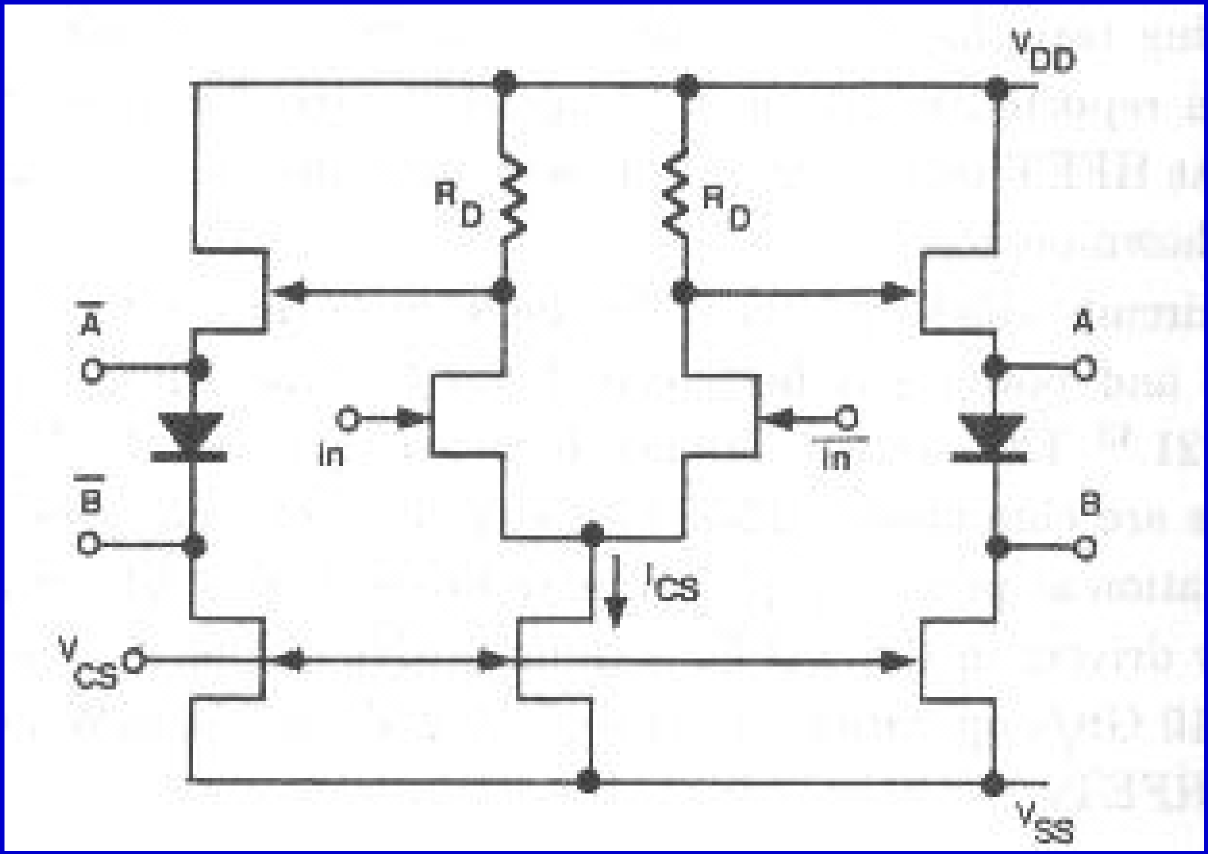
MCFF:
Memory Cell
Flip-Flop

Used as a alternative to standard D flip-flop (25GHz operation)
Lower latency (notice only 2 inverters in the critical path compared to 4 NOR gates with fan-out of 2)

After S. Long, High Speed Digital Circuit Technology, in Compound Semiconductor Technology. The Age of Maturity. M. S. Shur., Editor, World Scientific, 1996,p. 270

Logic Family (I) - SCFL

Source Coupled FET Logic



Equivalent to ECL in Bipolar logic family

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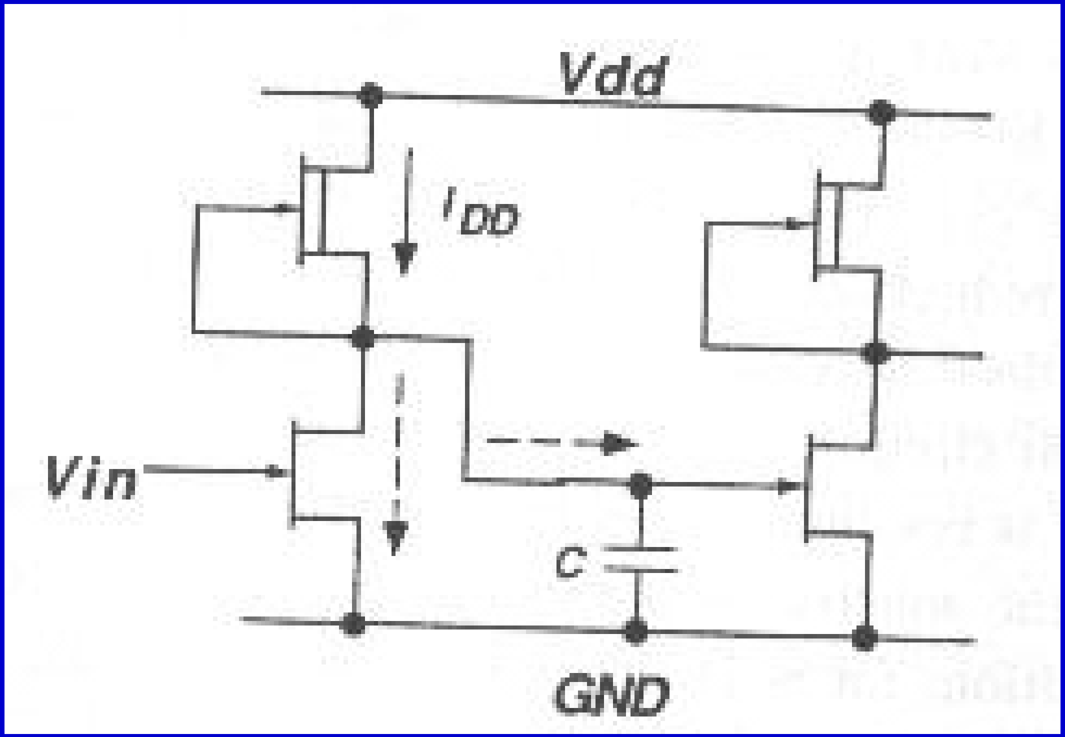
Logic Families (II) - DCFL



Direct-coupled FET logic

Static Ratioed Logic

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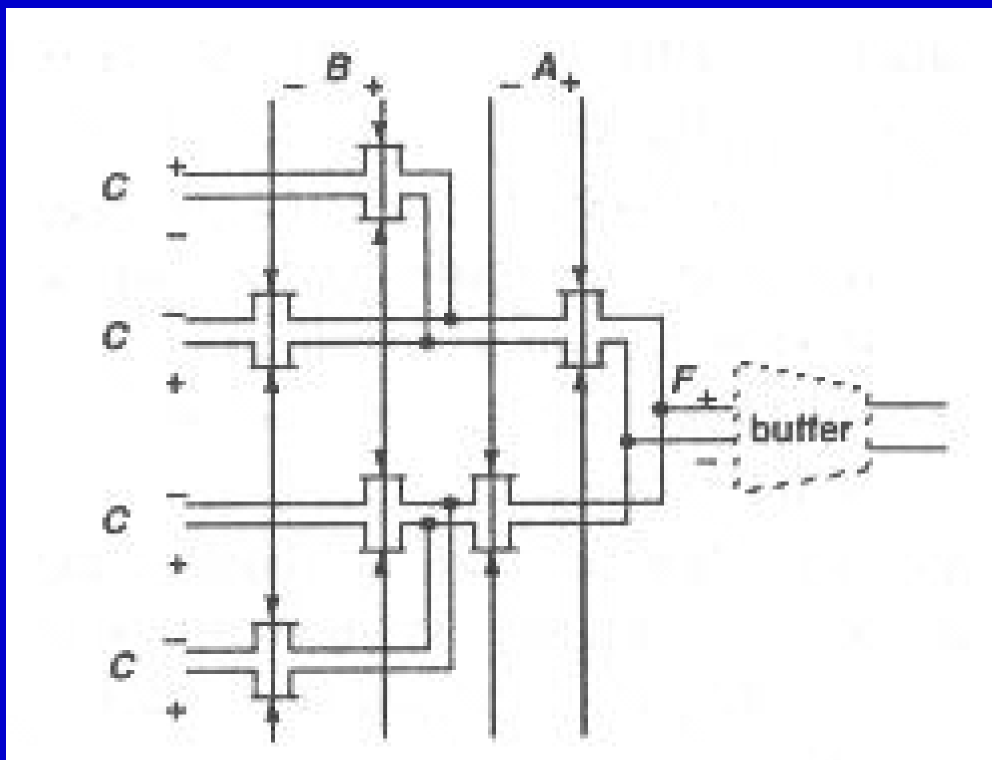
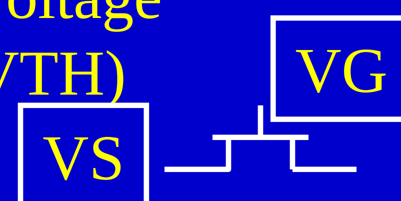
Logic Families (III) - DPTL



Differential Pass Transistor Logic

Be careful in the design: If only one type of signal is used, the logic level may suffer from a shift by the threshold voltage (VS<VG-VTH)



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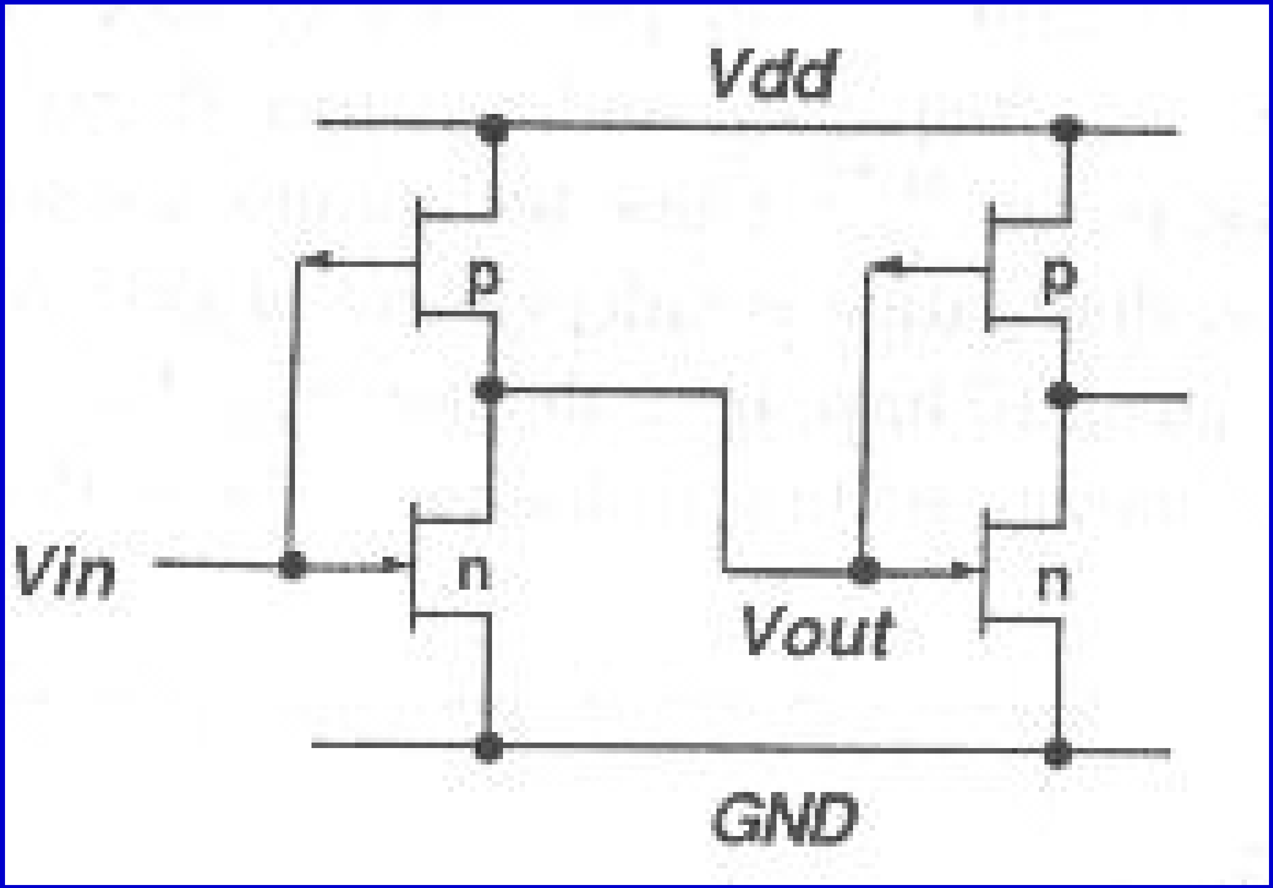
Static Non-ratioed Logic



Equivalent to CMOS Inverter

P-type transistor is usually much weaker

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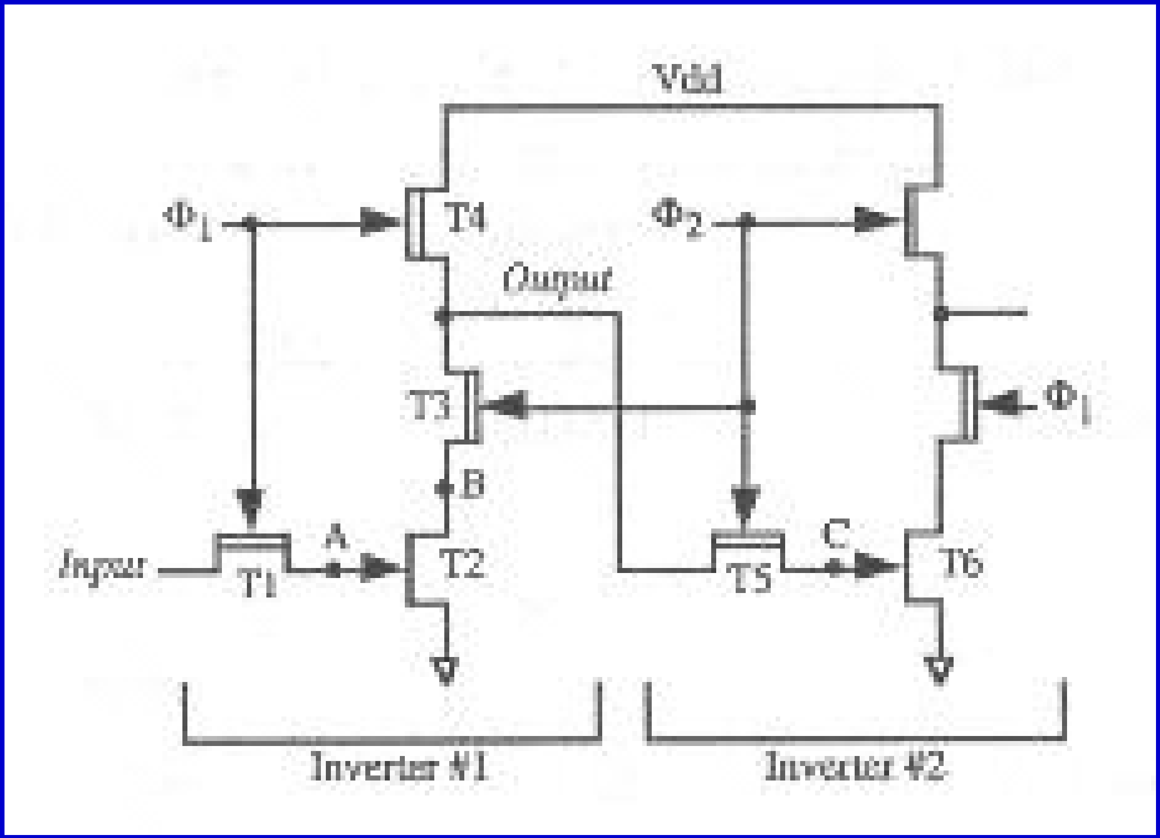
Logic Families (IV) -- TDFL



Two Phase Dynamic Logic

Precharge and Evaluate Stage

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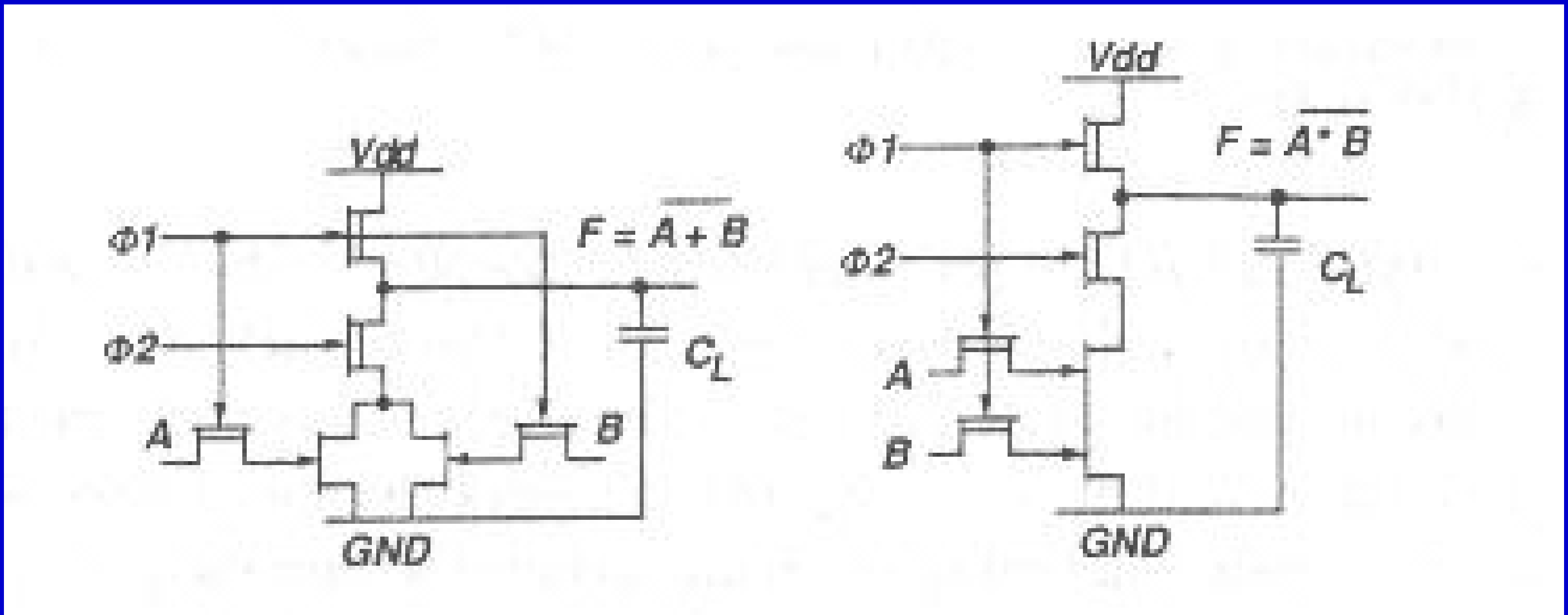
Asymmetries in TDFL



NOR gates could consumes power as much as three times than NAND gates

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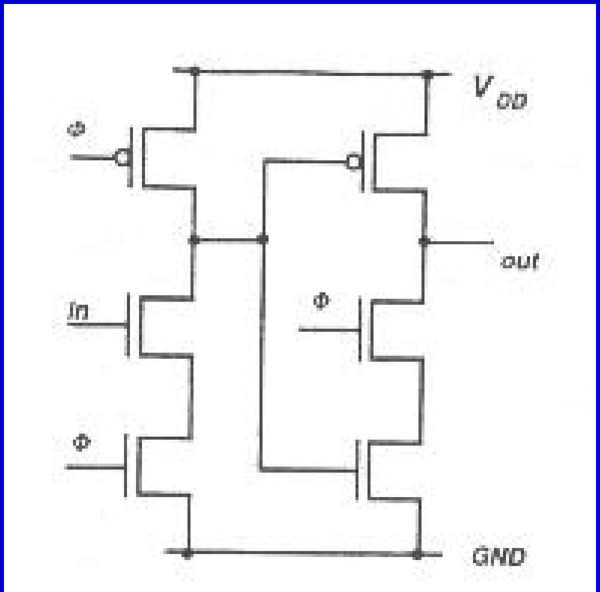
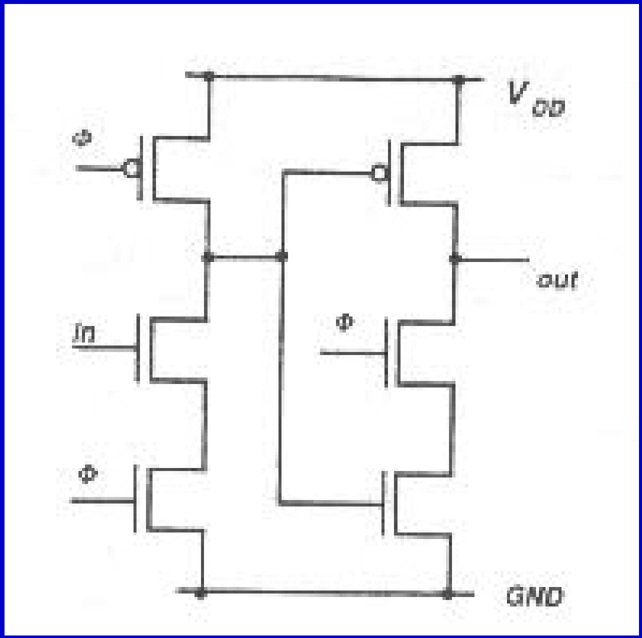
Logic Families (V) -- TSPC



N-block



P-block

True Single Phase clock CMOS logic

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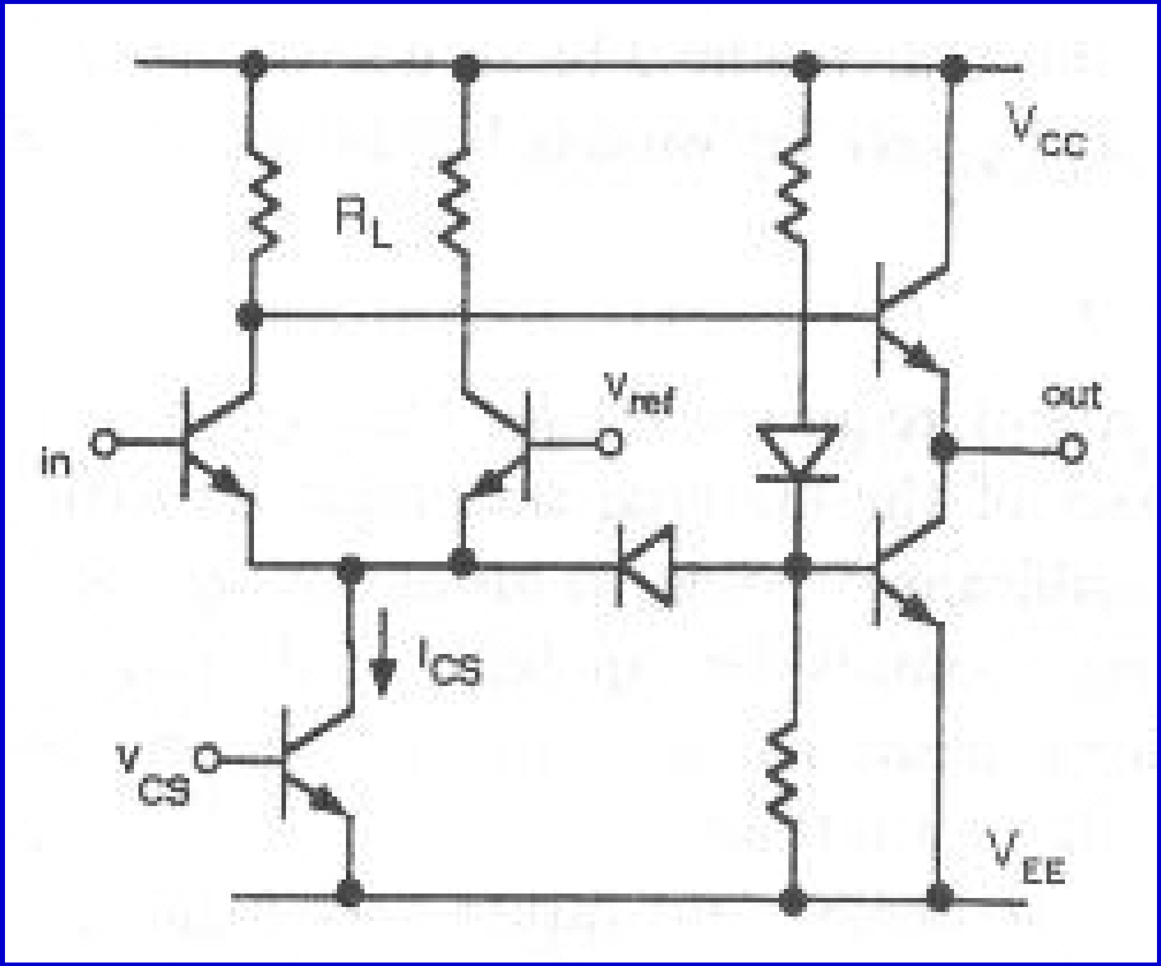
Low-Power Bipolar Logic



Charge-buffered active-pull-down ECL inverter

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Summary

Trade-off between speed and power
Power-delay products

$$I = C\frac{\Delta V}{\Delta t}$$

$$P = P_{static} + P_{dyn} = V_{DD}I_{DD} + Cf\eta\Delta V^2$$