

ABET COURSE SYLLABUS

ECSE-4770: Computer Hardware Design

Course Catalog Description: Techniques for building I/O controllers and microcomputer interfacing. Transmission line Bus Drivers. Emphasis on design of complex state machines. Implementation and testing of the designs using Field Programmable Gate arrays and FPGA support boards.. 3 credit hours.

Pre-Requisite Courses: Computer Organization and Computer Operation (ECSE-2610).

Co-Requisite Courses: None

- Prerequisites by Topic:**
1. Examination of Transmission Line Effects in Digital Systems
 2. 74 series TTL logic for small scale prototyping
 3. One Shots, Flip-flops, Hazards, Glitches
 4. CMOS vs. Bipolar, when to use each. Opto-isolators
 5. State Machine Design for large numbers of states
 6. Application to DMA channels
 7. Asynchronous vs. Synchronous Design
 8. FPGA prototyping using Altera Tools
 9. Incorporation of VHDL models
 10. VME and USB Asynchronous Buses
 11. PCI Synchronous Bus

Textbook: J. O. Hamblin, and M. D. Furman, "Rapid Prototyping of Digital Sstems –A (and/or other required material) Tutorial Approach, Kluwer. 1996

References: W. D. Peterson, "The VMEbus Handbook," VME Trade Association, 2000. T. Shandly, and D. Anderson, "PCI Architecture," Addison Wesley. 1999

Course Coordinator: John F. McDonald

Overall Educational Objective: To give students the experience of designing a complete computer or similar system, and validate it by extensive testing..

- Course Learning Outcomes:**
1. Understand the importance of interconnections in digital design, including transmission lines and terminators.
 2. Understand a basic bus structure and handshaking in data transfer.
 3. Understand architecture, data paths, arithmetic and logic units.
 4. Be able to design and debug practical state machines
 5. Prototype designs in an FPGA
 6. Test and validate simulated designs.

How Course Outcomes are Assessed:

No Homework Assignments	0%
4 Laboratory Pre-lab Designs	50-%
5 Project Proposal	50%

Relation to EE/CSE/EPE Outcomes

N = none
M = moderate
H = high

Outcome	Level	Demonstrate Proficiency
	N, M, H	e.g. Exams, projects, HW
Mathematics, science and engineering	M	Reports
Basic disciplines in Electrical Engineering	N	
Depth in Electrical Engineering	H	Reports
Basic disciplines in Computer & Sys. Eng.	N	Reports
Depth in Computer and Systems Eng.	H	Testing and debugging
Electromagnetics, electromechanics, power semiconductors	N	

Power system behavior	N	
Electrical energy conversion	N	
Conduct experiments and interpret data	H	Testing
Identify, formulate and solve problems	H	Debugging
Design a system, component or process	M	Complete Working Computer Interfaces
Communicate in written and oral form	M	Presentations, Reports
Function as part of a multi-disciplinary team	M	Teams of 3 to 4
Preparation for life-long learning	M	Must make it work
Ethical issues; safety, health, public welfare	N	
Humanities and social sciences	N	
Laboratory equipment and software tools	H	Labs
Variety of instruction formats	N	

**Topics Covered:
(number of hours or classes for each)**

1. Review of Transmission Line Wave Equation (2)
2. Termination vs. NonTermination of Transmission Lines (2)
3. Approaches to Coupling (2)
4. TTL OC drivers, Simultaneous Switching Noise (1)
5. ECL and CML full differential designs (1)
6. Richard's Controller State Machine (2)
7. DMA Channel State Machine (2)
8. Tutorial on FPG's (evening 2)
9. Asynchronous and Synchronous Design Tradeoffs (1)
10. Handshake Based Data Exchange and the VME bus (3)
11. Interrupt Handling, Stacks and Stack Pointers (1)
12. Serializers, Phase Locked Loop DES (2)
13. UART(1)
14. Optoisolators and optical modulators (1)
15. PCI vs. USB (4)

Computer Usage:

Students use Altera and/or Xilinx CAD tools

Laboratory Experiences:

1. Explore Transmission Line Effects, Terminators, Reflections, Coupling, Switching Noise in a Lab Setting
2. Build a large State Engine in 74 series on protoboard
3. Rebuild (2) as a 74 series library entry for Altera FPGA and compare
4. UART design on protoboard, including optoisolators
5. Rebuild (4) using VHDL in an FPGA

Design Experiences:

1. Three Hours a Week with TA supervision..

Independent Learning Experiences:

1. Laboratory projects require independent learning of different instruments used in the lab and characteristics of different passive and active components

Class/Lab Schedule:

3 lecture hours weekly for first 13 weeks of course, 3 hours of lab weekly..

**Contribution to the
Professional Component:**

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| (a) College-level mathematics and basic sciences | 0 credit hours |
| (b) Engineering Topics (Science and/or Design): | 3 credit hours |
| (c) General Education: | 0 credit hours |

Prepared by:	John F. McDonald
Date:	April 10, 2006