A Low-Power Dual-Band Oscillator Based on Band-Limited Negative Resistance

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***Abstract*—This paper presents a 2.1/3.9 GHz oscillator based on switching the negative resistance bandwidth of a capacitively degenerated common collector stage, while using a high order resonance tank. Multi-band oscillators have traditionally been implemented by reconfiguring the oscillator tank. In this paper, we employ a fixed high order resonator, and move the band-switching mechanism from the tank to the loss compensation network (i.e. negative resistance network), thus maintaining the high quality factor of the tank at multiple oscillation frequencies. The proposed oscillator is implemented in a 30GHz f_T GaAs process with V_{BE}=1.3V. The measured phase noise for both bands is -136dBc/Hz at 1MHz with a power consumption of 5.1mW, and a FOM of -195.39dBc/Hz and -200.72dBc/Hz for 2.1 and 3.9GHz respectively.**

I. Introduction

Dual band oscillators have been traditionally realized by reconfiguring the frequency selective network [1]-[3]. Typically, a cross-coupled negative resistance cell is combined with a switch-controlled resonator as shown Fig. 1. Switched resonators are used to change the LC constant, and thus the oscillation frequency either by connecting an inductor or a capacitor via a switch transistor to the main tank (Fig. 1a). However, because of the limited channel resistance of the switch, the tank Q is degraded up to 30%[1]. Another technique involves the use of a transformer whose primary winding is connected to the main tank while the secondary winding is connected in parallel to a transistor (Fig. 1b) [4]. The transistor acts as a voltage controlled resistor or an ON/OFF switch, thus the effective inductance seen in the primary winding is varied. However, this technique also suffers from the loss over the switch as a portion of the energy pumped into the tank is dissipated over the switch, degrading the quality factor of the tank. Another transformer based technique for multi-band oscillator uses the direction and/or the ratio of primary and secondary winding currents for band switching and/or in-band tuning purposes (Fig. 1c) [5]. Although this technique does not employ any switch directly connected to the tank, due to the opposite directions of the primary and secondary currents at high band, the effective Q of the tank is degraded.

The common feature of all prior techniques for multi-band oscillators is reconfiguring the resonator, which would consequently affect the tank quality factor. In this paper, we employ a *fixed* high order resonator, and move the band-switching mechanism from the tank to the loss compensation network (i.e. negative resistance network), thus maintaining the high quality factor of the tank at multiple oscillation frequencies. By moving the band switching mechanism to the active core of the oscillator, the overall performance can be simultaneously optimized for multiple frequency bands.

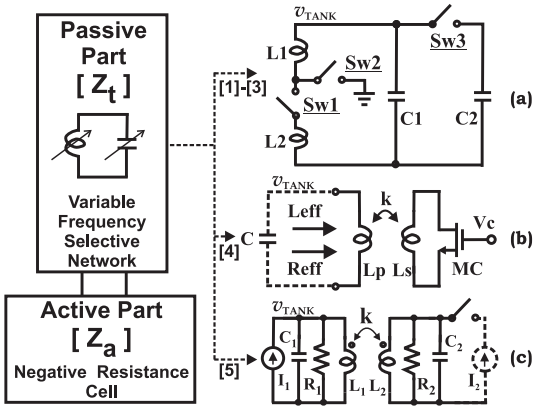

Fig. 1. Typical Implementations of multi-band oscillators, a) switched resonator, b) changing the effective inductance using resistive tuning, c) band-switching current driven double-tuned transformer.

II. Basic Concept

In a two-port oscillator, the frequency selective network or passive part (Z_t) determines the generated frequency depending on the resonance frequency of the network, while the active core of the circuit (Z_a) provides *enough* negative resistance at this resonance frequency to compensate for the loss of the tank. Fig. 2 explains conceptually the proposed dual-band operation technique using switchable negative resistance bandwidth. In this plot, we assume the oscillator's passive part is formed of a double-resonance network. The double resonance network can be implemented as a double-tuned transformer or a simple 4th order resonator. The resonance frequencies (ω_L and ω_H) has a corresponding parallel loss resistances in the resonator (Z_{tL} and Z_{tH}) as shown in the figure. When using an active core that provides a broadband negative resistance such as a cross-coupled negative resistance cell, the oscillator will either oscillate at one band or provide concurrent oscillations depending on the level of the negative resistance compared to both Z_{tL} and Z_{tH}. In our proposed approach, for band-switching without the possibility of concurrent oscillations, the active core of the oscillator has to provide an effective

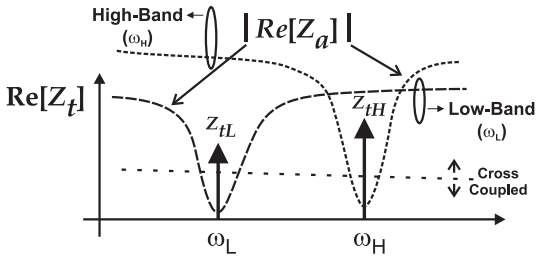

Fig. 2. Oscillation condition for dual-band band-switching operation

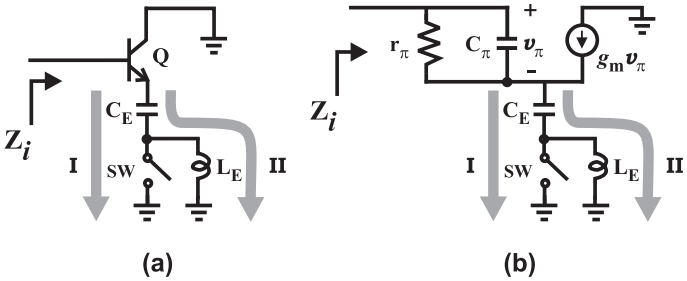

Fig. 3. a) Switch controlled band-limited negative resistance cell b) The equivalent circuit

negative resistance within a limited bandwidth around the targeted oscillation frequency as shown in Fig. 2. If oscillation is required at ω_L, the negative resistance characteristic can be shaped as the low-band characteristic shown in Fig. 2. This characteristic provides enough negative resistance at ω_L to compensate for the loss of the tank, while its *skirt* is well above the parallel equivalent loss resistance of the tank at ω_H failing to start the oscillation at this frequency. A similar scenario occurs at high-band operation.

A. Realization of Band-Limited Negative Resistance

To realize the band-limited negative resistance cell discussed above, let us consider Fig. 3a. If the switch SW is closed and the bottom plate of C_E is connected to ground, the current follows in *path I* as shown in Fig. 3a. Considering the equivalent circuit given in Fig. 3b and ignoring all other parasitic capacitances and base resistance of the transistor, the parallel equivalent negative resistance of the circuit, Ri, can be given as:

$$Ri = \frac{1}{\mathrm{Re}\{Y_i(\omega)\}} = \frac{(1+\beta)^2 g_m^2 r_\pi + \beta^2 (C_E + C_\pi)^2 \omega^2}{\omega^2 \beta g_m C_E (C_E - \beta C_\pi)} \tag{5}$$

Considering the denominator of (5), as long as the following condition is met, the input of the circuit exhibits a negative resistance

$$C_E < \beta C_\pi. \tag{6}$$

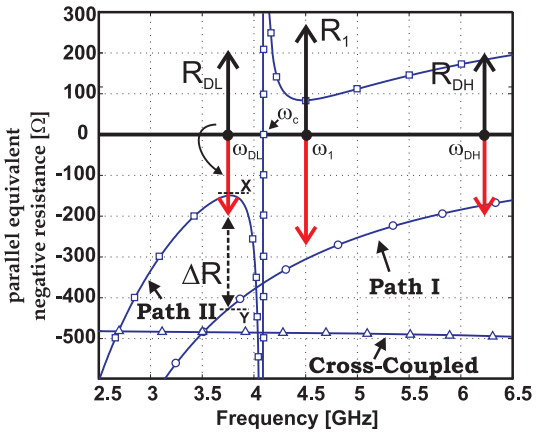

Fig. 4. Comparison of negative resistance characteristics and band-switching mechanism

If we assume that β is constant over the frequency range of interest, for a given βC_π, the negative resistance condition is only controlled by an *externally* connected C_E. Also, once the negative resistance condition is met, the resistance remains negative as frequency increases. Thus the circuit exhibits a broadband negative resistance behavior as shown in Fig. 4. This behavior is similar to a typical cross-coupled stage, with the later providing a flatter response over frequency. Thus, the fixed value of C_E can only make the input impedance either positive or negative without controlling its negative resistance bandwidth. By re-examining equations (1) and (2), a frequency dependent capacitor can limit the negative resistance bandwidth as its value changes with frequency. To build a frequency dependent capacitor, we consider the input impedance of a series LC network;

$$Z_E = \frac{1}{j\omega \underbrace{\left(\frac{C}{1-\omega^2 LC}\right)}_{C_{eff}}} = \frac{1}{j\omega C_{eff}} \tag{7}$$

Replacing C_E with Z_E network, we reach the topology shown in Fig. 3 for *path II*. For this topology, the parallel equivalent of the negative input resistance, Ri can be given as in (4). The effective negative resistance condition can be found from the nominator of (4) as given by;

$$C_E < \beta C_P \chi = \beta C_P \underbrace{\left[1 + \left(\frac{\omega}{\omega_e}\right)^2\right]}_{\chi} \tag{8}$$

where ω is operation frequency and ω_e is the resonance frequency of C_E and L_E. In this case, the denominator of the negative resistance equation has another term that can change the sign of resistance at a certain cut-off frequency ω_c, thus limiting the negative resistance bandwidth. In addition, the

$$Ri = \frac{(1+\beta)^2 gm^2 (1 - C_E L_E \omega^2)^2 + \beta^2 \omega^2 (C_E + C_\pi - C_E C_\pi L_E \omega^2)^2}{\beta C_E gm \omega^2 (C_E - \beta C_\pi + \beta C_E C_\pi L_E \omega^2)} \tag{4}$$

introduction of the emitter inductance through path II increases the effective capacitance between the emitter and ground by a factor of 1/(1-ωLC) compared to C_E, thus providing a higher negative resistance as shown at *point X* in Fig. 4 compared to its original value at *point Y*. This feature will enable the band switching mechanism as will be discussed in the next subsection.

It is worth noting that while the above analysis has been done using a bipolar device, it can be readily extended to a CMOS technology.

B. Band-switching

In this section, we assume that a high order resonator is employed as a fixed oscillator tank. For simplicity, we will use a double resonance network with effective parallel resistive loss R_{DL} in the low band, and R_{DH} in the high band. Fig. 4 shows the interaction between loss-compensation network (i.e. effective negative resistance R_i) and the resonator for possible band-switching. In this plot, the parallel loss resistances of a double resonance network (R_{DL} and R_{DH}) are drawn and mirrored to study oscillation start-up conditions. If the SW in Fig. 3 is closed and path I is enabled, the circuit fails to oscillate at low-band, ω_{DL}, since it requires at least —ΔR— less negative resistance to start the oscillation. On the other hand, when the SW is closed, path I provides enough negative resistance at high band, ω_{DH}, and oscillation starts. Similarly, when the SW is left open, path II is enabled, and circuit provides enough negative resistance to start the oscillation at ω_{DL}. However, since the circuit exhibits always positive effective resistance beyond ω_c, it can't trigger any oscillation at high band, ω_{DH}. Thus, if the frequency selective network is designed properly, changing the configuration of negative resistance cell, the oscillation band can be changed and this mechanism provides an oscillation only and only at one band at a time. Note that, even if the tank has a parasitic resonance frequency between ω_{DL} and ω_{DH} as the example case of ω_1, neither path I nor path II configuration can start an oscillation at ω_1 because of the lack of enough negative resistance at this frequency.

III. Circuit Design

The transistor level schematic of the dual-band oscillator is shown in Fig. 5. The double resonance network is formed using a 4th order resonator, which is connected in parallel to the negative resistance cell. Since this is a bipolar design, the input capacitance of the active part is substantial and should considered as part of $C1^*$. The transistors $Q1p$ and $Q1n$ are biased through the resonator network. A bias resistance Rg is connected between the common node of the resonator and bias source to avoid even mode oscillation. Z_E network is formed by C_E and L_E and path I/II configuration is controlled by the gate voltage of switch transistor M_{sw}. For differential operation, the AC ground is created at the common node of the switches and is shown by gray ground symbol in the figure.

The lowest supply voltage is limited by the relatively high V_{BE} voltage of the transistors provided in the technology. The

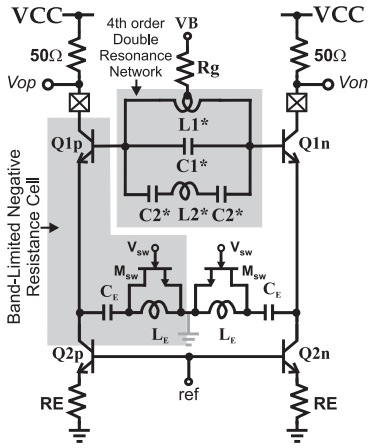

Fig. 5. Transistor level schematic of the dual-band oscillator

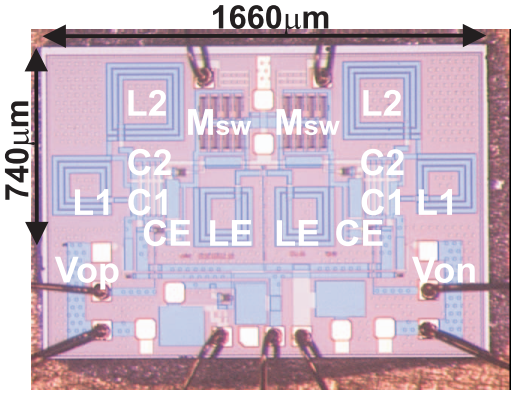

Fig. 6. The die photo of the dual-band oscillator

typical V_{BE} voltage of the GaAs process used is around 1.3V, while the same voltage is 0.9V for a SiGe bipolar process and 0.6∼0.7V for silicon bipolar processes. Despite the high V_{BE} voltage, the supply voltage could be lowered down to 1.7V while maintaining competitive performance parameters.

IV. Experimental Results

The dual-band VCO is implemented in RFMD three-metal GaAs BiFET-1 technology. The micrograph of the fabricated oscillator is shown in Fig. 6. The chip is mounted on an FR-4 board and measured in screened-room. Agilent E5052A signal source analyzer is used for phase noise measurements. The oscllator has no additional buffer, the negative resistance transistors have open collectors with one of the collector terminals connected to an off-chip bias-T and 50 ohms combination, while the other is terminated with off-chip bias-T and connected to a E5052A signal source analyzer. The oscillator is characterized for several bias and supply voltage conditions at low-band and high-band. The oscillator is functional down to 1.7V VCC, however the bias current range is relatively limited under such a low supply voltage. The measured phase noise for low-band is -136.03 dBc/Hz at a 1-MHz offset from a 2.10-GHz carrier with a power consumption of 5.1mW and -13.12dBm output power. For the high-band, the phase noise is -135.98 dBc/Hz at a 1-MHz offset from a 3.89-GHz carrier with a power consumption of 5.1mW and -

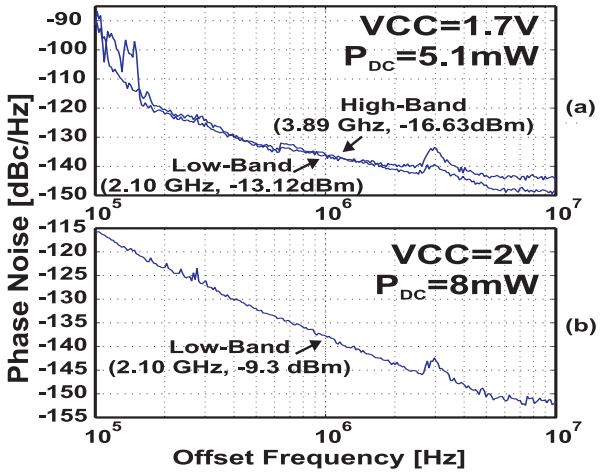

Fig. 7. Measured phase noise at low-band and high-band

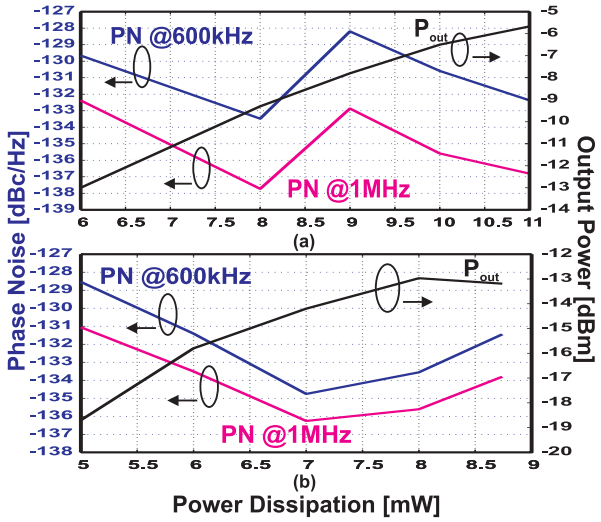

Fig. 8. Measured phase noise and output power as a function of power consumption at low-band and high-band

16.63dBm output power as shown in Fig. 7. The oscillator is also characterized under 2V VCC for a wider range of bias current. The performance of the oscillator is given for low and high band as a function of power consumption in Fig. 8a and b, respectively. For the power consumption from 5mW to 9mW, the phase noise has a valley shape characteristic. Interestingly, the best phase noise performance is obtained almost at the same power consumption (7∼8mW) for low and high-band. Thus, the topology can be optimized for both bands simultaneously without requiring a bias current adjustment after band switching. This feature can improve band switching time in a PLL application and simplify the oscillator bias control circuitry.

Table I compares the performance of the proposed oscillator with the state-of-the-art dual-band oscillators. From table I, the designed oscillator provides the highest FOM at high-band, as well as a competitive performance at low band. It is worth noting that a number of factors should be considered for a fair comparison. Since the process used does not have any varactors, the designed oscillator does not suffer from any

TABLE I
COMPARISON BETWEEN DUAL-BAND STATE-OF-THE-ART OSCILLATORS

Ref.	Tech.	f $[GHz]$	P_{DC} $[mW]$	Phase Noise $[dBc/Hz]$	FOM $[dBc/Hz]$
This Work	**GaAs pHEMT**	**2.1 3.9**	**5.1 5.1**	**-136.03@1MHz -135.98@1MHz**	**-195.39 -200.72**
[6]	0.18 μm SiGe	6 9	19.44 19.44	-106@1MHz -109@1MHz	-177 -178
[1]	0.18 μm CMOS	0.865 1.812	16 16	-125@0.6MHz -123@0.6MHz	-176 -181
[3]	0.25 μm CMOS	1 2	10.5 13.5	-138@3MHz -132@3MHz	-178 -177
[2]	0.18 μm CMOS	2.42 5.01	4.6 6	-134@1MHz -125@1MHz	-195 -192
[7]	InGaP/ GaAs	13 22	88 64	-108@1MHz -106@1MHz	-176 -175
[5]	0.25 μm CMOS	1.94 3.6	3.24 17.1	-120@1MHz -112@1MHz	-180 -170

phase noise degradation that may originate from the varactor. Additionally, a GaAs process has an obvious advantage over CMOS processes in terms of substrate loss and device noise. On the other hand, the design suffers from a very high V_{BE} voltage (1.3V) and relatively low f_T (30 GHz) with respect to those of CMOS and silicon bipolar processes.

V. CONCLUSION

The capability of band-limited negative resistance, provided by capacitively degenerated common collector stages, is exploited in this work for the design of a dual-band oscillator. Moving the band switching mechanism from the tank to the active core, allowed the simultaneous optimization of phase noise performance at the two frequency bands. The measurement results from the oscillator implemented in a 30GHz f_T GaAs prototype validate the concept with 2.1/3.9GHz operation, -136dBc/Hz @ 1MHz for both frequencies, power consumption of 5.1mW, and one of the highest reported FOM of -200.7dBc/Hz for the 3.9GHz band.

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