A Highly Efficient Interleaved DC-DC Converter using Coupled Inductors in GaAs Technology

Han Peng, T. P. Chow, and Mona Hella
Rensselaer Polytechnic Institute, ECSE Department, 110 8th Street, Troy, NY 12180, USA.
Email:pengh2,chowt,hellam@rpi.edu

***Abstract*—This paper presents a high power efficiency DC-DC buck converter in Gallium Arsenide technology targeting integrated power amplifier modules. The buck converter adopts an interleaved structure with negatively coupled inductors. Analysis of the effect of coupling on the steady state and transient response of the converter is given. The coupling factor is selected to achieve a maximum power efficiency for a given duty cycle with a minimum penalty on current ripple performance. The DC-DC converter is implemented in 0.5μm GaAs pHEMT process and occupies 2.7x2.7mm^2 without the output network. It converts 4.5V input to 3.3V output for 1A load current under 250MHz switching frequency with a power efficiency of 86.1% .**

I. Introduction

While silicon-based technologies have driven the wireless transceiver market in the last decade, III-V technologies, and particularly GaAs dominate the current landscape of handset power amplifiers. Several requirements, such as decreasing battery voltages (end of life and/or nominal voltages) and improved performance at low and mid-range power levels present challenges for power amplifiers in general [1]. DC-DC converters are a possible solution to both requirements, changing the voltage that the power amplifier sees at various output power settings to maintain efficiency or keeping current levels at permissible values to avoid device failures.

On-chip integrated DC-DC converters have been the subject of active research, particularly in CMOS technology [2-6] with emphasis on low current ratings (mA range), and low switching frequency. Power amplifiers require currents in the amps range and minimum interconnect losses between the PA module and the DC-DC converter module. Thus, GaAs technology is regarded as an optimum technology choice for DC-DC converters targeting power amplifiers as they can both be integrated on the same die. In addition, GaAs technology has notably higher electron mobility, allows higher breakdown voltage, and better quality passives [7]. These advantages would translate to higher switching frequency (>100MHz) and improved power efficiency.

This paper presents an interleaved DC-DC converter in GaAs 0.5μm pHEMT technology with negative coupling between the two phases. The paper is organized as follows; Section II describes the core structure of interleaved topology and the selection of coupling factor for both steady state and transient considerations. Section III presents the circuit design, including main switching device, and gate driver circuitry. Circuit characterization is given in section IV, while conclusions are drawn in Section V.

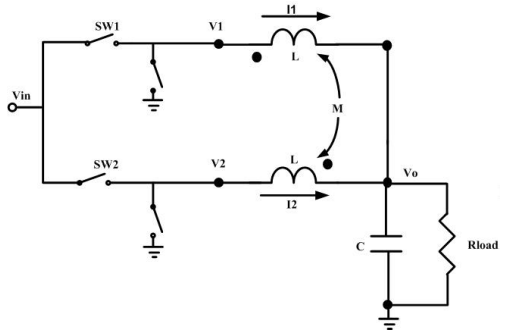

Fig. 1. Ideal interleaved topology with negative coupling

II. Interleaved DC-DC Converter with Negative Coupling

As mentioned earlier, high efficiency DC-DC converters supplying the power amplifier, which dominates the current consumption in any mobile terminal, will significantly improve the battery run-time. However, existing DC-DC converters operate at frequencies in the lower MHz range, and require external filter capacitors larger than 1μF and filter inductors higher than 1μH [5]. This impacts the system size and weight, which are critical factors in the commercial viability of mobile terminals. Interleaved DC-DC converters have been utilized to reduce the values of filter inductors by more than 50%. In this section, we examine the effect of adding negative coupling between the inductors in the interleaved structure on the steady-state and transient response of the DC-DC converter.

Fig. 1 illustrates the core interleaved structure with coupled inductors. M is the mutual inductance between the two phases. Here, we assume that the two branches have the same inductance L and $k = M/L$ is the coupling factor. The current and voltage waveforms at the input and output of the DC-DC converter for each phase, assuming ideal switching stages, are shown in Fig. 2 for a duty cycle higher than 0.5. From Fig. 2, we can see that there are four different states for V_1 and V_2. For states (i) and (iii), V_1=V_2=V_{in} and both switches SW1 and SW2 are on. For state (ii), V_1=V_{in}, V_2=0, switch SW1 is on, and switch SW2 is off. For state (iv), V_1=0, V_2=V_{in}, switch SW2 is on, and switch SW1 is off. In general, the voltages across the inductors (V_1, V_2) can be expressed as:

$$V_1 - V_0 = L\frac{\partial i_1}{\partial t} - M\frac{\partial i_2}{\partial t} \quad (1)$$

978-1-4244-3828-0/09/$25.00 ©2009 IEEE

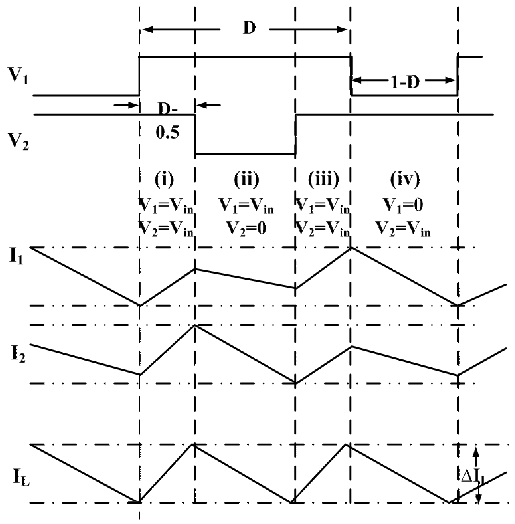

Fig. 2. Voltage and current waveforms at the terminals of the coupled inductors

$$V_2 - V_0 = L\frac{\partial i_2}{\partial t} - M\frac{\partial i_1}{\partial t} \tag{2}$$

For a symmetrical structure, the relation between the current ripple $\frac{\partial i_1}{\partial t}$ and the coupling factor k can be given as:

$$\frac{\partial i_1}{\partial t} = \frac{(V_1 - V_0) + k(V_2 - V_0)}{L(1-k^2)} \tag{3}$$

The value of the effective inductance in each phase and the resulting current ripple depend on the operating state. In (i) and (iii), both V_1 and V_2 are equal to V_{in}, Thus the current ripple can be expressed as;

$$\frac{\Delta i_1}{\Delta t} = \frac{V_{in}(1-D) + kV_{in}(1-D)}{L(1-k^2)} = \frac{V_{in}(1-D)}{L(1-k)} \tag{4}$$

As k is selected between 0 and 1, equation (4) shows that the current ripple increases with the increase in coupling factor k. Under the same operating conditions, the equivalent inductor is $L_{eq1} = L(1-k)$ [8].

For state (ii), $V_1 = V_{in}$ and $V_2 = 0$. Thus the current ripple can be given as;

$$\frac{\Delta i_1}{\Delta t} = \frac{V_{in}(1-D) + kV_{in}(-D)}{L(1-k^2)} = \frac{V_{in}(1-D)(1-\frac{D}{1-D}k)}{L(1-k^2)} \tag{5}$$

and the equivalent inductor is $L_{eq2} = \left(\frac{1-k^2}{1-\frac{D}{1-D}k}\right) L$.

However, it is clear from Fig. 2 that steady state ripple is reached at state (iv), where $V_2 = V_{in}$ and $V_1 = 0$, and its value is given by;

$$\frac{\Delta i_1}{\Delta t} = \frac{-V_{in}D(1-\frac{(1-D)k}{D})}{L(1-k^2)} \tag{6}$$

where the equivalent inductor at state (iv) is $L_{eq4} = \left(\frac{1-k^2}{1-\frac{1-D}{D}k}\right) L$. From equation (6), it is evident that increasing the effective inductance L_{eq4} will reduce the steady state current ripple. Fig. 3 plots L_{eq4}/L against the coupling factor for different duty cycles. Accordingly, the effective inductance value is higher than the nominal inductance for duty cycles around 0.5 with a peak value around k equals to 0.6∼0.7.

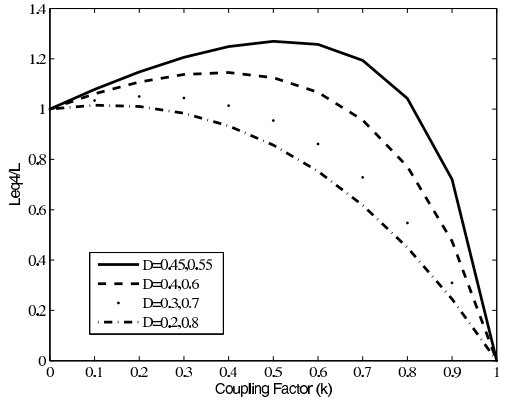

Fig. 3. The normalized effective inductance L_{eq4}/L versus coupling coefficient

For the DC-DC converter's transient behavior, it is measured by the time it takes the converter to stabilize when the input voltage or the duty cycle changes. This is a function of the output filter network formed of the inductance and capacitance as well as their parasitic resistances. For faster transient response, the value of inductor should be small enough to allow a fast slew rate and prevent excessive voltage changes on the capacitor. The equivalent inductor for transient response is given by $L_{eq-trans} = L(1-k)$ [8], which implies that higher coupling coefficients result in reduced rise and fall times.

The above discussion clearly illustrates the effect of negative coupling on the steady state and transient behavior of interleaved DC-DC converters. There is normally an optimum value of k that will satisfy both conditions of reduced current ripple as well as lower rise and fall times during transient operation, depending on the duty cycle or input/output voltage ratings.

III. Circuit Implementation

The interleaved DC-DC converter is designed using a three metal layer, 0.5 μm, GaAs pHEMT process with both depletion and enhancement mode pHEMTs. The schematic shown in Fig. 4 is composed of the main switching stages connected to an output filtering network. The switching stages are driven by two gate drivers whose input is supplied by an external control circuitry. Two loss mechanisms are encountered in the switching stage; the switching losses due to charging and discharging of the devices input capacitance, and conduction losses due to the finite on-resistance of the switching devices. Fig. 5 shows the variation of both losses as a function of the switching transistor width for a given duty cycle of 0.65. The widths of SW1 and SW2 are selected as 20mm, which is the point at which the combined power loss is minimum and the effective efficiency of the converter is maximized. It is worth noting that the plotted efficiency takes into account the losses

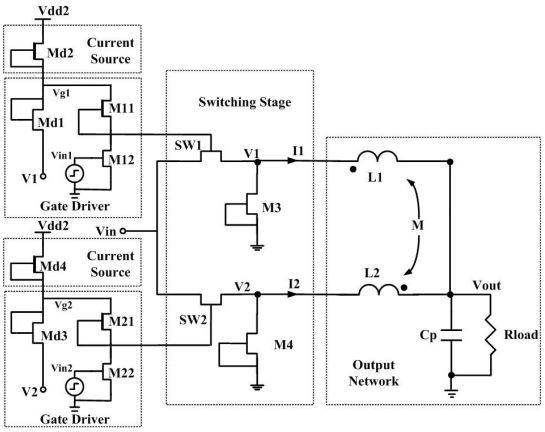

Fig. 4. Circuit Topology

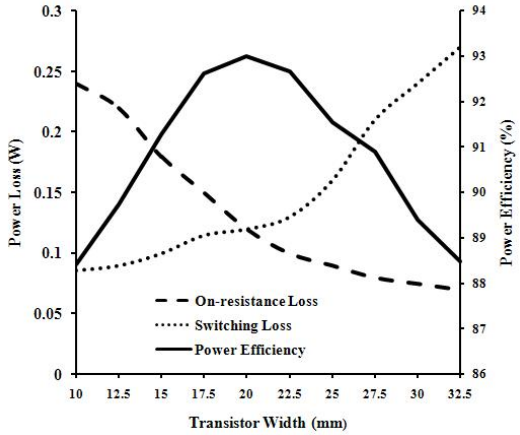

Fig. 5. Transistor loss and overall power efficiency versus transistor width

in the gate driver as well as the switching stage. The diode-connected transistors M3 and M4 are sized to handle the large currents injected when SW1 and SW2 are off. In this design, they are selected to have the same size as SW1 and SW2.

Due to the lack of complementary transistors in the used technology, the gate driver stage is designed as an active load inverter. The Enhancement mode pHEMT M12 is the main switching transistor and Depletion mode pHEMT M11 is connected as the active load. The width of M11 is 1/3 that of M12 for symmetrical switching. The size of M12 depends on the size of the main switching transistor SW1 and is chosen to satisfy the trade off between the power consumption of the gate driver stage and switching loss of SW1. The larger sizes of M11 and M12 provide better driving capability while decreasing the rise and fall times, which will accordingly reduce the switching loss of the main transistor. However, larger sizes of M11 and M12 will also increase the power consumption in the gate driver, thus M12 is sized to be 1/10 of the width of SW1. In order to minimize the power consumption in the gate drivers, their supply voltages (V_{g1},V_{g2}) need to be set at the minimum value to drive SW1 and SW2, which is equal to $V_{1,2} + V_p$, where V_p is the pinch off voltage, and $V_{1,2}$ are the voltages at the sources of SW1 and SW2. This is done by using the current source Md2/Md4 and diode connected transistor Md1/Md3.

To illustrate the advantages and limitations of the coupled interleaved topology, we compared its performance relative to a traditional buck converter, and interleaved structures with no-coupling. Ideal simulations were performed on the four topologies shown in Fig. 6, a single phase buck converter, an interleaved structure without coupling employing a 3nH inductor, an interleaved non-coupled structure with an equivalent inductance of $L_{eq} = (1-k)L$ equals to 0.9nH for k=0.7, and the proposed coupled interleaved structure with the same L=3nH. Table I provides the comparison based on ideal simulations. The coupled interleaved structure provides 7% efficiency improvement over non-coupled structure with the same inductance and 14.6% improvement over non-coupled interleaved structure with an equivalent inductance to the coupled one. The improvement in efficiency comes at the expense of slight increase in current ripple compared to the non-coupled structure with the same inductance. However, the use of coupling will minimize the area consumed by the inductor when implemented on chip.

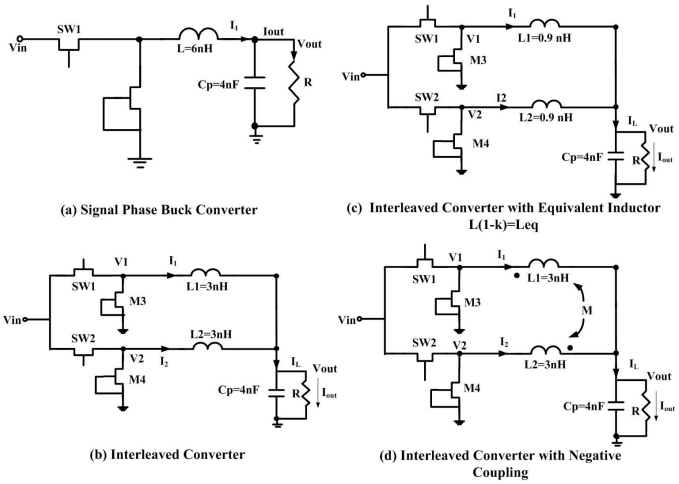

Fig. 6. Comparison between different buck converter topologies

IV. Circuit Characterization

The circuit shown in Fig. 4 was designed at 250MHz with 3nH coupled inductors and 4nF load capacitor. The circuit converts 4.5V input to a 3.3V output with a 1A output current, which is typical for GSM power amplifiers. The duty cycle is selected as 0.65 and the coupling factor is 0.66. The optimum value of coupling was selected according to section II while taking into account the interconnect resistive and capacitive effects extracted from the layout as well as accounting for bondwires. The die micrograph is shown in Fig. 7. The area of the converter is $2.7 * 2.7mm^2$ excluding the output filter. As an initial phase for this work, a separate die containing the coupled-inductor will be connected to the switching stage via bondwire inductances. The extracted efficiency versus output current is plotted in Fig. 8, with the power loss contribution of different elements for the case of an output voltage of 3.3V

TABLE I
COMPARISON BETWEEN DIFFERENT TOPOLOGIES BASED ON IDEAL SIMULATIONS

Type	Buck(6nH)	Interleaved(3nH)	Interleaved(0.9nH)	Interleaved With Negative Coupling
ΔV_{out}(mV)	72	47	123	74
ΔI_{out}(mA)	23	13	62	22.6
ΔI_L(A)	0.415	0.498	2.227	1.03
P_{out}(W)	3.303	3.35	3.68	3.398
Eff.%	85.4	85.8	78.72	93.3

and output current of 1A. Fig. 9 shows the efficiency and output voltage versus the duty cycle. In the shown extracted simulation results, the quality factor of the coupled inductors is set at 20, while a 0.5nH inductance is assumed for the connection between the converter die and coupled inductors die. A 7.3% reduction in efficiency from the ideal simulation case is due to the effect of interconnect losses and finite dc resistance of the coupled inductors in addition to the slight reduction in the coupling factor due to the effect of bond wire inductances.

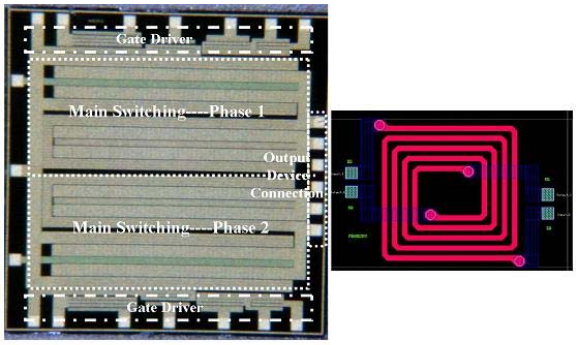

Fig. 7. Die photo of DC-DC converter

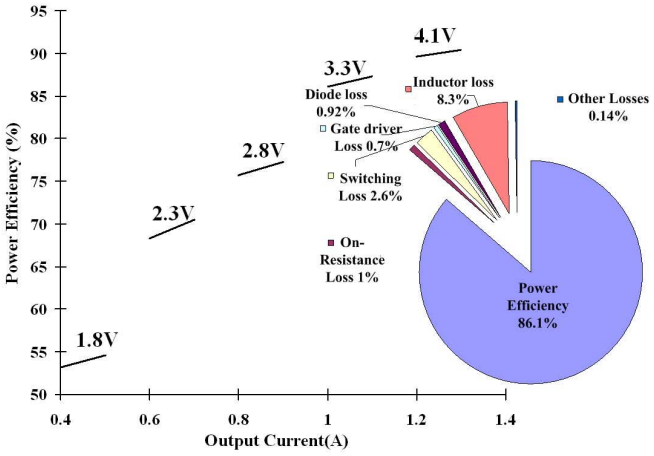

Fig. 8. Power efficiency versus output current. The inset shows power loss contribution of different elements

V. CONCLUSION

An interleaved DC-DC converter with negative coupling has been demonstrated in 0.5μm, pHEMT GaAs technology. GaAs technology provides a faster switch with lower on-resistance and smaller parasitic capacitors compared to CMOS

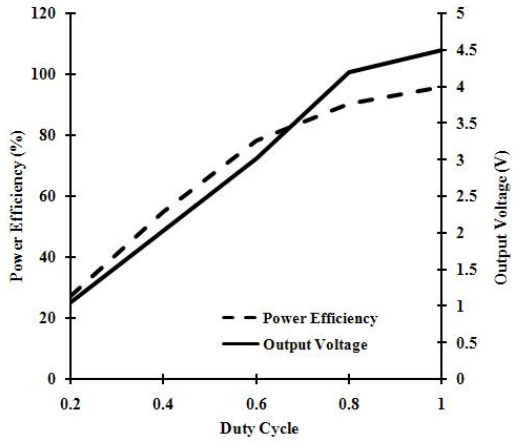

Fig. 9. Output voltage and power efficiency versus duty cycle

technology. This results in an improved efficiency of 86.1% at 250MHz with 4.5V/3.3V output and 1A load current. The highest reported efficiency for DC-DC converters in CMOS technology has been below 80% using in-package inductors at lower current ratings. The proposed architecture is ideal for integrated GaAs power amplifier modules.

VI. ACKNOWLEDGEMENT

The authors would like to acknowledge TriQuint Semiconductor for fabrication.

REFERENCES

[1] P. J. Zampardi, "GaAs technology status and perspectives for multi-band and multi-standard challenges in upcoming RF-frontends", *Radio and Wireless Conference*, pp.187-190, Jan. 2008.

[2] J. Wibben and R. Harjani, "A High-Efficiency DC-DC Converter Using 2nH Integrated Inductors", *IEEE J.Solid State Circuits*, vol.43, no.4, pp. 844-854, April 2008.

[3] P.Hazucha, G.Schrom and J,Hahn, "A 233-MHz 80% Efficient Four-Phase DC-CDC Converter Utilizing Air-Core Inductors on Package", *IEEE J.Solid State Circuits*, vol. 40, no.4, pp. 838-845, April 2005.

[4] G. Schrom, P. Hazucha, J. Hahn, D.S. Gardner, B.A. Bloechel, G. Dermer, S.G. Narendra, T. Karnik and V. De, "A 480-MHz, multi-phase interleaved buck DC-DC converter with hysteretic control", *Power Electronics Specialists Conference*, 2004, pp.4702- 4707.

[5] S. Abedinpour, B. Bakkaloglu and S. Kiaei, "A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 um SiGe Process", *IEEE Trans.on Power Electronics*, vol.22, no.6, pp.2164-2175, Nov.2007.

[6] J. Sun, J. Lu, D. Giuliano, T.P. Chow and R.Gutmann, "3D Power Delivery for Microprocessors and High-Performance ASICs", *Applied Power Electronics Conference*, 2007, pp.127-133.

[7] S. Ajram and G. Salmer, "Ultrahigh Frequency DC-to-DC Converters Using GaAs Power Switches", *IEEE Trans.on Power Electronics*, vol.16, no.5, pp.594-602, Sept.2001.

[8] P.Wong, P.Xu, B.Yang, and F. Lee, "Performance Improvements of Interleaving VRMs with Coupling Inductors", *IEEE Trans.on Power Electronics*, vol. 16, no. 4, pp. 99-507, July 2001.