Analysis and Optimization of Transformer-Based Series Power Combining for Reconfigurable Power Amplifiers

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***Abstract*—Transformer-based series power combiners are analyzed within the context of reconfigurable, watt-level, wideband digital envelope tracking transmitters. A model is developed for designing and analyzing transformer-based switchable series combiners. This model takes into account losses in the windings and nonideal mutual coupling, as well as the effect of switching and scaling the input amplifiers on the combiner efficiency, input impedance, and power combining ratio. Optimum combining efficiency is derived for a combiner with scaled sources. Based on the developed model, a four-element 29.5-dBm power amplifier with 31% peak efficiency at 1.9 GHz, using a 1.5-V supply is designed and simulated in IBM 130-nm CMOS technology. The efficiency drops to 14% at 12 dB power back-off when elements are turned off. The amplifier maintains an output power >25 dBm from 1.8 GHz to 2.5 GHz. The studies presented in this paper can be extended to any series combiner implementation and any frequency range, which can be effective in the design of watt-level power amplifiers in submicrometer CMOS technologies.**

***Index Terms*—CMOS technology, digital transmitter architectures, efficiency enhancement, envelope tracking, power amplifiers, series power combining.**

I. Introduction

RECENT research on CMOS power amplifiers has focused on addressing two fundamental problems. The first is increasing the output power levels, using a combination of cascoding and on-chip power combining [1]–[5]. The second problem is addressing the efficiency/linearity tradeoff, particularly for nonconstant envelope modulation schemes through dynamic biasing of linear amplifiers [6]–[9], polar modulation [10]–[12], outphasing amplifiers [13], [14], and other techniques [15], [16].

The efficiency/linearity tradeoff in power amplifiers is a common problem in any technology and has been widely investigated for many years. Dynamic power-supply tracking schemes [e.g., envelope elimination and restoration (EER), polar modulation (PM), and envelope tracking (ET)] have shown great potential for the realization of high average efficiency and high linearity for high peak-to-average ratio (PAR) signals. They have also been particularly interesting for their potential in multistandard applications such as the software defined radio (SDR) [17]. The EER/PM transmitter in Fig. 1(a) uses a combination of a high-efficiency switched-mode PA with an envelope modulator circuit on the supply. ET, on the other hand, shown in Fig. 1(b), utilizes a linear PA and a controlled supply voltage, which tracks the output envelope. Theoretically, EER/PM is more efficient than ET, since the RF amplifier is operating in a switched mode. However, traditional EER/PM poses practical challenges on the modulation bandwidth of the supply modulator and has been limited to narrowband applications [18]. By contrast, ET requires a smaller envelope amplifier bandwidth and less precise time-alignment between the envelope and the RF paths. The supply modulator for both systems must be designed for high efficiency, wide bandwidth, and the capability to drive a PA load. Linear regulators (LDO) and switch-mode dc-dc converters have been implemented with good performance and adequate bandwidth for their corresponding wireless standards. However, both fail to address the future needs of communication systems as RF bandwidth increases above 10 MHz, with the former suffering from low efficiency, and the later requiring external inductors and producing switching spurs. Increasing the switching frequency in switch mode dc-dc converters can reduce the size of the passive components and simplifies the filtering of the switching spurs. However, this comes at the expense of increasing the switching loss and reducing the overall efficiency of the converter, particularly in CMOS implementations.

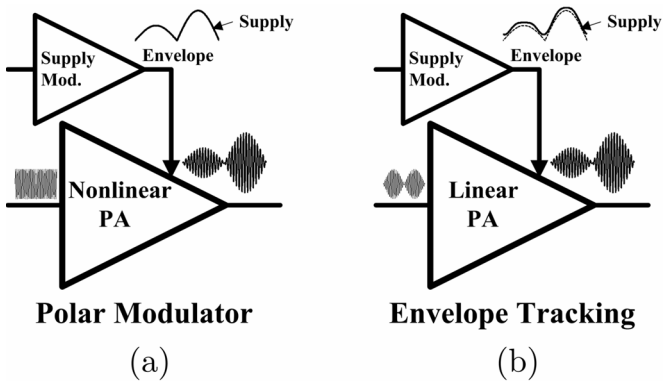

Fig. 1. Dynamic power supply tracking schemes. (a) Polar modulation. (b) Envelope tacking.

Hybrid supply modulators have recently evolved as a possible solution with reported modulation bandwidth up to 4 MHz. Table I compares recent work on supply modulator-based power amplifiers, highlighting efficiency, output power, and die area. An excellent system level analysis that compares various power supply tracking schemes for mobile transmitters is also given in [12].

Digitally inspired envelope modulators [19]–[22] have been shown as a possible solution to eliminate the supply modulator

Manuscript received December 07, 2009; revised April 15, 2010; accepted May 30, 2010. This paper was recommended by Associate Editor E. Alarcon.

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Digital Object Identifier 10.1109/TCSI.2010.2055272

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART INTEGRATED POWER AMPLIFIER SUPPLY MODULATORS

Ref. (Die Area)	Technique	Max P_{out}	Max η	η at -12dB	Technology
[18] ($1.0\times4.0\text{mm}^2$)	5MHz hybrid linear/switched	0.8W	65%	N/A	BiCMOS 180nm
[31] (N/A)	50MHz dual-pulse PWM converter	0.25W	73.5%	23.5%	CMOS 0.6μm
[32] (4.6mm^2)	10MHz hybrid class AB/switched	1.6W	82%	50%	CMOS 350nm
[33] ($1.0\times1.1\text{mm}^2$)	130MHz Switch Mode converter	1.6W	75%	37%	BiCMOS 250nm (w/LDMOS)
[34] ($2.1\times2.0\text{mm}^2$)	Hybrid linear / ΔM reg.	1.2W	76%	30%	CMOS 250nm

and directly reconstruct the signal envelope in the RF domain. They are formed of arrays of unit amplifiers that are activated by a digital code representing the amplitude of the signal envelope. By adapting the number of amplifier units, and thus the dc current, to the envelope, the complete amplifier achieves improvement in average efficiency over output dynamic range. While this approach has been successful in GaAs implementations [20] yielding a true software defined transmitter, its application to CMOS technology has been limited by the breakdown voltage limit of devices. Integrated power combiners can boost the output power level to the watt range; however, the power combiner in this case becomes an integral part of the whole system, affecting its overall efficiency and output power level.

The purpose of this paper is to investigate the behavior of switchable series power combiners when interfaced with various amplifiers types (linear and nonlinear) in digitally inspired envelope modulators, as shown in Fig. 2. The switchable combiner boosts the output power while maintaining efficiency at back-off power levels. While Aoki [2] and An [23] have studied the performance of integrated fixed power combiners, in this work we consider for the first time the effects of scaling the unit amplifiers and switching power amplifier elements on the efficiency and power combining ratio of the series power combining networks. We present a high-level general analysis based on impedance parameters that is independent of the circuit implementation so that the analysis can be extended beyond the special case of transformer-based networks. The analysis also takes into account arbitrary loss mechanisms which has not been reported in previous analyses.

The general model for series combiners is presented in Section II and the effect of scaling on combiner parameters is given in Section III. The special case of transformer-based combining networks is analyzed in Section IV and various characterization is done in Section V. Finally, a design example for a CMOS power amplifier with integrated switchable power combiner in IBM 130-nm CMOS technology is given in Section VI, based on the models derived in Section IV. Analysis and simulation results are presented in Section VII and conclusions are drawn in Section VIII.

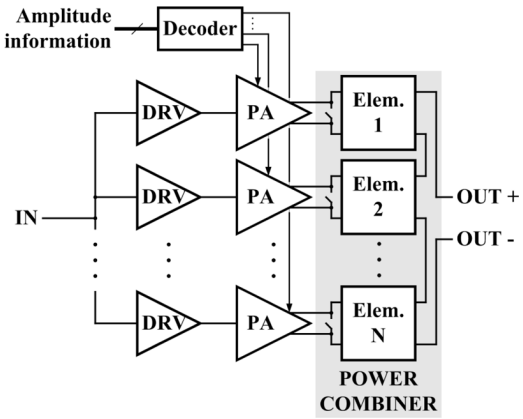

Fig. 2. Digital envelope modulator with array of unit amplifiers and power combiner. Output amplitude is modulated by turning amplifiers on and off.

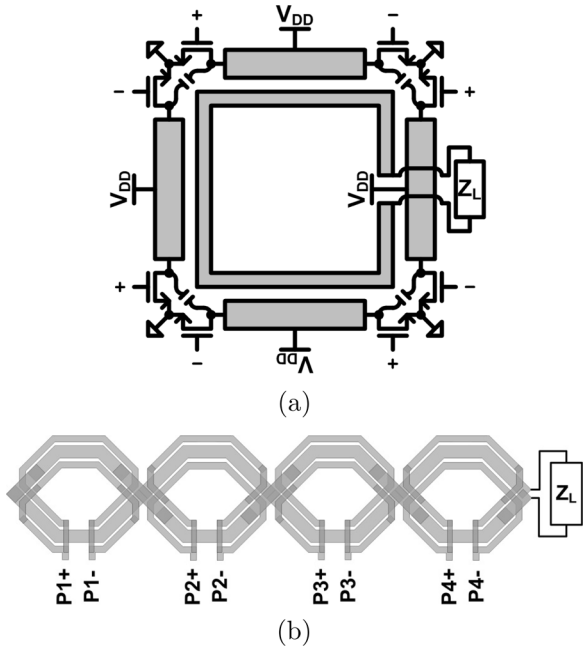

Fig. 3. Different series power combiner implementations. (a) DAT [2]. (b) Figure 8 [24].

II. SERIES POWER COMBINERS

On-chip power combiners are required to raise the output power of CMOS power amplifiers to the watt level, due to the low breakdown voltage of FETs in CMOS technology. In addition to increasing the available output power, combiners can also perform impedance transformation. In fact, the process of power

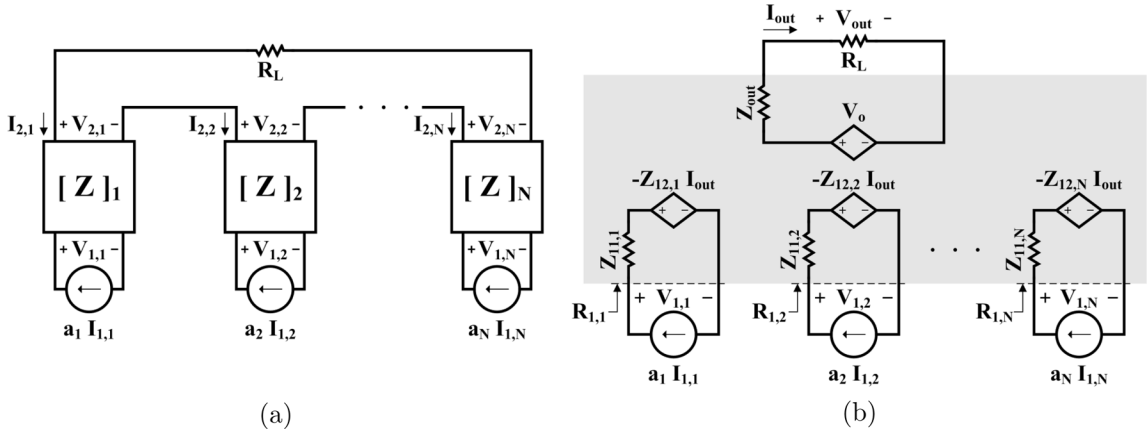

Fig. 4. (a) Series combining network with arbitrary combining element represented by impedance matrix. (b) Model of full power combining network.

combining is essentially a power matching problem where the load impedance is transformed to an optimal impedance for the driving circuitry. Depending on how the combiner is constructed, it may also provide port isolation.

Combiners can be categorized as series or parallel combiners, according to the method that their output signals combine; a series combiner will sum output voltages and a parallel combiner will sum currents of individual elements. Distributed active transformers (DATs) [2] and Figure 8 transformers [24] whose secondary windings are cascaded are examples of existing series combiner implementations. Parallel combiners have also been reported using interleaved transformers [5], [23], lumped-element baluns [25], and external $\lambda/4$ networks [26]. This paper focuses mainly on series combiners given their higher output power capability.

Several implementations of transformer-based series power combiners have been reported in the literature as shown in Fig. 3 [2], [24]. Although successful implementations of power combining schemes exist, a more generalized analysis of the combiner topology and its unit elements can enhance their applicability for multistandard radios and even for high-frequency ranges such as mm-wave and sub-THz ranges where they are needed the most due to the limited power capability of nanometer scale CMOS technologies. Most of the efforts on combiners have focused on compact layout techniques. This manuscript is the first to address the combiner in general, taking into account the effect of the nonidealities of the combining elements, the number of elements, power scaling, and switching of combining elements on the combining efficiency and net output power.

A. General Analysis of the Series Combining Network

Fig. 4 shows the model that will be used to analyze the series power combining system. This model is constructed from unit elements that provide impedance transformation and act as an interface between each power source and the combined output. Each element is represented by an impedance- or Z-parameter matrix, making this analysis generic for any network element implementation. In the case of a series combiner, the combining element provides an output voltage that is summed by stacking the outputs of the elements. In this analysis, an ideal current source is used to model a transconductance device, such as a linear class amplifier. Then the element converts the current signal to an appropriate voltage signal. The choice of impedance parameters in this case comes from the choice of a linear class amplifier as the input current and the summation of voltages at the output. For other cases (such as parallel combining, summing the currents at the output), the choice of a different linear parameter block may be more prudent. The Z parameters of each combiner element are given in (1)

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2. \end{aligned} \tag{1}$$

In Fig. 4(b), the open-circuit output voltage V_o and output impedance Z_{out} across all N elements can be given by (2)

$$V_o = \sum_{i=1}^{N} a_i Z_{21,i} I_{1,i}, \quad Z_{\text{out}} = \sum_{i=1}^{N} Z_{22,i} \tag{2}$$

where the variable a_i, which can take a binary value 1 or 0, represents whether the input at element i is on or off, respectively. Note that, because the inputs are current sources, all inputs are high-impedance and considered open-circuit when the sources are off.

For the rest of the analysis, we will normalize the impedances $Z_{jk,i}$, output impedance Z_{out}, and open-circuit output voltage V_o to the load impedance such that

$$z_{jk,i} = \frac{Z_{jk,i}}{R_L}, \quad z_{\text{out}} = \frac{Z_{\text{out}}}{R_L}$$

and

$$I_o = \frac{V_o}{R_L} = \sum_{i=1}^{N} a_i z_{21,i} I_{1,i}.$$

For simplicity, we will also assume that the load resistance R_L and all input currents $I_{1,i}$ are real. From Fig. 4(b), we can derive the output voltage V_{out}, the output current I_{out}, and the output power P_{out} as (3)–(5), respectively

$$V_{\text{out}} = V_o \left(\frac{R_L}{R_L + Z_{\text{out}}} \right) = R_L \left(\frac{I_o}{1 + z_{\text{out}}} \right) \tag{3}$$

$$I_{\text{out}} = \frac{V_{\text{out}}}{R_L} = \frac{I_o}{1 + z_{\text{out}}} \tag{4}$$

$$P_{\text{out}} = \Re \left\{ \frac{V_{\text{out}} I_{\text{out}}^*}{2} \right\} = \frac{R_L}{2} \left| \frac{I_o}{1 + z_{\text{out}}} \right|^2. \tag{5}$$

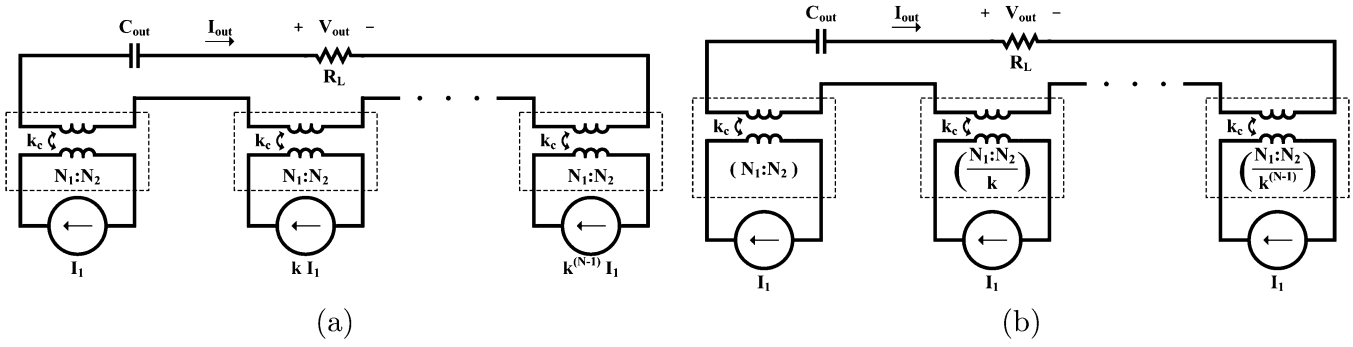

Fig. 5. Series combiners using transformers. (a) Scaled sources, (b) scaled transformers.

The input power of each stage can be found as (6)

$$P_{\text{in},i} = \left(\frac{I_{1,i}^2 R_L}{2}\right) \Re\left\{a_i z_{11,i} - \left(\frac{I_o}{I_{1,i}}\right)\frac{z_{12,i}}{1+z_{\text{out}}}\right\} \tag{6}$$

Thus, the combiner efficiency can be calculated according to (7)

$$\eta = \frac{\left|\frac{I_o}{1+z_{\text{out}}}\right|^2}{\sum_{i=1}^{N} I_{1,i}^2 \Re\left\{z_{11,i} - \left(\frac{I_o}{I_{1,i}}\right)\frac{z_{12,i}}{1+z_{\text{out}}}\right\}} \tag{7}$$

III. Scaled Power Combining Networks

The analysis in Section II is generic for any combining system formed of arbitrary linear combiner elements. In some applications, it is useful to set all output signals equal or scale them in a regular fashion, such as binary. In these cases, further simplifications can be made to the system analysis.

The output voltage signal is scaled when the output generated by adjacent stages is a fixed multiple, represented by k. Therefore, the output signal generated by element 2 is k times that generated by element 1 and so forth. As an example, if the output generated from element 1 is 1 V, then the output generated from element 2 is 0.5 V when $k = 0.5$. When the output is not scaled (when each element generates the same output signal), then $k = 1$.

In practical implementations with power amplifiers, there are two scaling scenarios, as shown in Fig. 5. The first is scaled unit amplifiers feeding a power combiner formed of identical unit elements, and the second is using identical unit amplifiers driving scaled combiner elements (for example transformers with different turns ratios or $\lambda/4$ lines with different characteristic impedances [26]).

A. Scaled Input Currents

As the combiner is assumed to be linear, the source currents are scaled by the same amount as the output. Thus,

$$k = \frac{V_{2,(i+1)}}{V_{2,i}} = \frac{I_{1,(i+1)}}{I_{1,i}}.$$

From this, we can see that

$$I_{1,i} = I_{1,1} k^{(i-1)}.$$

Let us define K_1 as the ratio of the sum of all input currents to the input current of the first element and K_2 as the ratio of the sum of the input powers to the input power of the first element. K_3 is the ratio of the input power generated if the average input current were applied to a single element to the actual average input power per element

$$K_1 = \sum_{i=1}^{N} a_i k^{(i-1)} \text{ and } K_2 = \sum_{i=1}^{N} a_i k^{2(i-1)}.$$
$$K_3 = \left(\frac{K_1}{N}\right)^2 \left(\frac{N}{K_2}\right) = \frac{K_1^2}{N K_2}. \tag{8}$$

When all combining elements are identical, I_o and z_{out} can be simplified as follows:

$$I_o = K_1 z_{21} I_{1,1}, \quad z_{\text{out}} = N z_{22}.$$

Substituting these into (3)–(5), (6), and (7) the output voltage, output current, and the overall efficiency of the combiner can be found as

$$\begin{aligned} V_{\text{out}} &= K_1 I_{1,1} R_L \left(\frac{z_{21}}{1+N z_{22}}\right), \\ I_{\text{out}} &= K_1 I_{1,1} \left(\frac{z_{21}}{1+N z_{22}}\right). \\ P_{\text{out}} &= \frac{K_1^2 I_{1,1}^2 R_L}{2} \left|\frac{z_{21}}{1+N z_{22}}\right|^2 \\ P_{\text{in},i} &= \left(\frac{I_{1,1}^2 R_L}{2}\right) \\ &\quad \cdot \Re\left\{a_i k^{2(i-1)} z_{11} - k^{(i-1)} K_1 \left(\frac{z_{21}^2}{1+N z_{22}}\right)\right\} \end{aligned} \tag{9}$$

$$\Sigma P_{\text{in}} = \left(\frac{I_{1,1}^2 R_L}{2}\right) \Re\left\{K_2 z_{11} - K_1^2 \left(\frac{z_{21}^2}{1+N z_{22}}\right)\right\} \tag{10}$$

$$\eta = \frac{\left|\frac{z_{21}}{1+N z_{22}}\right|^2}{\Re\left\{\frac{z_{11}}{N K_3} - \left(\frac{z_{21}^2}{1+N z_{22}}\right)\right\}} \tag{11}$$

Note that in all of the above derivations, we have assumed a passive, reciprocal network where $z_{12} = z_{21}$.

From (8), we can see that K_3 will decrease when the currents applied to each element become nonuniform. When this happens, the effect of the input loss of the combining elements z_{11} is magnified and the efficiency decreases. This occurs when the sources are scaled ($k \neq 1$), or when any are shut off. This is quantified in Section V for transformer-based combiners. In the case of a unary system ($k = 1$), K_3 is independent on the

number of elements and does not vary from 1 when all elements are on. However, it is always less than 1 for a binary system and decreases when increasing the number of elements.

B. Scaled Combining Elements

In this analysis, the sources are assumed to be identical and the combining elements are scaled (such as transformer turns ratio, $\lambda/4$ line characteristic impedance, etc). First, the criteria for scaling the elements are derived, then the circuit quantities are presented.

Because V_{out} is linearly proportional to $z_{21,i}$, scaling $z_{21,i}$ will also result in the scaling of V_{out} for different states

$$\frac{z_{21,(i+1)}}{z_{21,i}} = k \rightarrow z_{21,i} = k^{(i-1)} z_{21,1}. \tag{12}$$

Similar analysis can be performed, as in the case of scaled sources. Note that, in this case, the output impedances $z_{22,i}$ cannot be determined, as they depend upon the actual implementation of the element

$$I_o = K_1 z_{21,1} I_1. \tag{13}$$

By substituting in (3)–(5), the output voltage, current, and power can be derived

$$V_{\text{out}} = K_1 I_1 R_L \left(\frac{z_{21,1}}{1 + z_{\text{out}}} \right) \tag{14}$$

$$I_{\text{out}} = K_1 I_1 \left(\frac{z_{21,1}}{1 + z_{\text{out}}} \right) \tag{15}$$

$$P_{\text{out}} = \frac{K_1^2 I_1^2 R_L}{2} \left| \frac{z_{21,1}}{1 + z_{\text{out}}} \right|^2 \tag{16}$$

$$P_{\text{in},i} = \left(\frac{I_1^2 R_L}{2} \right) \Re \left\{ a_i z_{11,i} - K_1 \left(\frac{z_{21,1}^2}{1 + z_{\text{out}}} \right) \right\}. \tag{17}$$

Assuming that z_{11} does not change from element to element and all elements are on ($a_i = 1$ for all i), we can calculate the efficiency

$$\Sigma P_{\text{in}} = \left(\frac{N I_1^2 R_L}{2} \right) \Re \left\{ z_{11} - K_1 \left(\frac{z_{21,1}^2}{1 + z_{\text{out}}} \right) \right\} \tag{18}$$

$$\eta = \frac{K_1^2 \left| \frac{z_{21,1}}{1+z_{\text{out}}} \right|^2}{N \Re \left\{ z_{11} - K_1 \left(\frac{z_{21,1}^2}{1+z_{\text{out}}} \right) \right\}}. \tag{19}$$

C. Scaled Sources Versus Scaled Elements

While scaling either the input or combining elements are theoretically possible, and will ideally yield similar results, the analysis going forward will focus on fixed combining elements, specifically a transformer, with scaled or unary inputs. There are several reasons for this.

First, it is often simpler in practice to design scaled amplifiers than transformers. If the combiner is to be operated dynamically (turning elements on and off), the linearity of the output power will be directly related to the accuracy of the scaling of the combining elements. Because designing a transformer for specific winding reactances is an iterative process, it may be difficult to converge to the desired value for a specific scaling factor.

Second, the output loss of the transformer (Z_{22}) will change from element to element. This is not easily predictable, as it is a function of several factors, such as winding loss, parasitic capacitance, and stray inductance. To accurately predict this behavior, and its variation from element to element, would be quite complicated.

Finally, and specifically for the case of a transformer combining element, extending the number of scaled units is limited. A 1:1 transformer is easily constructed, as is a 1:2 and 1:4 transformer. However, beyond this, the length of the secondary winding becomes significantly long (because the transformation ratio is related to the square of the windings reactances, thus their length) and its losses contribute to the reduction in system efficiency, particularly at high frequencies.

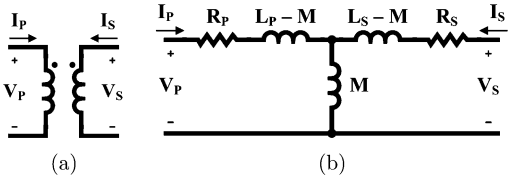

Fig. 6. (a) Schematic symbol and (b) T-model of a transformer.

TABLE II
TRANSFORMER MODEL QUANTITIES

Parameter	Description
n	Transformation ratio, $n = \sqrt{X_S/X_P}$
k_c	Coupling factor between windings, $-1 \leq k_c \leq 1$
X_P	Reactance of primary winding, $X_P = \omega L_P$
X_S	Reactance of secondary winding, $X_S = \omega L_S$
Q_P	Quality factor of primary winding, $Q_P = X_P/R_P$
Q_S	Quality factor of secondary winding, $Q_S = X_S/R_S$
Q_M	Mutual quality factor, $Q_M = k_c^2 Q_P Q_S$

IV. ANALYSIS OF TRANSFORMER-BASED SERIES COMBINERS

In this section, we will consider the case of a transformer as a combining element. The secondary windings are tied together in series such that the currents delivered to the primary terminals are then added as voltages across the secondary terminals, as shown in Fig. 5(a). In an ideal transformer, the output voltage and current are directly proportional to the input, yielding an impedance transformation. For this analysis, the T-model shown in Fig. 6 is used [27]. In this model, M is the mutual inductance and L_P and L_S are the self-inductances of the primary and secondary windings, respectively.

Reactances X_P and X_S are used instead of the actual inductances L_P and L_S, and the quality factors Q_P and Q_S are used instead of the absolute resistances R_P and R_S. In addition to these standard values, an additional parameter will be defined: the *mutual quality factor* $Q_M = k_c^2 Q_P Q_S$ [28]. This parameter includes all nonidealities of the transformer captured by the T-model and directly affects the efficiency of the system. Table II summarizes these relationships.

From the T-model, the Z parameters can be calculated (20). For simplicity, the coupling loss resistance, sometimes seen in series or parallel with M, is neglected

$$Z_{11} = \frac{X_P}{Q_P}(1 + jQ_P) \quad Z_{12} = jk_c\sqrt{X_P X_S}$$
$$Z_{21} = jk_c\sqrt{X_P X_S} \quad Z_{22} = \frac{X_S}{Q_S}(1 + jQ_S). \tag{20}$$

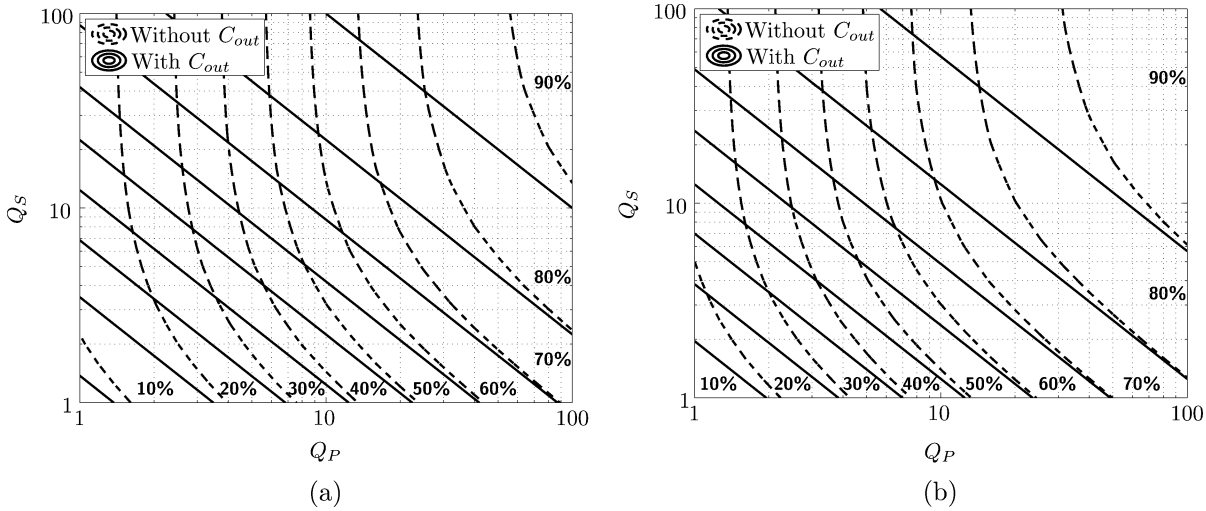

Fig. 7. Efficiency of combiner as a function of primary and secondary quality factors. $N = 4; k = 1$ and coupling factor (a) $k_c = 0.6$, (b) $k_c = 0.8$.

By substituting the above Z parameters into (9) and (11) for a system with scaled sources and identical transformers, the output power and efficiency can be written as (21) and (22), respectively

$$P_{\text{out}} = \left(\frac{K_1^2 I_{1,1}^2 R_L}{2N^2 n^2}\right)\left[\frac{x_S^2 k_c^2 Q_S^2}{(x_S - x_C)^2 Q_S^2 + (x_S + Q_S)^2}\right] \tag{21}$$

$$\eta = \frac{x_S Q_S}{x_S(x_S + Q_S) + \frac{(x_S+Q_S)^2 + Q_S^2(x_S - x_C)^2}{K_3 Q_M}}, \tag{22}$$

where normalized primary and secondary reactances are used in the above equations and defined as $x_P = NX_P/R_L$ and $x_S = NX_S/R_L$, respectively. x_C is the normalized reactance of the capacitor at the output, $x_C = 1/\omega R_L C_{\text{out}}$.

When there is no capacitor ($x_C = 0$) connected in series with the output, we see that the efficiency is a function of the secondary winding reactance X_S and quality factor Q_S, and mutual quality factor Q_M. The optimal reactance can be found by differentiating η by x_S

$$x_{S(\text{opt})} = \frac{Q_S}{\sqrt{Q_S^2 + K_3 Q_M + 1}} \tag{23}$$

$$\eta_{(\text{opt})} = \frac{1}{1 + 2\left(\frac{1+\sqrt{Q_S^2 + K_3 Q_M + 1}}{K_3 Q_M}\right)}. \tag{24}$$

By adding a capacitor in series with the secondary winding to resonate the inductive reactance of the transformer, the efficiency can be increased. In this case, the optimal component values are as given in (25) and (26). When all elements are equal and on ($K_3 = 1$), (25) and (27) agree with the results previously published in [2]

$$x_{S(\text{opt})} = \frac{Q_S}{\sqrt{K_3 Q_M + 1}} \tag{25}$$

$$x_{C(\text{opt})} = x_S \tag{26}$$

$$\eta_{(\text{opt})} = \frac{1}{1 + 2\left(\frac{1+\sqrt{K_3 Q_M + 1}}{K_3 Q_M}\right)}. \tag{27}$$

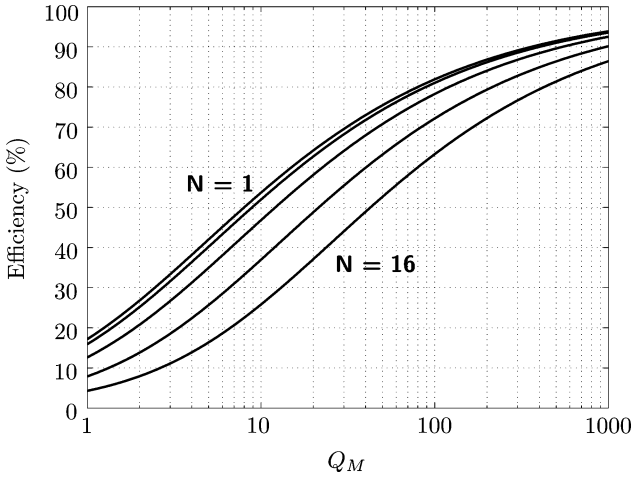

Fig. 8. Efficiency of combiner as a function of Q_M. Binary scaling ($k = 0.5$), number of elements $N = 1, 2, 4, 8, 16$. Optimal x_S and C_{out}.

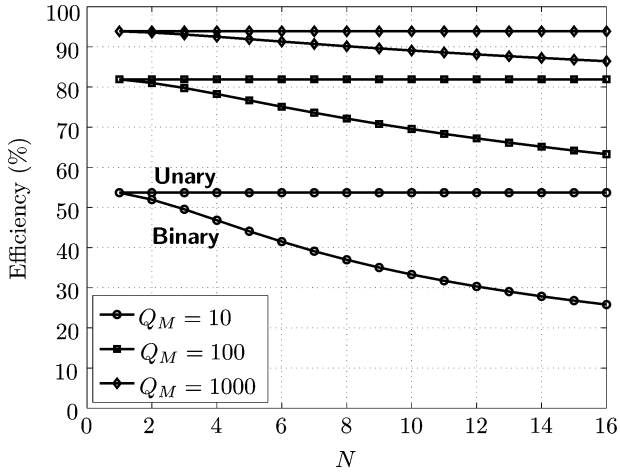

Fig. 9. Efficiency of combiner as a function of the number of combining elements.

Note the capacitor resonates with the sum of the inductive reactances, so it is not scaled by N when denormalized.

Fig. 7 plots (24) and (27) to show the effect of finite winding quality factors on the efficiency of the power combining system with and without C_{out} for selected coupling factors k_c. From

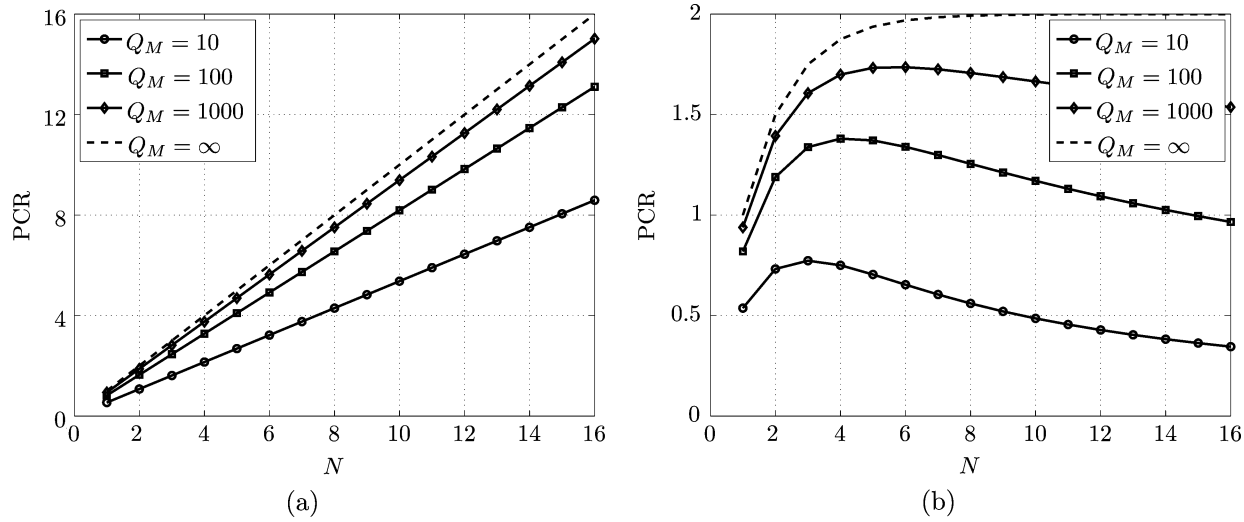

Fig. 10. PCR as a function of the number of elements. $Q_M = 10, 100, 1000; N = 1, 2, 4, 8, 16$. (a) Unary, (b) binary.

this figure, and as can be seen from the equations, adding the capacitor removes the additional contribution of Q_S in the denominator of η, thereby increasing the efficiency. While C_{out} will reduce the effective bandwidth of the combining system, the efficiency improvement can be significant, especially for low-quality transformers. As seen in Fig. 7, for $Q_P = Q_S = 20$ and $k_c = 0.6$, the efficiency increases from almost 74% to 84% by adding C_{out}. For a transformer with higher coupling coefficient ($k_c = 0.8$), the efficiency increases from almost 82% to 87% with the addition of the output capacitance C_{out}.

V. Characterization of Nonideal Power Combiner

The overall vision for future watt-level power amplifiers is that the system of unit amplifiers together with power combiner can be part of a digital to RF power converter. In this section, we investigate the combining efficiency and power combining ratio of power combiners when interfaced with equal unit amplifiers (unary combining) or binary weighted amplifiers. Unless otherwise stated, data is presented when all elements are on.

Fig. 8 shows the effect of general nonidealities in the transformer-based combiner on the efficiency for the case of unary and binary combiners with different numbers of elements ($N = 1, 2, 4, 8, 16$) and an optimal x_S and C_{out}. From (27), the efficiency is a function of Q_M, which quantifies the nonideal behavior of the transformer, and K_3, which describes the state of the system. Because K_3 does not vary from 1 in a unary system when all elements are on, the efficiency is independent of the number of elements and follows the top line in the figure. However, for a binary system, K_3 decreases with increasing N, resulting in reduced efficiency. For typical integrated CMOS transformers ($k_c = 0.7, Q_P = Q_S = 15$), Q_M is approximately equal to 100; in this case, the maximum efficiency for a unary system is about 81%, whereas the maximum efficiency for a binary system with 4 elements is about 78%, and it drops significantly as the number of elements increases.

Fig. 9 shows the effect of increasing the number of elements in the combiner on the overall efficiency for both unary and binary power combining. As shown above, if a unary system is designed optimally, the efficiency does not degrade as the number of elements increases. However, if the system consists of scaled elements, we see that the efficiency decreases with increasing N.

A useful metric for a power combining system is power combining ratio (28) [2]. For a unary system ($P_{\text{in},1} = \cdots = P_{\text{in},N}$), PCR is defined as the output power divided by a unit input power. However, when the elements are scaled, PCR can be defined as the output power divided by the input power of the first (reference) element, since all other input elements are simply scaled versions of this

$$\text{PCR} = \frac{P_{\text{out}}}{P_{\text{in},1}}. \tag{28}$$

It is intuitive that increasing the number of elements will increase the PCR—more input power will increase the output power—and this is what is seen in Fig. 10(a) for a unary system. While finite Q_M will reduce the effect, the figure does show a monotonic increase in PCR as more elements are added. However, for binary scaling, in Fig. 10(b), we see that the PCR will reach a maximum and then start to decrease. This is because the efficiency drops off significantly for an increasing number of elements reducing the output power for a given input power. For $Q_M = 100$, the PCR will reach a maximum at 4 elements and then start to decrease.

Fig. 11 shows the PCR for unary and binary cases versus Q_M. As is shown, finite Q_M has more significant effect on the system as the number of elements is increased. From Fig. 11(b), adding elements to a binary system will actually decrease the PCR below about $Q_M = 10$.

For the case of a power combiner with four elements, Fig. 12 shows the efficiency of the combining system as some stages are switched off. If a 4-digit binary word controls the respective element, the unary system will have four states and binary system will have 16, including a state 0 when all elements are off (in fact, both systems will have 16 states, but in the unary system, each state is repeated four times, one for each position in the control word). In this model, when a stage is off, the input to the combiner is left open-circuited. It can be seen from the figure that the efficiency does vary significantly over different states.

Fig. 13 plots PCR versus state. If the transformer is close to ideal, switching elements on and off will provide a linear output power depending on the switch state, which can be used as an accurate power control mechanism. Although a unary system provides higher PCR and higher efficiency, its output power quantization levels are relatively large which could be beneficial for

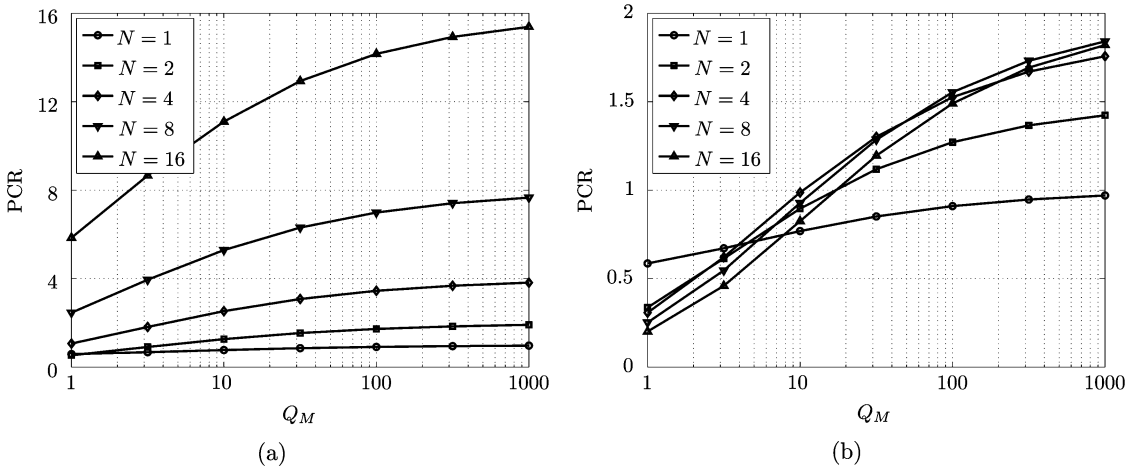

Fig. 11. PCR as a function of Q_M. $N = 1, 2, 4, 8, 16$. (a) Unary, (b) binary.

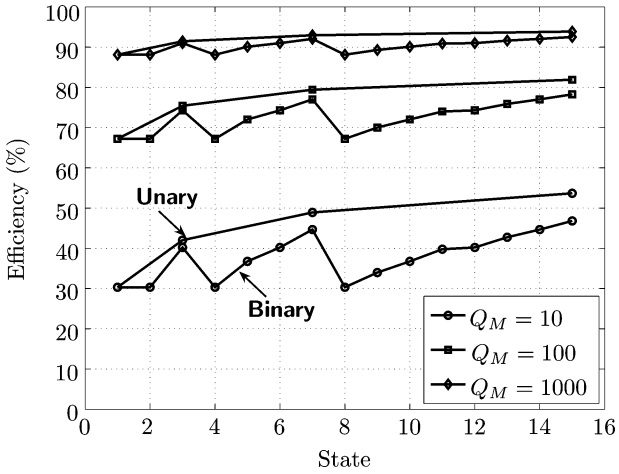

Fig. 12. Efficiency as a function of state. $N = 4, Q_M = 10, 100, 1000$.

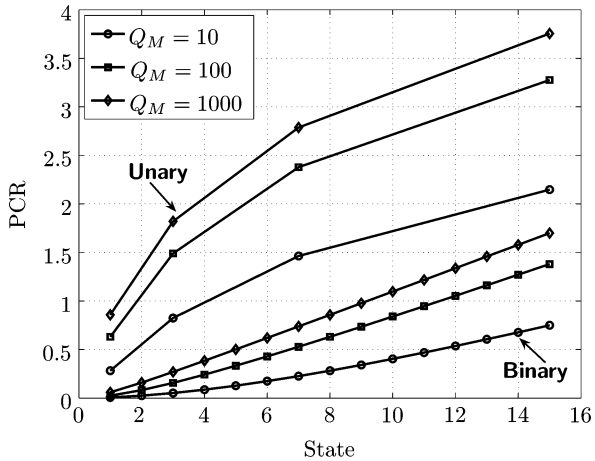

Fig. 13. PCR as a function of state. $N = 4; Q_M = 10, 100, 1000$.

coarse power setting, but does not have the resolution that a binary-scaled system would have for a digital to RF power converter.

Finally, Fig. 14 shows the overall effect of amplifier scaling on the efficiency of a transformer-based series power combiner. While the efficiency of the unary combiner is independent of N, it decreases as a strong function of N when k varies from unity. This can be explained as follows: when all elements are

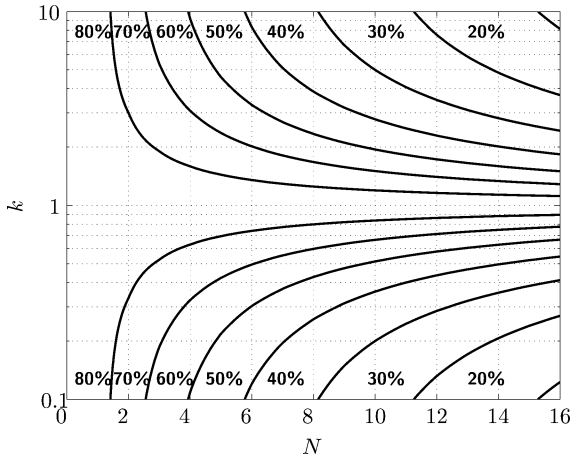

Fig. 14. Efficiency of series combiner as a function of scaling k and number of elements N. $Q_M = 100$.

driven by identical currents, the transformer will couple some of the magnetic flux to the secondary, increasing its reactance and thus, its effective quality factor. If the current applied to the primary winding decreases, the magnetic flux coupled to the secondary also decreases, reducing its effective reactance and quality factor. This reduction in the effective quality factor contributes to the reduction in the overall combiner efficiency.

VI. Design of CMOS Power Amplifier With Switchable Series Combining Network

A four-element power amplifier for WCMDA standard is designed in an 130-nm CMOS process to illustrate the benefits and limitations of switchable series power combiners. The process has eight metal layers, including two thick RF top metals to facilitate high-quality passives that are used for signal routing and implementation of the transformers. Thin oxide (1.2 V) devices are used exclusively for the amplifiers and thick oxide (3.3 V) switches are used across the primaries of the transformers. Four pseudodifferential Class-AB amplifiers are used. Given the negative effect of scaling on the efficiency of the power amplifier as discussed in Section V, unary combining is employed.

A pseudodifferential topology is used for the power amplifier, providing a virtual ac ground at the power supply and ground nodes that allows for suppression of even harmonics and provides dc power feed through a center tap on the primary winding

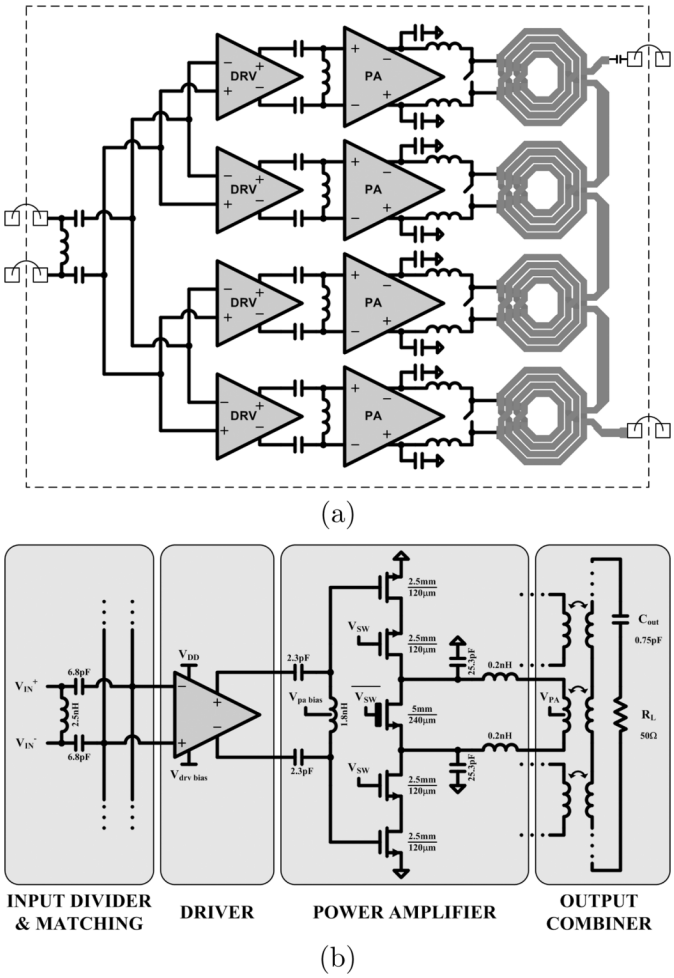

Fig. 15. (a) System-level schematic and (b) unit element schematic.

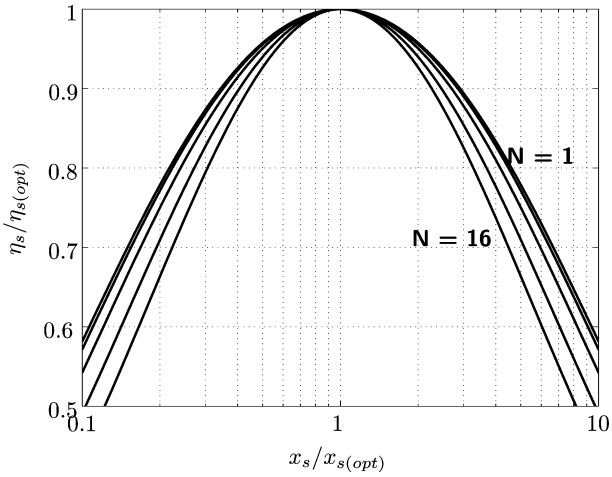

Fig. 16. Efficiency of combiner as a function of nonoptimum secondary reactance. $k = 0.5; N = 1, 2, 4, 8, 16; C_{\text{out}} = C_{\text{out(opt)}}$.

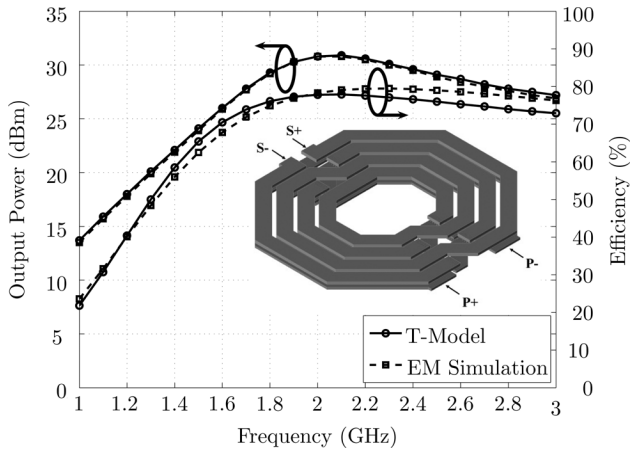

Fig. 17. Transformer model comparison: T-model versus EM Simulation in 4-element combiner. Unary, $I_1 = 450$ mA. Inset: 1:4 overlap transformer.

of the transformer. While device matching is critical for pseudo- and fully differential circuits, devices in power amplifiers are typically large enough such that imperfections are fairly distributed evenly across the die. Still, care must be taken to place complementary devices as close as possible to reduce any undesirable mismatch effects.

Fig. 15 shows the system-level and unit element schematics. Each power stage is fed by a driver amplifier that is designed to be active at all times, and provides a buffer between the input and the PA stages that will be enabled and disabled as needed. Thus, a single on-chip input matching network is implemented as shown in the figure. An input division network distributes the power among the four unit drivers and is implemented as a simple binary tree network. The layout of the elements is linear (as opposed to a ring, such as in [29]) for simplicity of routing and access to the output pad. During the design, inductances of 1 nH are placed in series with the input and output signal lines during tuning to include the effect of bond wires in simulations.

A. Design of Transformer-Based Series Power Combiner

DATs [2] and Figure 8 transformers [24] have been reported as examples of series combiners with promising results in terms of efficiency and die area. The DAT has been implemented with slab inductors with high-quality factors, but takes up a large area and has limited coupling. In addition, because of the large size, resonant capacitors are added between the windings, instead of across them, making use of the virtual ac ground generated from the differential operation of the amplifiers. Thus, the scheme would not lend itself to scaling or dynamic amplifier operation. The Figure 8 transformer has demonstrated a small size and high coupling, however, due to the nature of the layout, the turns ratio of the unit transformer is severely limited. Further, because of a split secondary winding, the signal is coupled from the primary winding to the secondary winding twice, slightly out of phase, and cannot accurately be modeled using the simple T-model.

The vertically stacked (overlap) transformer [27] is chosen as the unit combiner because of its smaller size and increased coupling factor compared with a standard lateral transformer. While the stacked windings produce an increased interwinding capacitance, reducing the peak Q frequency, this effect is not significant at the current operating frequency. This topology also provides a simple layout, since each winding is constructed on a separate plane and can be designed somewhat independently. However, this topology might not always be practical, especially for certain processes without RF top metal layers, or with metal layers close to the substrate.

The design of each unit transformer in the series combiner is an iterative process. To begin, assumptions are made regarding the device. While maximizing the coupling and quality factors of the windings maximizes the combining efficiency, realistic

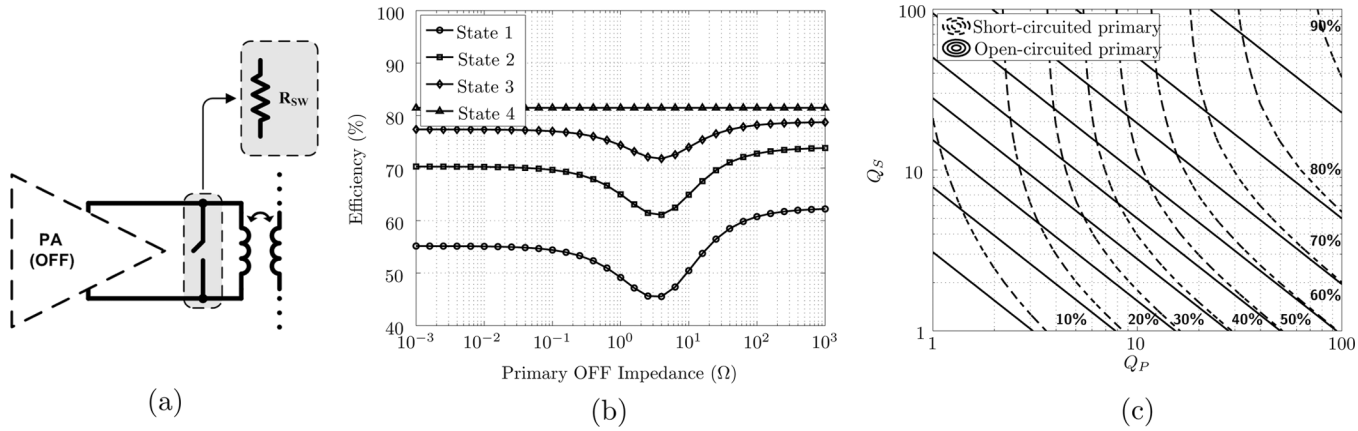

Fig. 18. (a) When an amplifier is off, the primary winding of the transformer can be shorted or opened. (b) Combiner efficiency as a function of off-element primary resistance. $N = 4$, transformer $Q_P = Q_S = 13, k_c = 0.75$. (c) Efficiency of a 4-element unary transformer-based power combiner in State 1 versus primary and secondary winding quality factors. $k_c = 0.8$.

values must be chosen beforehand in the initial design of the transformer. In this case, the initial coupling factor is assumed to be around $k_c = 0.75$ and quality factors $Q_P = Q_S = 13$. Finally, some assumptions regarding the input and output signals are necessary. Each PA element is assumed to generate about 500 mA of current into the combiner for a maximum output power of 30 dBm (1 W).

From the information provided (frequency band, input current, element scaling, coupling, and quality factors), the optimal reactances of the transformer windings and output capacitor C_{out} can be determined using (25) and (26), respectively. From these equations, the optimal secondary inductance is found to be $L_S = 1.35$ nH and output capacitor $C_{\text{out}} = 1.2$ pF. Solving for n, (21) can be used to determine the turns ratio of the transformer. In this case, $n = 4.1$, yields a primary inductance $L_P = 0.082$ nH.

Because it is not trivial to design and manufacture a transformer with a specific winding inductance, it is useful to determine the effect of a nonoptimal winding reactance. Fig. 16 shows the effect of using a nonoptimal secondary reactance. It is shown that, as long as the reactance is within a factor of 2 of its optimal value, the efficiency of the system is above 95% of its optimal value.

Because the optimal inductances calculated in this example are so small, the transformer was designed for a secondary inductance twice the optimal value. From (21), it can be seen that to maintain the output power, either the turns ratio must be increased or the input current must be decreased. In this case, it was chosen to maintain a turns ratio of about 4 and decrease the input current, which also simplifies the design of the amplifiers.

The transformer is simulated using Agilent Momentum and the T-model parameters are extracted from the Z parameters. The primary and secondary inductances are $L_P = 0.2$ nH and $L_S = 2.9$ nH, yielding a turns ratio $n = 3.8$.

The transformer measures approximately 300 μm $\times$ 350 μm, while the combiner is approximately 375 μm $\times$ 1450 μm. Fig. 17 shows the vertical transformer used in this work and compares the output power and efficiency of the EM-simulated transformer and the T-model.

TABLE III
SUMMARY OF RESULTS

	State 4	State 3	State 2	State 1
Technology	130nm CMOS			
Chip size (mm^2)	2.0 x 2.0			
Gain (dB)	26.9	25.9	23.0	18.1
P1dB (dBm)	29.5	26.5	22.5	17.5
Efficiency @ P1dB (%)	31	27	25	14
Efficiency @ 17dBm (%)	7	8	11	14

B. Output Stage Design

The schematic of the unit amplifier is shown in Fig. 15(b). A pseudodifferential cascoded linear Class-AB topology is used as the PA element in the combining system as a compromise between linearity and efficiency. The cascode topology offers several advantages. First, because of the limited drain voltage in modern CMOS processes, the stacking of the MOS transistors in the cascode topology eases the voltage constraints of the devices by effectively doubling the allowed drain voltage swing across the amplifier. Also, by stacking the devices, a higher channel impedance is achieved, increasing the amplifier output impedance. Finally, by applying a positive or grounded signal to the cascode device, the amplifier can be switched on or off.

The device sizes are chosen to achieve a system P1 dB of approximately 30 dBm. Each device is a 2500 μm/0.12 μm NMOS with an optimal load impedance of about $4+j4\Omega$, as determined by a simulated loadpull. DC is fed in from a center tap in the primary winding of the transformer, eliminating the need for an RF choke. Each amplifier has a matching network between the previous driver and itself. The network includes a differential shunt inductor with gate bias fed in through a center-tap.

C. MOSFET Switch and Unused Primary Termination

When an amplifier is turned off, it must be effectively removed from the circuit to avoid unnecessary loading on the system to maximize efficiency. This can be accomplished by shorting or opening the primary winding of the unused transformer element [Fig. 18(a)]. Ideally, either would be sufficient;

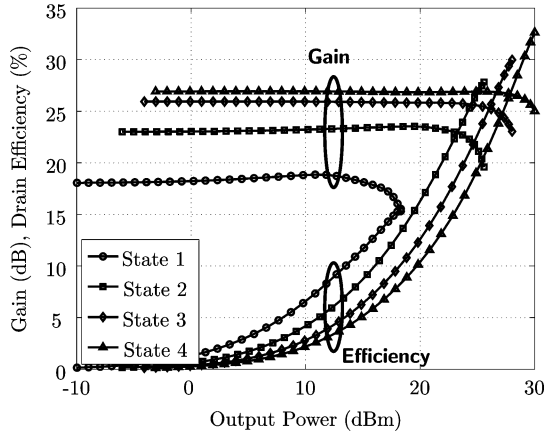

Fig. 19. Power gain and efficiency versus output power.

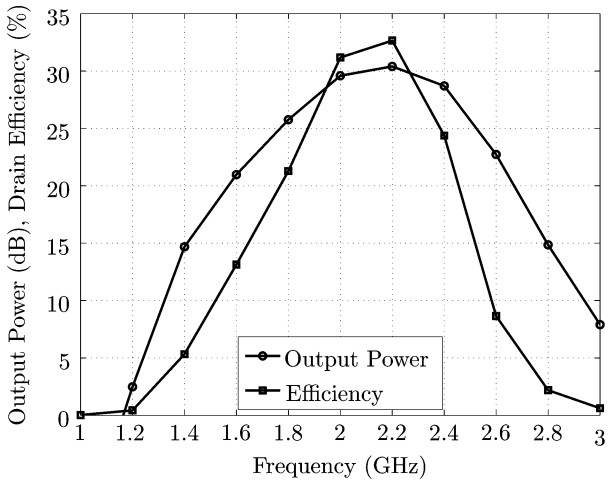

Fig. 20. Output power and efficiency over frequency.

however, Fig. 18(b) shows the combiner efficiency for various primary resistances on unused elements. From the figure, it can be seen that a high impedance, or open circuit will produce a higher efficiency than a lower impedance, or short circuit.

Because a transformer is a reciprocal device, power is coupled from the primary winding to the secondary, as well as vice versa. When a current path exists through the primary, any loss in the winding will cause additional loading for the secondary and add loss to the system. If the primary winding is open-circuited, the current path is broken and its loss will not contribute to the overall output power loss.

Open-circuiting the primary winding will result in a variation in the effective reactance of the secondary winding because the flux from the primary winding will no longer add to that of the secondary. This is taken into account in the model and results in the drop in efficiency seen when elements are turned off, or are driven in a nonunary fashion.

To quantify these effects, the system was solved using a short circuit at the input that is turned off and the combiner efficiency is derived as in (29); this is the case using an optimal secondary reactance x_S and output capacitor x_C

$$\eta_{(\mathrm{opt})} = \frac{1}{1+2\left(\frac{1+\sqrt{K_3 Q_M+(Q_M+2)\alpha+1}+\alpha}{K_3 Q_M}\right)} \tag{29}$$

where

$$\alpha = Q_M\left(\frac{1-K_3}{Q_P^2+1}\right).$$

When $K_3 = 1, \alpha = 0$ and (29) reduces to (27). Fig. 18(c) shows the efficiency of a 4-element unary transformer-based combiner with only one element on versus primary and secondary quality factors for the cases of open-circuited and short-circuited primaries. It can be seen that, for a large Q_P, the efficiencies are close, even for varying Q_S. However, as Q_P drops, the efficiency in the case of short-circuited primary windings falls off faster than when the primary windings are open-circuited.

This analysis produces another interesting result. Because the K_3 parameter quantifies two aspects of the system (switching sources on and off and input signal scaling), both modes of operation are shown to be equivalent in the model. From this, we can see that driving the combiner with a high-impedance (current) source will result in a higher combiner efficiency when the elements are scaled or switched off.

In the designed circuit, an open circuit could not be easily constructed without severely distorting the output signal and introducing losses in other areas. Thus, a short circuit was chosen, which was implemented using a 5000 μm/0.24 μm thick-oxide NFET across the differential output lines.

VII. Results

A. Extracted Simulation Results

Table III presents a summary of the circuit performance from extracted simulations. In state 1, a single element is on, whereas in state 4, all elements are on. Fig. 19 shows the power gain and efficiency for different operating states. The maximum power gain of the power amplifier is 27 dB with a maximum output power of 29.5 dBm and an efficiency of 31%. At state 1, when only one amplifier is on, the maximum output power is 17 dBm at an efficiency of 14%, which is twice as high as that obtained by the same output power when all 4 amplifiers are on. Another advantage of the transformer-based power combiner is the frequency response of the power amplifier as shown in Fig. 20, where the output power is maintained over 25 dBm over 700 MHz of bandwidth from 1.8 GHz to 2.5 GHz, and efficiency is above 20% from 1.8 GHz to 2.43 GHz respectively.

Table IV compares this work with several recent series combiner works. Both this work and [10] make use of switching amplifiers off at reduced output to save power and increase efficiency.

B. Limitations of Series Combiner Model

Fig. 21 compares the simulated efficiency of the PA system and the efficiency predicted by the short-circuit model, showing good agreement. While Fig. 17 also shows reasonable agreement between combiners using the T-model and EM-simulated transformer, the inset in Fig. 21 shows a significant difference in the input impedances for a system using the T-model and simulated transformer. For the system with the T-model, the impedance varies between about $1 + j2.5\Omega$ and $4 + j2.5\Omega$ (the imaginary component remains constant). However, the impedance of the system with the real simulated transformer is significantly different; the impedance varies between about

TABLE IV
COMPARISON OF INTEGRATED POWER AMPLIFIERS WITH SERIES POWER COMBINING

Ref.	Technique	Frequency	Max P_{out}	Max η	η at -12dB	Technology	Amplifier class	V_{DD}	Die Area
[10]	DAT	1.88GHz	1.7W	35%	16%	CMOS 180nm	Nonlinear Class E	0.3V–3V	2.0×1.5mm^2
[29]	DAT	GSM, EGSM DCS, PCS	3.2W 2	51% 45	N/A	CMOS 130nm	Linear	3.5V	2.8×1.5mm^2
[35]	DAT	2.4GHz	2.2W	31%	3%	CMOS 350nm	Nonlinear Class E/F$_3$	2V	1.3×2.0mm^2
[36]	Symmetric XFMR	2.4GHz	0.6W	30%	5%	CMOS 90nm	Linear Class AB	3.3V	2.1×2.0mm^2
This work*	Octagonal XFMR	1.9GHz	0.9W	31%	14%	CMOS 130nm	Linear Class AB	1.5V	2.0×2.0mm^2

* Extracted simulation results.

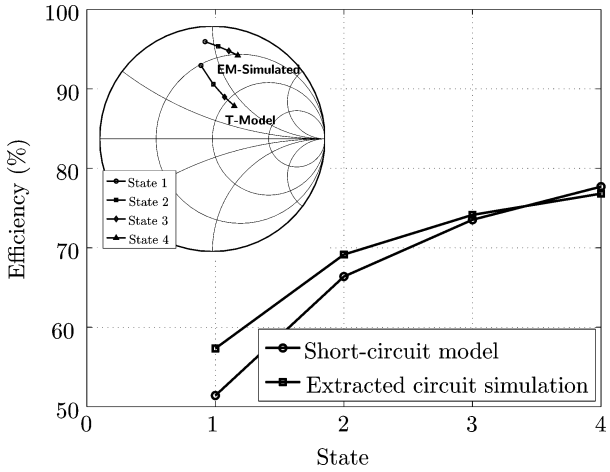

Fig. 21. Efficiency of circuit combiner and model. Inset: Input impedance of the system using the T-model, EM-simulated transformer and the extracted circuit. Normalized to $R_L/n^2 = 3.125\Omega$.

$0.4+j2.8\Omega$ and $1.1+j4\Omega$. This is a direct result of the nonzero real component of Z_{12} and Z_{21} that is not taken into account in the T-model.

C. Discussion of the Analysis Results

This analysis has shown that the efficiency of a transformer-based series power combiner with a series capacitor is a function of both the mutual quality factor Q_M and the scaling parameter K_3. Without the capacitor, the efficiency is degraded further by the finite quality factor of the secondary.

The following summarizes several characteristics of transformer-based series power combiners that are extracted from the analysis in Section V.

1) The scaling parameter K_3 models both the scaling of elements and the operation when elements are turned on and off, showing that the two produce equivalent behavior. For a unary system with all elements on, K_3 is unity and decreases to 0 as elements are shut off, resulting in a drop from optimal efficiency. However, $K_3 < 1$ for a nonunary system, resulting in a less than optimal efficiency.
2) For a unary combiner, elements can be added without a degradation in efficiency. However, adding scaled elements will reduce the maximum combiner efficiency. Further, adding elements to a unary system results in a monotonic increase in the PCR, but, because of the reduction in efficiency when scaled elements are added, a maximum PCR will be reached with a certain number of elements, depending on the mutual quality factor Q_M.
3) When designing a transformer for the power combiner, the optimal reactance of the secondary winding must be targeted. However, the model shows that the efficiency does not vary significantly with the variation in this reactance. Therefore, designing a transformer with nonoptimal reactance may improve system efficiency if a greater quality factor can be achieved.
4) When an element is turned off, the primary terminals of the transformer can be shorted or open-circuited. If the transformer is lossless, either choice will be acceptable. However, if the transformer is lossy, shorting the primary terminals will provide a lossy current path that will be coupled to the secondary, resulting in added loss to the system. If the terminals are left open, no current can flow and so no losses will be coupled to the secondary winding, maintaining efficiency. This may also affect amplifier choice, considering the output impedance.

Power combining with several discrete elements that are switched off at back-off power levels can improve efficiency, similar to discrete envelope tracking where the supply voltage is switched to discrete levels following output power requirements. Thus, the multielement combiner can theoretically eliminate the need for a supply modulator with the efficiency limitations and circuit complexity associated with it, provided that sufficient number of combining elements are utilized. Hybrid parallel and series combining can also be used to overcome the die area limitation of series combining. As seen in Fig. 12, a combiner with $Q_M = 100$ and $N = 4$ suffers 15% drop in efficiency as the power combiner changes from maximum power state (all element are on) to minimum power state, which is equivalent to 12 dB back off power. This can be compared to recently published results on various types of supply modulators, presented in Table I, which shows approximately 30%–40% drop in efficiency for the same back-off power. Considerable out-of-band emission due to aliasing and quantization noise can result from the digital envelope modulation approach due to the switching of combining elements as the output power is varied, but can addressed using techniques such as L-fold interpolation [30] or over-sampling [22].

VIII. Conclusion

Transformer-based series power combiners are analyzed for reconfigurable, high-power, wideband integrated envelope-tracking amplifiers. A high-level model for series power combiners is developed and is applied to a transformer implementation that incorporates losses, scaling, and switching effects. An optimum combining efficiency is derived for the combiner with arbitrary scaling of the input power sources. Based on this model, a four element 29.5 dBm power amplifier with 31% efficiency is designed and simulated in IBM 130-nm CMOS process. The amplifier maintains an output power $>$25 dBm over 700 MHz from 1.8 GHz to 2.5 GHz. The efficiency drops to 14% at 12 dB power back-off when elements are turned off. The studies presented in this paper can be extended to any series combiner implementation and any frequency range, which can be effective in the design of watt-level power amplifiers in submicrometer CMOS technologies.

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