A 150MHz, 84% efficiency, Two Phase Interleaved DC-DC Converter in AlGaAs/GaAs P-HEMT Technology for Integrated Power Amplifier Modules

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***Abstract*—This paper presents a high efficiency, high switching speed, two-stage interleaved DC-DC buck converter with negatively-coupled inductors in AlGaAs/GaAs technology, targeting integrated power amplifier modules. The flip chip DC-DC converter is implemented in 0.5 μm GaAs pHEMT process and occupies $2 \times 2.1mm^2$ without the output network. The inductors in the output network are implemented in 65 μm thick top copper metal layer and have a quality factor of 25 at 150 MHz. The interleaved DC-DC converter achieves 84% efficiency when operating at 150MHz switching frequency with 4.5V/3.3V conversion ratio and 1A load current.**

***Index Terms*—Gallium Arsenide Technology, p-HEMT, interleaved DC-DC converters, coupled inductors, conversion efficiency, supply modulators.**

I. Introduction

Mobile communication systems utilizing non-constant envelope modulation, require highly linear power amplifiers. To meet the stringent linearity requirements, the power amplifier (PA) typically operates in "back-off" power mode, leading to lower efficiency. Transmitter architectures such as envelope tracking and polar modulation have been developed to enhance the efficiency at back-off power, by modulating the supply voltage of the PA. High efficiency, small size, high modulation bandwidth, and multi-mode operation are the main requirements of supply modulators in mobile applications. Different types of supply modulators include switched-mode DC-DC converters, linear regulators, and hybrid-solutions that combine both functionalities. While switched-mode DC-DC converters can provide the highest efficiency, their reported bandwidth in silicon technologies have been limited due to the gate charging and switching losses of the employed field effect transistors (FETs).

This paper proposes the use of GaAs technology for the implementation of switched-mode, high efficiency, DC-DC converters targeting GSM/EDGE applications with their relatively high voltage, high current requirements. Given that GaAs is the most popular technology for power amplifier implementations, it is natural to integrate the supply modulator with the PA in the same technology. It has been previously shown that GaAs P-HEMT based switching transistors have a lower switching figure of merit compared to silicon MOSFETs for the same voltage range [1]. In this paper, we demonstrate a flip-chip integrated 150MHz, two phase interleaved DC-DC converter with negatively coupled inductors in the output filter network. The DC-DC converter achieves 84% maximum efficiency for 1A load current and 4.5/3.3V ratings. Section II discusses the advantages of coupled inductors in terms of the steady state and transient performance of the DC-DC converter. Section III provides the details of the circuit implementation. Measurement results are presented in section IV, while conclusions are drawn in Section V.

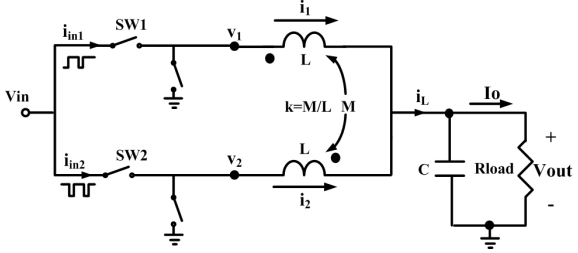

Fig. 1. Ideal interleaved topology with negatively coupled inductors.

II. Analysis of Interleaved Topology with Coupled Inductors

Increasing the switching speed and the use of interleaved architectures in DC-DC converters have been shown to reduce the values of filter inductors by more than 50% [2], [3], [4], [5]. In this section, we study the effect of introducing coupling between the filter inductors in two phase interleaved converters on the steady state current ripple and the system bandwidth.

A. Steady State Analysis

Fig. 1 shows conceptually the core interleaved structure with coupled inductors, where M is the mutual inductance between the two phases. Here, we assume that the two branches have equal inductances L and $k = M/L$, where k is the coupling factor. Following the analysis presented in [5], [6], the steady state current ripple per phase in the inductor for duty ratios larger than 0.5 can be given by:

$$\Delta i_1 = \frac{V_{in}(1-D)(\frac{D}{1-D}+k)}{L(1-k^2)} \cdot (1-D)T \qquad (1)$$

Where V_{in} is the input voltage and D is the duty cycle. Fig. 2 shows Δi_1 as function of coupling factor for different duty cycles assuming an input voltage V_{in} of 4.5V, a switching frequency of 150MHz and a filter inductor of 8nH. As can be seen from the figure, the coupling factor that results

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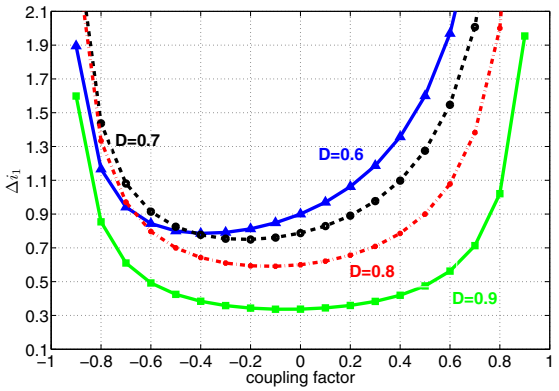

Fig. 2. Current ripple versus inductors' coupling factor for different duty cycles.

in minimum current ripple is a function of the duty ratio. However, one can make the statement that a negative coupling factor between -0.2∼-0.4 would generally result in lower current ripple, while positive coupling increases the ripple beyond the uncoupled case. A higher current ripple results in larger inductor loss, which lowers the efficiency of the DC-DC converter. In the given example of 4.5/3.3V conversion ratio, the optimum coupling factor for minimum current ripple is around -0.3.

B. System Stability and Transient Response

Considering the transient response, the open loop transfer function $\frac{v_o(s)}{d(s)}$, where $d(s)$ is the small signal function of duty ratio D, can be derived from the inductor current and capacitor voltage as in (2), following the analysis described in [7], while including the dc resistance of the inductors.

The small signal transfer function for different coupling factors is plotted in Fig. 3. The figure compares the bandwidth and phase margin of non-coupled, positively coupled and negatively coupled inductors in two phase interleaved converters. Negatively coupled inductors increase the bandwidth by 29.2% compared to non-coupled inductors, and 52.7% compared to positively coupled inductors for the case of $k = \pm 0.4$. Thus, it is evident from the discussion above that negative coupling can improve both the steady state and transient response, by reducing the current ripple and increasing the bandwidth of the DC-DC converter. However, optimum ripple cancellation depends on the selected coupling factor, which varies for different duty cycles. To achieve the best ripple cancellation, the coupling factor should be selected according to Fig. 2.

III. Circuit Implementation

A prototype of the interleaved DC-DC converter is designed for 4.5V to 3.3V conversion, 1A load current, in a three metal

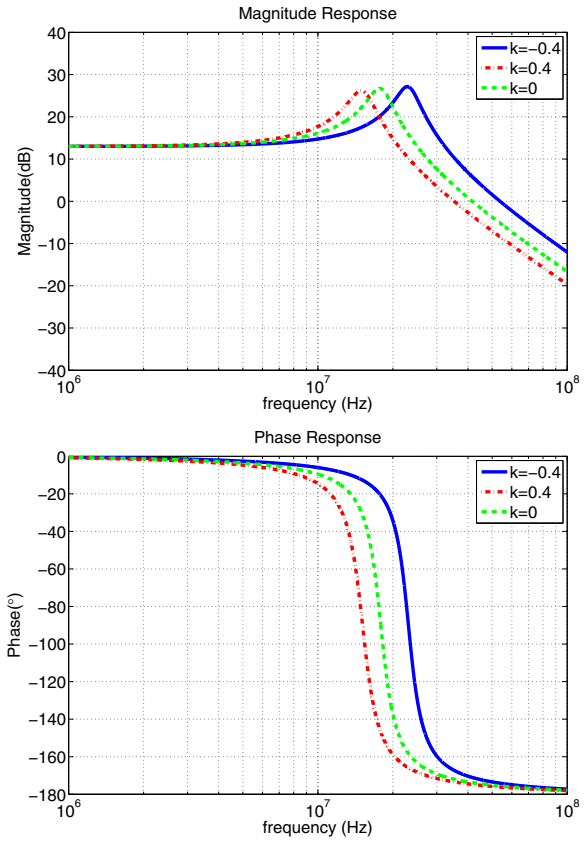

Fig. 3. Open loop transfer function for different coupling factors.

layer 0.5 μm GaAs p-HEMT process with both depletion and enhancement mode p-HEMT devices. The coupled inductors are implemented in 65 μm top copper layer. The circuit diagram of the converter is shown in Fig. 4.

A. Output Stage and Gate Driver Design

Two loss mechanisms are encountered in the switching stage; the switching loss and the conduction loss. Fig. 5 shows the variations of both losses as a function of the switching transistor width for 4.5V to 3.3V conversion ratio. The sizes of the high side switches are selected at the point where the conduction loss equals to the switching loss to achieve maximum efficiency. It is important to include the gate driver losses with the overall losses when sizing the switching transistor. For 1A output current and the required voltage conversion ratio, the widths of SW1 and SW2 are chosen as 10mm. M3 and M4 provide a path for the current when SW1 and SW2 are off and they are sized at the same width as SW1 and SW2.

Given that there are no complementary devices in the used technology, the supply voltage of the gate driver needs to

$$\frac{v_o(s)}{d(s)} = \frac{\frac{2V_{in}}{C(L+M)}(s+\frac{r_L}{L-M})}{s^3+(\frac{1}{R_{load}C}+\frac{2Lr_L}{L^2-M^2})s^2+(\frac{2Lr_L}{R_{load}C(L^2-M^2)}+\frac{r_L^2}{L^2-M^2}+\frac{2}{C(L+M)})s+(\frac{r_L^2}{R_{load}C(L^2-M^2)}+\frac{2r_L}{C(L^2-M^2)})} \quad (2)$$

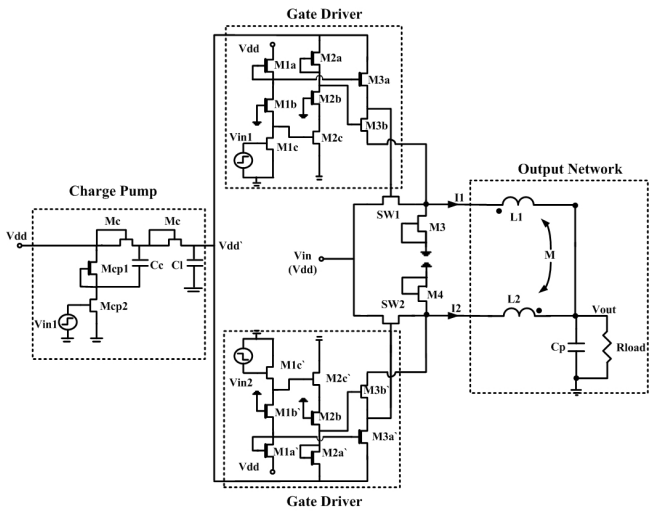

Fig. 4. Circuit topology.

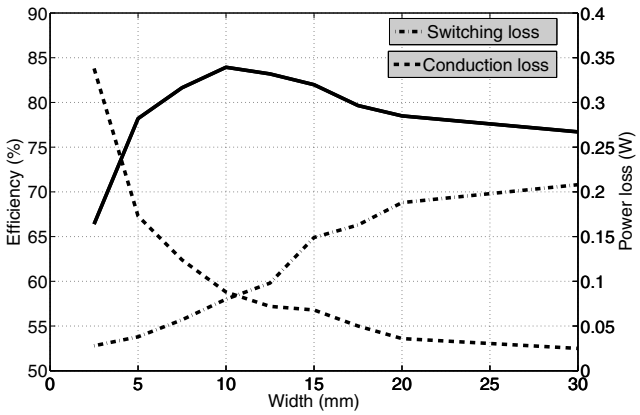

Fig. 5. Transistor loss and efficiency versus transistor size.

be higher than the supply voltage of the converter to drive the high side switches. The minimum value of gate driver supply voltage is $V_{dd} + V_p$, where V_p is the pinch off voltage of the enhancement mode p-HEMT. A single stage Dickson charge pump is adopted to increase the supply voltage. The gate driver stage is a two-stage active inverter with the second stage referenced to the source of the high side switches. The second inverter stage is designed as pseudo complementary switches with high side depletion mode HEMT and low side enhancement mode HEMT. The first two stages generate the gate control signals of the M_{3a} and M_{3b} separately. The sizing of the gate driver stages is a tradeoff between reducing the gate driver losses and enhancing the driving capability for the high side switches, which affects the switching loss of SW1 and SW2. The enhancement mode pHEMT M_{3b} is the main switching transistor, and its width is chosen as $1/10$ of the high side switch SW1, while M_{3a} is sized as 1/3 of M_{3b}.

B. Inductor Design

The coupled inductors must be properly selected to achieve an optimal balance between the required inductance value

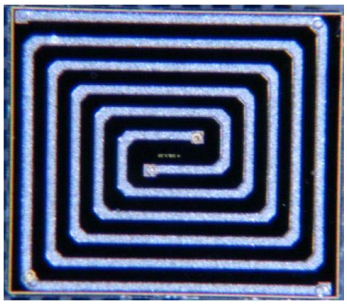

Fig. 6. Die photo of coupled inductors.

at the given switching speed and a low series resistance to minimize the losses. The size of inductors is set according to the switching frequency, output current level and current ripple requirements. The maximum current ripple can be defined at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM), which is the point at which the steady state current ripple Δi_1 equals to the load current I_o [6]. Hence, using (1), the minimum required inductor can be defined as:

$$L_{min} = \frac{V_{in}(\frac{D}{1-D} + k)(1-D)^2}{(1-k^2) f_{sw} I_o} \tag{3}$$

The minimum inductor for the given circuit specifications is 6.28nH. Fig.6 shows the die photo of the coupled inductors, implemented using the interleaved topology and fabricated in 65 μm copper layer. The electromagnetic simulation results of the coupled inductors are shown in Table I.

TABLE I
INDUCTOR PARAMETERS

Area	$2.3 * 2.7mm^2$
Width	60 μm
Turns	2.75
Spacing	140 μm
L	6.28nH
R_{dc}	0.055 ohm
k	0.3
$Q_{at150MHz}$	25

IV. MEASUREMENT RESULTS

The circuit shown in Fig. 4 is designed at 150MHz with 6.28nH coupled inductors and 20nF load capacitor. The circuit converts 4.5V input to 3.3V output with 1A output current. The duty cycle is 0.65 and the coupling factor is -0.3. The die micrograph is shown in Fig. 7. The converter die and coupled inductors are flip chip bonded to a PCB board. The area of the converter is $2 \times 2.1mm^2$. The interleaved DC-DC converter is tested using an external pulsed source, provided by Agilent B1110A. The transient response is measured using HP Infinium 1.5GHz Oscilloscope. Fig. 8 shows the transient response of the output voltage. It is worth noting that the relatively high measured output voltage ripple of 112 mV, which is 2 times higher than the simulated value, is due to the deviation of implemented inductors from the target values of inductance and coupling factors for maximum ripple

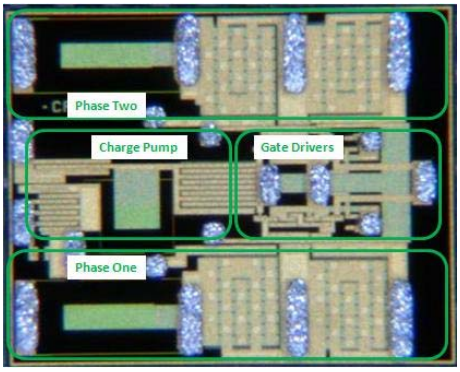

Fig. 7. Die photo of DC-DC converter.

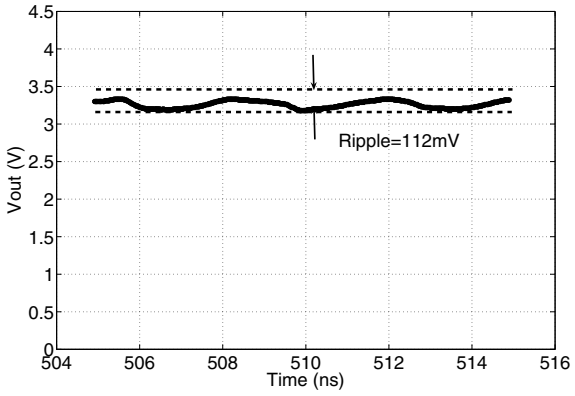

Fig. 8. Output transient response.

cancellation (the implemented inductors have a value of 8.7nH and a coupling factor of 0.46 compared to the target values of 6.28nH inductance and 0.3 coupling factor).

The measured efficiency for 4.5V input, 1A output current at 150MHz switching frequency with varying duty cycle is plotted in Fig. 9. The efficiency at the target conversion of 4.5V/3.3V is 83.8%. For duty ratios between 0.2 to 0.8, the efficiency variations are around 30%, which can be improved by using synchronous rectifiers and adding control techniques such as adaptive dead-time control. The efficiency is maintained over a wide range of output current as seen in Fig. 10.

V. Conclusion

A high efficiency, high switching frequency interleaved DC-DC converter with negatively coupled inductors has been demonstrated in 0.5μm, p-HEMT GaAs technology. GaAs technology provides a faster switch with lower on-resistance and smaller parasitic capacitance compared to CMOS technology. The interleaved converter achieves a peak efficiency of 84% at 150MHz with 4.5V/3.3V conversion ratio and 1A load current. This work demonstrates the potential of GaAs technology to extend the efficient operation of switching supply modulators to the hundreds of MHz, ultimately enabling fast tracking and multi-mode operation of integrated GaAs power amplifier modules.

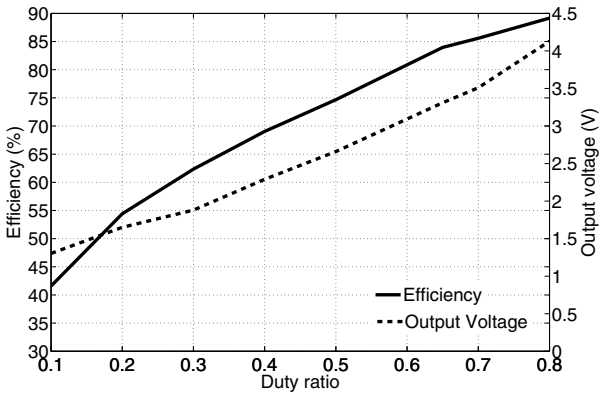

Fig. 9. Efficiency and output voltage at varying duty cycle.

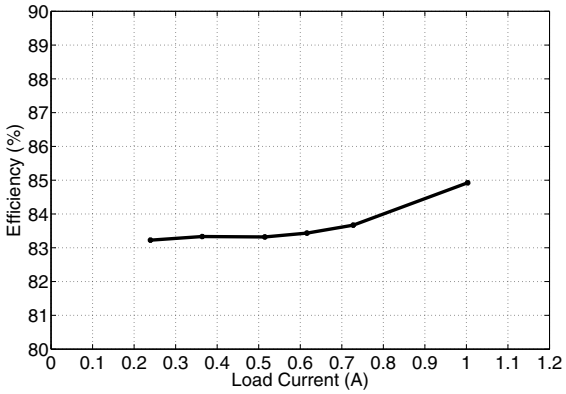

Fig. 10. Efficiency at different load currents.

VI. Acknowledgement

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