Frequency synthesiser architecture eliminating high speed frequency dividers for millimetre-wave applications

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A frequency synthesiser architecture for millimetre-wave applications is proposed. The architecture is based on a triple-push oscillator, which functions both as a divider and oscillator. Thus, the proposed architecture eliminates the need for injection locked frequency dividers that are the main contributors to the limited tuning capability of millimetre-wave phase-locked loops. Since the proposed architecture is solely based on the performance of the triple-push oscillator, the measurement result of the first silicon triple-push oscillator at 30 GHz is presented to support the validity of the concept.

Introduction: The recent move from the lower GHz frequency range to millimetre (mm)-wave frequencies (60 GHz band) offers 7 GHz of bandwidth for high data rate communication. For the frequency synthesiser, the large bandwidth feature requires wider tuning range oscillators and high speed frequency dividers to cover the whole 7 GHz of bandwidth. Fig. 1 shows a typical mm-wave frequency synthesiser architecture, which is generally identical to low frequency synthesisers except for its frequency divider. Given the speed limitation, traditional frequency dividers are replaced with injection locked frequency dividers (ILFDs) [1, 2] immediately after the voltage-controlled oscillator (VCO) as shown in Fig. 1. Although the ILFD is intrinsically an oscillator whose oscillation frequency is f_{ILFD}, it can be treated as a mixer in a given phase-locked loop (PLL). For this analogy, the ILFD acts as a downconversion mixer with a LO frequency f_{ILFD} and RF frequency f_o ($\approx 2 \times f_{ILFD}$) [3]. The resulting downconverted signal has an approximate frequency of $f_o - f_{ILFD}$, and can be subsequently divided using other divider circuits (e.g. Miller dividers).

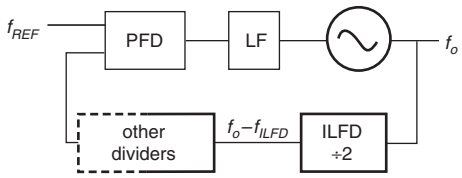

Fig. 1 *Traditional mm-wave frequency synthesiser architecture*

To date, the ILFD is the circuit of choice for implementing frequency dividers in mm-wave synthesisers. However, finite locking range and matching the tuning requirements of the VCO and IFLD have limited the achievable tuning range in mm-wave synthesisers (0.5% at 75 GHz [1], and 3.33% at 60 GHz [2]). Fig. 2 graphically illustrates the limitations of ILFDs. ILFD dividers intrinsically have a very narrow locking range with respect to the VCO's tuning range. Thus, the frequency synthesiser's tuning range is determined mostly by ILFD's locking range rather than the VCO's tuning range (Fig. 2*b*). Another problem arises from f_o ($\approx 2 \times f_{ILFD}$) and f_{ILFD} interaction. If f_{ILFD} is not exactly achieved due to PVT, this would result in either locking failure or very low tuning range as illustrated in Fig. 2*c*.

Proposed architecture: The proposed architecture is shown in Fig. 3. The frequency synthesiser employs a triple-push VCO instead of a single fundamental oscillator. The outputs of three fundamental oscillators that oscillate at $f_o/3$ are combined and the third harmonic at f_o is obtained as the output signal from the frequency synthesiser. While the output is at frequency f_o, the loop is closed with the frequency component at $f_o/3$, which is the output of any of the fundamental oscillators. For proper triple-push oscillator operation, each fundamental oscillator should have the same amplitude with a $2\pi/3$ phase difference between fundamental components [4]. Interestingly, these conditions are similar to a three-stage ring oscillator that is used as an ILFD divider, which shows that a triple-push oscillator can be used as a divide-by-three circuit as well. Note that a three-stage mm-wave ring oscillator is based on a time delay mechanism rather than an *n*th frequency harmonic addition/subtraction as the case of the triple-push VCO. Apart from the difficulties in implementing ring oscillators at mm-wave frequencies, a triple-push VCO which has LC oscillators as fundamental oscillators would outperform any delay-based ring oscillator in terms of phase noise performance.

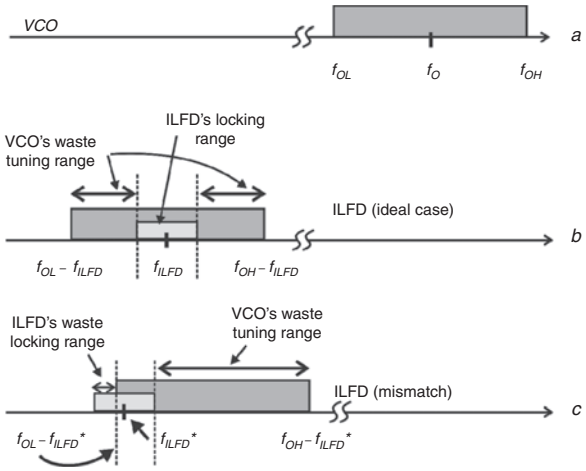

Fig. 2 *Effect of limitations of ILFD on tuning range performance of mm-wave frequency synthesisers*

a VCO's tuning range
b Tuning range reduction due to ILFD limited locking range
c Tuning range reduction due to mismatch between oscillation frequencies of ILFD and VCO

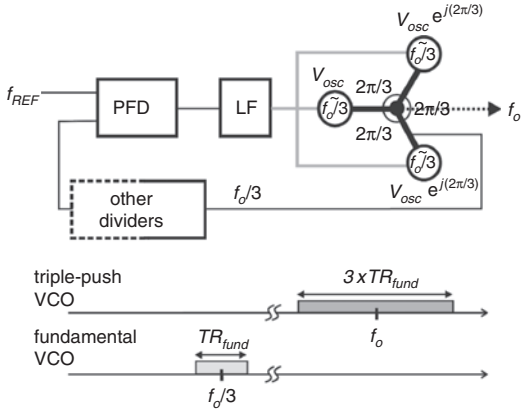

Fig. 3 *Proposed mm-wave frequency synthesiser architecture using triple-push oscillator*

Compared to ILFD-based synthesisers, the proposed mm-wave frequency synthesiser based on triple-push oscillators (or in general any *n*th push oscillator) offers the following advantages:

1. The triple-push VCO works both as an oscillator and divider, eliminating the need for mm-wave frequency dividers such as an ILFD.
2. Since the division process is intrinsically part of the oscillation process in triple-push oscillators, it is impossible to lose tuning range because of limited locking range as in the case of Fig. 2*b* or suffer from any mismatch between locking and tuning ranges as in the case of Fig. 2*c*.
3. For a mm-wave frequency synthesiser employing a triple-push oscillator generating a signal f_o, the output of the fundamental–oscillator/divider circuit is at $f_o/3$. Thus a traditional static divider can easily be employed rather than a Miller divider which suffers from a limited bandwidth compared to static dividers. Note that static dividers are reported up to 25 GHz in mainstream CMOS technologies with reasonable power consumption [5].

Feasibility of CMOS triple-push oscillators: The stability and performance of the proposed architecture in Fig. 3 depend solely on the accurate design of the triple-push VCO. Harmonic oscillators such as triple-push oscillators are based on combining multiple fundamental–oscillator units to boost the second, third, or fourth harmonics. For manufacturability, matching between the oscillator units is crucial to guarantee functionality and acceptable levels of suppression to all the other harmonics. At mm-wave frequencies and above, matching can be even

more critical owing to the effects of interconnects and smaller feature sizes for active devices. The matching of three fundamental oscillators is crucial to meet the phase condition for triple-push operation and to have a high output power at f_o with much lower power at $f_o/3$ [4].

To test the feasibility of mm-wave CMOS triple-push oscillators, we have fabricated and tested a 30 GHz VCO in a 0.13 μm CMOS technology. The triple-push oscillator (TPO) shown in Fig. 4 is realised using three Colpitts oscillator units with their outputs combined via on-chip gain-boosted buffers. The sensitivity of fundamental and second harmonic rejections to matching conditions were characterised by performing Monte Carlo simulations, where the steady state output power spectrum of the VCO is obtained by setting up SpectreRF PSS and 50 mismatch simulations were run for the oscillator. The third-harmonic amplitude varied from −11.8 to −12.8 dBm with the maximum number of occurrences around −12 dBm, while the fundamental amplitude varied from −22 to −40 dBm with the maximum number of occurrences around −32 dBm. The TPO is also experimentally characterised using a Cascade RF probe station and Rohde-Schwarz FSP 40 GHz spectrum analyser. Our initial experimental results show that triple-push oscillators are feasible at mm-wave frequencies in today's deep submicron CMOS technologies with a good output power and fundamental rejection performance. The VCO delivers an output power up to −3 dBm with a maximum measured fundamental rejection performance of −18.6 dBc. Fundamental rejection performance deviates from −18 to −14 dBc as the output power scales. Fig. 5 shows the measured output spectrum when the output power is set at −14 dBm. The measurements were also repeated on several dies to assess sensitivity to matching and process variations. Similar results were obtained within +/−2.5% deviation from simulations. To the best of our knowledge, this is the first triple-push VCO on silicon and the highest fundamental rejection performance reported among published non-silicon integrated triple-push VCOs [4, 6] to date.

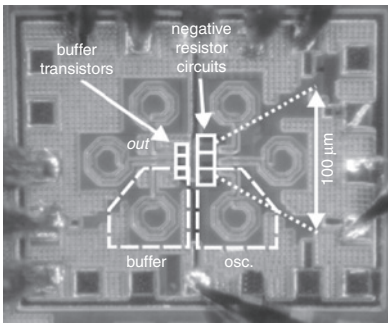

Fig. 4 *Die photo of CMOS triple-push VCO*

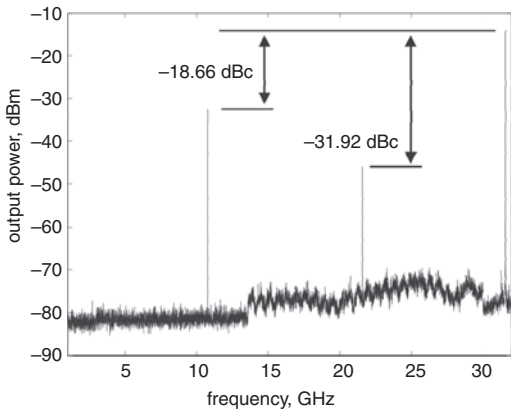

Fig. 5 *Measured output spectrum of CMOS triple-push VCO at 30 GHz*

Conclusion: A mm-wave frequency synthesiser architecture without an ILFD is proposed. The advantages of the proposed architecture are discussed. The experimental study of a CMOS triple-push oscillator, on which the architecture is based, is presented to support the validity of the proposed architecture.

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