A 30-GHz Triple-Push Oscillator on Silicon for mm-wave Applications

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***Abstract*—Methodologies for a manufacturable design, and layout optimization of voltage controlled oscillators in triple push architectures for mm-wave applications, are proposed. The techniques are applied in the design of a fully-monolithic 30GHz triple push oscillator in 130nm CMOS technology.The oscillator provides an output power up to 0dBm with a maximum fundamental harmonic suppression of -18.66dBc and second harmonic suppression better than -30dBc. To the authors' knowledge, this is the first triple push oscillator on silicon and the highest levels of harmonic rejections reported for integrated triple-push oscillators.**

I. Introduction

The quest for low cost integrated solutions to high data rate applications, has increased the interest in wide bandwidth communications systems operating in the millimeter-wave range. With f_T of CMOS technology reaching the limits of 280GHz (expected in 45nm process), CMOS has already proven its capability in terms of functionality and performance to operate in the mm-wave band approaching THz limits. Oscillators operating at such high frequency ranges are either implemented as fundamental-mode oscillators, or harmonic based oscillators (push-push, triple-push, etc). Fundamental mode oscillators require f_{max} of the device to be substantially higher than the required frequency of oscillation with sufficient available power gain at nominal operating frequency. Harmonic oscillators on the other hand allow for extended operating frequencies from the active device in addition to wider tuning range capability.

Harmonic oscillators are based on combining multiple fundamental-oscillator units to boost the second, third, or fourth harmonics. For integrated oscillators satisfying design for manufacturability (DFM) constraints, matching between the oscillator units is crucial to guarantee functionality and acceptable levels of suppression to all the other harmonics. For mm-wave frequencies and above, matching can be even more critical due to the effects of interconnects and smaller feature sizes for active devices. While push-push oscillators have been demonstrated in CMOS for frequencies up to 192GHz [1] and tuning ranges up to 15% [2], triple-push oscillators (TPO) can even achieve higher frequencies but have only been reported using discrete devices and III-V technologies [3]-[5]. To the best of our knowledge, our paper is the first to address implementation issues associated with silicon triple-push oscillators for a manufacturable design. We will analyze and experimentally validate the effect of matching between core oscillator cells on the output power level as well as first and second harmonic rejection performance.

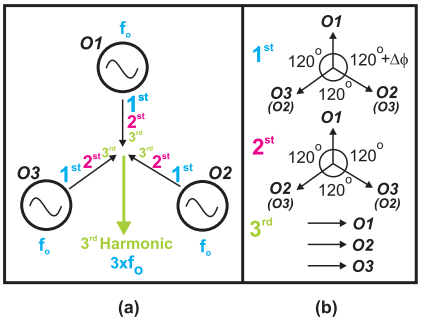

Fig. 1. Conceptual Triple-Push VCO and vector expressions of fundamental and harmonic components

II. Principle of Operation and Matching Considerations

The conceptual diagram of a triple-push oscillator (TPO) is shown in Fig. 1(a). It is formed of three identical fundamental oscillators, whose outputs are connected to a common load. The mathematical formulation for triple push oscillators was reported in [3] using three port Z-parameter representation. The analysis of the Z-parameter matrix equation gives one even mode and two odd modes for steady state operation. The odd modes can be vectorially represented as shown in Fig. 1(b). Since the fundamental components are separated by 120^o and second harmonic components have 240^o phase shift, they cancel each other when combined at the output. However, the third harmonic components are in phase because of the 360^o phase shift, and are added together, boosting the third harmonic's power.

Although the fundamental and second harmonic components are ideally canceled at the output, this is only true for exact phase shifts of 120^o between the oscillator unit cells and as long as the output power of these unit cells are equal. In other words, any power or phase mismatch between the three fundamental oscillators would result in lower third harmonic power and less fundamental and second harmonic rejection.

To illustrate the effect of phase mismatch, the output powers at the fundamental, second, and third harmonics of a TPO are plotted as function of the phase error between the three fundamental oscillator units while assuming equal output

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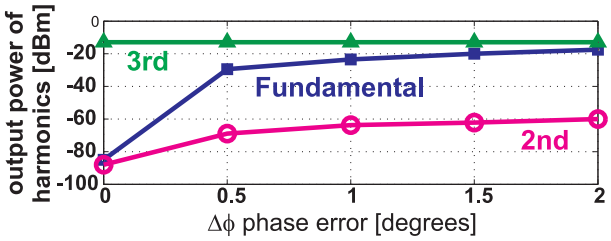

Fig. 2. Fundamental and harmonics power levels as a function of phase error

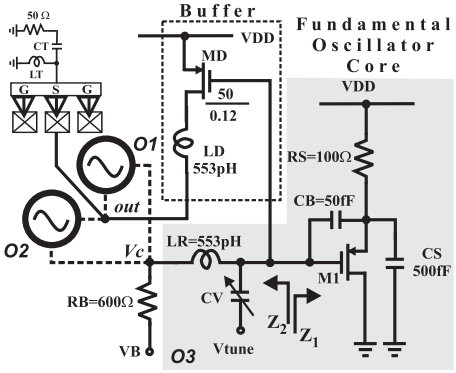

Fig. 3. Transistor level schematic of fundamental VCO in triple-push architecture

powers. Fig. 2 shows the deviation of harmonics powers and fundamental suppression performance as a function of phase error $\Delta\Phi$. It is evident from the figure that steep degradation in the fundamental suppression is observed for phase errors as small as 0.5^o, which clearly reflects the importance of matching in the design of triple-push VCOs.

III. Triple Push Oscillator Design

A. The Core

The transistor level schematic of the fundamental VCO in the triple-push architecture is shown in Fig. 3. A capacitively degenerated stage is used as negative resistance cell. The current feed for the core VCO cell is realized with a metal resistor, RS. The resonator is formed of an LC tank (LR and CV in Fig. 3). The octagonal inductor (LR) is created by shorting top two metals of the process with vias along the spiral. It has a diameter of 120μm and 2 turns. The number of turns is selected as an integer to facilitate routing. The gate bias to all fundamental units is provided through an n-well resistor, RB whose value is selected to suppress undesired even mode oscillation. PMOS transistors are used for both negative resistance cell and buffer designs due to their outperforming noise performance compared to that of NMOS transistors in the used process. The aspect ratio for M1 is selected roughly equal to 150μm/0.12μm. However, the size of M1 will be varied to generate multiple designs and provide an assessment to the sensitivity of circuit performance to exact device sizes as explained in Section III(c).

To guarantee that even mode oscillation is suppressed, the impedance characteristics of the fundamental oscillator for

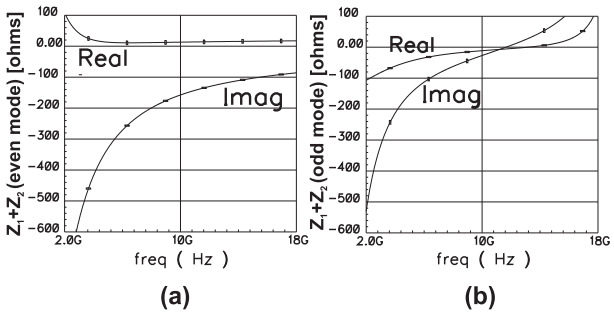

Fig. 4. (a) Even and (b) odd mode impedance characteristics of fundamental VCO in triple push oscillator architecture.

even and odd modes is plotted in Fig. 4. The simulation results in Fig. 4 show that the real part of impedance for even mode is always positive (no possible oscillation), while odd mode oscillation occurs at 11.6 GHz for the design shown in Fig. 3

B. Buffer Design

Triple-push oscillators (TPO) can provide higher Q-factor resonator and sufficient device gain since they rely on a core operating at one-third the desired frequency. However the levels of output power are normally low because of the relatively low power of third harmonic. To boost the output power level of the designed TPO, the three fundamental oscillator units are connected to a common output load via an optimized buffer stage. The buffer, a simple inductor loaded common source amplifier, is shown in Fig. 3 in dashed box. Inductor LD is used to minimize the effect of loading introduced by the buffer on the core cells and would ultimately lead to doubling the amplitude of the signal at the output. The value of LD is chosen equal to the core inductor LR to provide a symmetrical layout and minimize any possible mismatch between individual oscillator units.

C. Design Strategy

The matching of the three fundamental oscillator units in a typical TPO is crucial as illustrated in Fig. 2. Careful floor-planning is required to guarantee identical oscillators and symmetrical interconnects. Similarly, the matching of the transistors have utmost importance to minimize phase and amplitude mismatches. In this section, the strategy developed to evaluate transistor level matching issues are discussed while floor-planning is addressed in the next section.

MOS transistors in general have poor matching properties compared to their bipolar counterparts. Typical matching strategies by increasing the channel length beyond minimum feature size is not an option at mm-wave frequencies. Increasing the channel width is a possibility that comes at the expense of increasing the gate resistance and thus higher phase noise for the oscillator. To evaluate the trade-off between matching and phase noise analytically and experimentally, several channel widths were selected for the finger width of M1 (the main transistor in the core oscillator in Fig. 3). Three different triple push oscillators (TPOs) were designed using

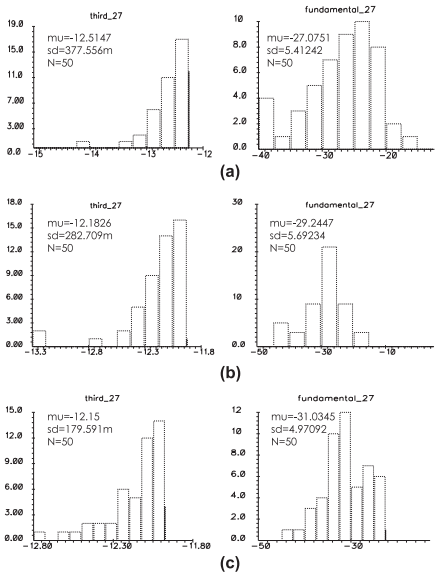

Fig. 5. Monte Carlo mismatch simulations of the fundamental and third harmonic power for 3 different version of TPO (a)W=480nm, (b)W=1μm, (c)W=2μm

the variable channel widths according to Table-I. Note that the aspect ratio of M1 is almost constant for the three versions of the TPOs. The layout of the oscillator and buffer transistor size are also kept constant. Since the actual fundamental

TABLE I
TPO DESIGN PLAN

TPO name	Finger Width [nm]	# of Fingers	# of Transistors	Effective Width [μm]
W480n	480	80	4	153.6
W1000n	1000	75	2	150
W2000n	2000	75	1	150

and second harmonic rejections are based on matching, Monte Carlo simulations were performed to evaluate the sensitivity of the design to transistor matching. The steady state output power spectrum of the VCO is obtained by setting up SpectreRF PSS and 50 mismatch simulations were run for each oscillator. The simulation results are shown in Fig. 5. As the channel width increases from 480nm to 1000nm, expected harmonic suppression improves from -14 dBc to -18 dBc. However, scaling the width to 2000nm does provide a marginal improvement on the rejection performance.

IV. Implementation and Experimental Results

A. Floorplan of the VCO

Because matching is one of the most important design parameters, the layout of the VCO should be designed accordingly. In addition, for mm-wave operation, the layout should be as compact as possible to reduce parasitics. The chip micrograph of the designed VCO is shown in Fig. 6. The VCO core occupies an area of 590μm x 420μm. The fundamental oscillator cores and the buffers are grouped

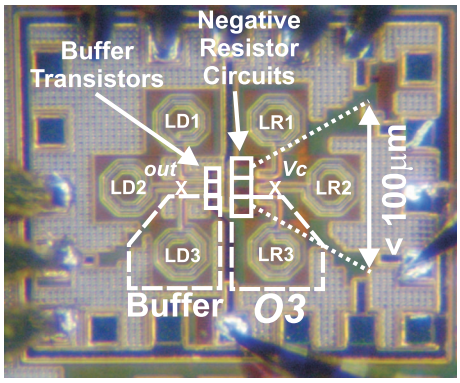

Fig. 6. Physical design and die micrograph of the TPO.

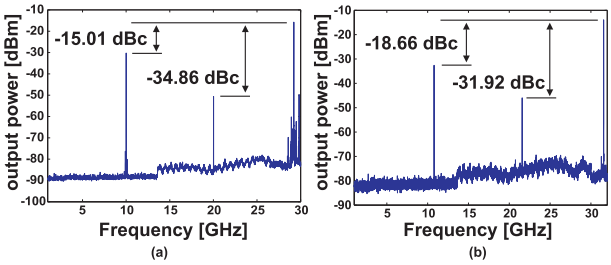

Fig. 7. Measured output spectrum of two triple push oscillators a) W480n b) W2000n

together to maintain symmetry. The two common mode points (***Vc*** and ***out*** in Fig. 3) are crucial in sustaining odd mode operation and are located on each side of the vertical axis. These points are shown by "X" in Fig. 6. The active part of buffer and fundamental oscillator core are put side by side and the required interconnects are minimized. Finally, the MOS transistors are laid out in the same direction and in a compact way such that the longest distance between the transistors is less than 100μm to improve matching.

B. Experimental Results

The triple push oscillator is implemented in 0.13μm IBM CMOS technology. Three layouts were generated as in Table-I. All the fundamental cells in the implemented TPO share the same supply lines. Similarly, the buffer cells have a separate but common VDD supply. The TPO is characterized with a Cascade RF probe station and Rohde-Schwarz FSP 40GHz spectrum analyzer. The common output of the buffers are connected to DC ground via an off-chip bias-tee as shown in Fig. 3. The measured output spectrums for TPOs versions W480n and W2000n are shown in Fig. 7. A fundamental oscillation around 10 GHz is observed while the third harmonic is around 30 GHz. The fundamental rejection for the TPO version (W480n) is -15dBc while that for TPO version (W2000n) is -18.66 dBc. 3.66 dB improvement can be attributed to larger channel width and improved matching.

To observe the reliability of harmonic suppression, the output power of each version was changed from -22dBm to -2dBm with a constant 5dBm step. The measurement results

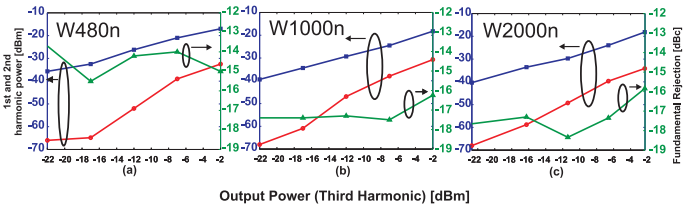

Fig. 8. Measured output power of fundamental,second harmonic and fundamental rejection performance as a function of output power of the VCOs (third harmonic power) a) W480n b) W1000n c)W2000n

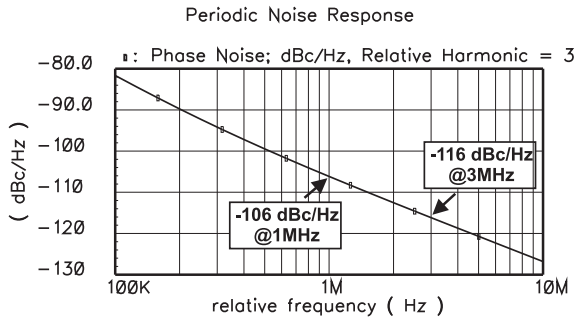

Fig. 9. Phase noise performance of the proposed TPO at 1 and 3 MHz offset from a 31.6 GHz carrier

show that each TPO's fundamental rejection performance deviates in a range of 1∼2dB. Also note that scaling the unit transistor's width from 480nm to 1000nm improves the harmonic rejection up to 3dB. However, as it can be seen from Fig. 8(b) and (c) any further increase in the channel width marginally improves the fundamental rejection performance.

The measurements presented above were repeated on several die samples and similar results were obtained. At this point, it is important to compare the simulation and measurement results. Table-II compares simulation and measurement results for fundamental rejection performance of the TPO operating around 30 GHz. There is a perfect agreement between simulated and measured results.

TABLE II
COMPARISON OF SIMULATION AND MEASUREMENT RESULTS FOR FUNDAMENTAL REJECTION PERFORMANCE ($P_{out} \approx$ -12dBm , $f_{out} \approx 30$ GHz)

VCO name	Fundamental Rejection (simulation) [dBc]	Fundamental Rejection (measurement) [dBc]
W480n	-14.56	-14.21
W1000n	-17.06	-17.5
W2000n	-18.88	-18.34

While phase noise measurement capability at 30GHz was not available, the simulated phase noise performance is plotted in Fig. 9. The reported phase noise simulations are taken under a total core current of 8.4mA, total buffer current of 11.35mA from a 1.2V supply, and an output power of -10.34dBm. The tuning range is 5GHz covering the frequency range from 26.6 to 31.6GHz.

Fig. 10 compares the measured fundamental rejection performance of a number of published TPOs with our design.

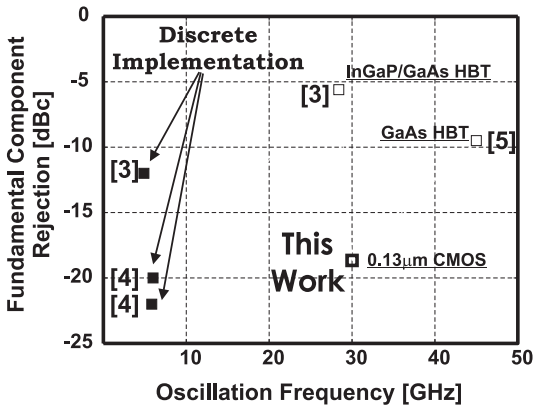

Fig. 10. Comparison of the fundamental rejection performance of the designed TPO with former work

The discrete TPO that operates around 6 GHz with on-board tuning, has the best fundamental rejection performance. On the other hand, the designed TPO at 30GHz outperforms all other integrated TPOs to date in terms of fundamental rejection performance for almost the same power levels and phase noise performance. Additionally, CMOS-based triple push oscillators, and harmonic-based oscillators in general can be employed in low cost mm-wave PLLs to act as both an oscillator as well as provide frequency division through internal access to the core oscillators [6], thus eliminating the need for high power consumption frequency division circuitry at mm-wave frequencies.

V. CONCLUSION

This paper reports the first silicon triple-push VCO for mm-wave applications. Design for manufacturability techniques and layout optimizations are discussed. The presented triple push oscillator has the highest fundamental rejection performance among integrated triple-push VCOs in other technologies reported to date. The best fundamental rejection performance measured is -18.66 dBc around 30 GHz. The fundamental rejection performance of the TPO has a flat characteristic as function of the output power level.

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