

# Triple-Push Operation for Combined Oscillation/Division Functionality in Millimeter-Wave Frequency Synthesizers

Burak Çatlı, *Student Member, IEEE*, and Mona Mostafa Hella, *Member, IEEE*

**Abstract**—This paper proposes the use of N-push operation for combining the functions of the VCO and divider in the mm-wave frequency range. If employed in a PLL, the combined VCO/divider (C-VCO/D) would potentially provide wider tuning range than traditional mm-wave PLLs employing injection locked frequency dividers, thus exploiting the full range available in the 60 GHz band (57 GHz–64 GHz). The behavior of triple push oscillators based on injection locking theory is analyzed to study their various oscillation modes, their stability and the effect of mismatch on the oscillator performance. Design guidelines are provided for boosting the third harmonic power at a given power budget. Using 130 nm IBM CMOS technology, multiple versions of the triple push oscillator are implemented and characterized. A 55 GHz–65 GHz tuning range is obtained using a 206 pH tank inductance and requires  $I_{\text{core}} = 20$  mA, and  $I_{\text{buffer}} = 15$  mA from a 1.4 V supply. For a tank inductance of 140 pH, a 63.2 GHz–72.4 GHz tuning range is obtained using  $I_{\text{core}} = 17$  mA, and  $I_{\text{buffer}} = 18$  mA with a phase noise of  $-91$  dBc/Hz at 10 MHz from the 63.2 GHz carrier and  $-95$  dBc/Hz at 10 MHz from the 72.4 GHz carrier.

**Index Terms**—Frequency synthesizers, injection locking, millimeter-wave oscillators, triple push oscillators, 60 GHz radio.

## I. INTRODUCTION

**D**URING the past few years, substantial knowledge about the 60-GHz millimeter-wave (MMW) channel has been accumulated with a considerable amount of work done towards developing MMW communication systems for commercial applications [1]–[5]. The immediately seen opportunities in this particular region of the spectrum include next-generation wireless personal area networks (WPANs) with applications in high definition video streaming and wireless Gigabit ethernet. In the physical implementation of transceivers at 60 GHz, millimeter wave signal generators are key components, where achieving reasonable output power levels and low phase noise over a wide tuning range can be a challenging task.

A number of recent studies have reported various architectures for CMOS mm-wave frequency generators targeting the 60 GHz band [6]–[10]. However, among previously reported results, there are few examples that achieve the required tuning

range to cover the worldwide union of bands from 57 GHz to 66 GHz, with some margin for process and temperature variations. Achieving such tuning range for a given phase noise is hampered by the limited varactor tunability at 60 GHz, and the need for high frequency dividers with wide locking ranges. A notable exception to the direct frequency synthesis using a 60 GHz phase locked loop is the use of frequency multipliers to up-convert lower frequency sources (e.g., 20 GHz) to the 60 GHz range as demonstrated by Floyd [11], Chan and Long [12].

This paper proposes the use of triple push oscillators as combined oscillator/divider in a typical mm-wave frequency synthesizer. Section II presents the challenges for wide operation range mm-wave PLLs. Section III discusses an architecture for mm-wave PLLs based on triple push oscillators and compares this architecture to existing designs based on frequency multipliers. The behavior of triple push oscillators based on injection locking theory is analyzed in Section IV to study their various oscillation modes, their stability and the effect of mismatch on the oscillator performance. Section V gives the implementation details for a triple push oscillator in 130 nm CMOS technology based on our work published in [13]. Key experimental results are highlighted in Section VI, and Section VII concludes the paper.

## II. CHALLENGES IN THE DESIGN OF WIDE OPERATION RANGE MMW PLLS

The block diagram of a typical MMW PLL employing injection-locked frequency dividers, is shown in Fig. 1. For a wide operation range, the VCO has to cover a broad tuning range while maintaining phase noise over that range. The divider locking range should also capture the VCO tuning range and the center frequencies of both circuits have to be aligned.

For the VCO, the tank quality factor affects phase noise, tuning range and power consumption. Although inductor values and their associated series loss tend to decrease at mm-wave frequencies, their quality factors are expected to stay around 30 in the 60 GHz range mainly due to increased substrate losses [14]. This has been demonstrated in various publications as in [10], [14], [15]. This saturation of Q makes the design of millimeter-wave oscillators quite difficult as the trade-offs between phase noise, tuning range, and power dissipation become much more severe. In addition, the Q of varactors appears to fall below that of inductors at millimeter-wave frequencies (for example, a quality factor in the range of 5–20

Manuscript received November 22, 2009; revised January 30, 2010; accepted April 14, 2010. Current version published July 23, 2010. This paper was approved by Guest Editor Ramesh Harjani. This work was supported by NSF ECCS award 0952581.

The authors are with the Electrical, Computer, and Systems Engineering Department, Rensselaer Polytechnic Institute, Troy, NY 12180 USA (e-mail: hellam@rpi.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2010.2049915

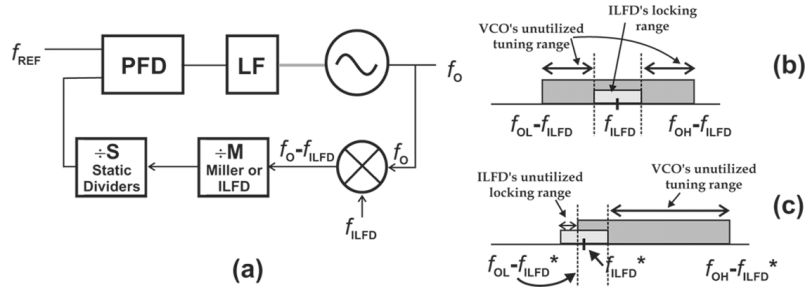


Fig. 1. (a) Typical mm-wave PLL employing injection-locked frequency divider ILFD. (b) Bandwidth performance limitations due to finite locking range of ILFD and (c) possible mismatch in the center frequencies.

TABLE I  
COMPARISON OF DIVIDER TOPOLOGIES

	Power	$f_{in}$	$f_{op(BW)}$
Static	High	Low	High
Miller	Moderate	Moderate	Moderate
Injection Locked	Low	High	Low

is reported for varactors at 60 GHz using 90 nm technology [14]). Moreover, meeting a wide tuning range requirement is another challenge, as the  $LC$  budget is strictly limited by device parasitics. In recently published CMOS VCOs operating near 40–60 GHz, tuning ranges were significantly less than 5 GHz as in [16]–[18], except for those fabricated using SOI processes [19], [20] due to the lower parasitic capacitances in the SOI process.

In addition to the above requirements, the oscillator needs to drive high speed dividers in the PLL. Frequency divider stages become more difficult to implement and are power hungry at mm-wave frequencies. Table I compares divider architectures and their performances, where it can be seen that injection locked frequency dividers (ILFD) are more appropriate for mm-wave applications compared to other architectures, and indeed they are a common practice as reported in [6]–[10]. When a mm-wave VCO and ILFD are combined, typically the locking range of the ILFD is much narrower than the tuning range of the mm-wave VCO. The locking range of ILFD is given by [23]

$$\omega_L = \frac{\omega_o}{Q} \frac{K_I}{\sqrt{1 - K_I^2}} \quad (1)$$

where  $\omega_o$  is the free running tank frequency,  $Q$  is the tank quality factor, and  $K_I = I_{inj}/I_{dc} < 1$  is the injection strength. Injection-locked circuits typically suffer from a limited locking range, which results in narrower operation range for the PLL and a significant portion of the tuning range of the VCO getting unutilized. While the locking range of the ILFD can be enhanced through increasing the signal power or reducing the tank  $Q$ , this comes at the expense of increasing the power consumption in the VCO to raise the level of output power necessary to drive the ILFD.

Matching the oscillator and divider center frequencies is another issue in the design of mm-wave PLLs based on ILFD. To understand this limitation, let us re-examine Fig. 1, where the “phase locking” mechanism in a frequency synthesizer involves aligning the output phase of the divided or “down-con-

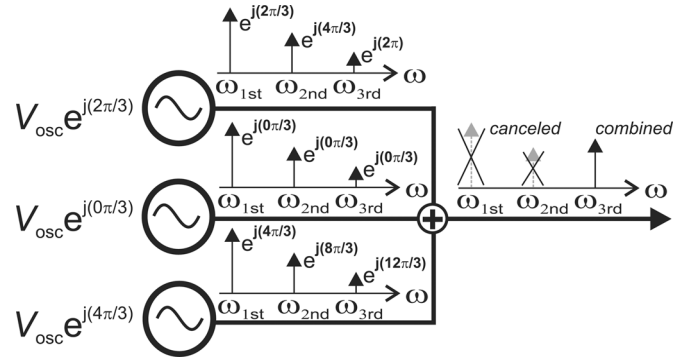


Fig. 2. Triple push operation.

verted” VCO signal with the phase of a reference clock. In theory, ILFDs can be considered as an oscillator with a specific phase condition between the injected signal and its free running frequency along the locking range. Thus, fundamentally, having a mm-wave oscillator followed by an ILFD in a PLL loop is basically equivalent to having two independent oscillators that are oscillating at two different frequencies and attempting to achieve locking condition. Published design techniques to mitigate the mismatch effect include driving the VCO and the injection locked divider using the same control voltage [10] as well as off-chip and on-chip calibration of the divider control voltage [6], [7]. Recent millimeter-wave PLLs using ILFD have reported a tuning range between 320 MHz to 4.6 GHz [6]–[10], [24], [25], which is not sufficient to cover the whole ISM band at 60 GHz. Other techniques use multiple oscillators to cover the required operating band [21]. Frequency multipliers that follow a lower frequency PLL-stage have also been reported [11], [12], [22]. The advantages and limitations of PLLs based on frequency multipliers are discussed in Section III.

### III. N-PUSH OSCILLATORS AS COMBINED OSCILLATORS/DIVIDERS IN MMW PLLS

$N$ -push oscillator topologies are a special class of coupled oscillators that explore symmetry to generate the  $N$ th harmonic frequency signal. This is done by coupling  $N$  oscillators either through a ring based network or through a star network. When individual coupled oscillators are synchronized with a progressive phase distribution of  $2\pi/N$  rad, the combined output will have all harmonics up to the order  $(N - 1)$  canceled, whereas the  $N$ th harmonic summed up as shown conceptually in Fig. 2.

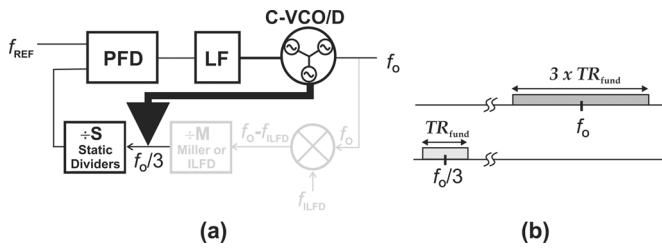


Fig. 3. (a) MMW PLL employing combined VCO/divider, (b) using triple push oscillators as combined VCO/divider with the potential of tripling the effective tuning range of the core oscillator.

Now, in the light of the discussion in Section II, let us consider the  $N$ -push oscillator (for example  $N = 3$ ) in a given mm-wave PLL as shown in Fig. 3. In this scenario, the  $N$ -push oscillator is analogous to a combined oscillator/ILFD, where the phase locking condition is intrinsically satisfied due to the coupling between the oscillators in the  $N$ -push operation. In addition, the “divided” signal is already present at the output of the fundamental oscillator. For example, in the case of the shown 3-push 60 GHz oscillator, a 20 GHz signal is available from the core oscillators which enables the direct use of just static dividers with wide operation range compared to Miller or additional injection locked dividers in the PLL chain. Avoiding the division process results in maintaining almost complete tuning range of the VCO. This is in contrast to the VCO followed by ILFD where any mismatch between the center frequencies or limited locking range would result in reduced bandwidth of the PLL [26].

Within the context of mm-wave PLLs, an  $N$ -push oscillator acting as a combined oscillator/divider C-VCO/D has several advantages. First, since the fundamental signal is generated at one  $N$ th of the mm-wave signal, the fundamental oscillators have a better phase noise performance due to higher quality factor varactors in the lower frequency range. Second, since the generated signal is the  $N$ th harmonic of the fundamental, the output tuning range is  $N$  times that of the fundamental oscillator [Fig. 3(b)]. Finally, as reported in the classic work of York [27] and verified by Georgiadis *et al.* [28], the near-carrier phase noise of coupled oscillators is reduced to  $1/N$  of the unit oscillator, provided that the coupling network is reciprocal. This behavior is also confirmed through phase noise simulations as shown in Fig. 4 at the fundamental and third harmonic of a stand alone oscillator compared to fundamental and third harmonic of a triple push oscillator formed of the same stand alone oscillators. However, it should be noted that the triple push oscillator in the simulations consume 3 times the power of the stand alone oscillator. While this might suggest that the increase in power consumption is responsible for the improved phase noise, conceptually, if we assume that we begin with an already optimized VCO, one can not get  $N$ -push VCO’s improved phase noise performance out of the single VCO even if the power consumption is increased further given the practical limits of the tank parameters. In [29], a coupled oscillator mechanical analogy is used to show that coupled oscillators are less sensitive to impulsive perturbations than individual oscillators. Thus, coupling multiple

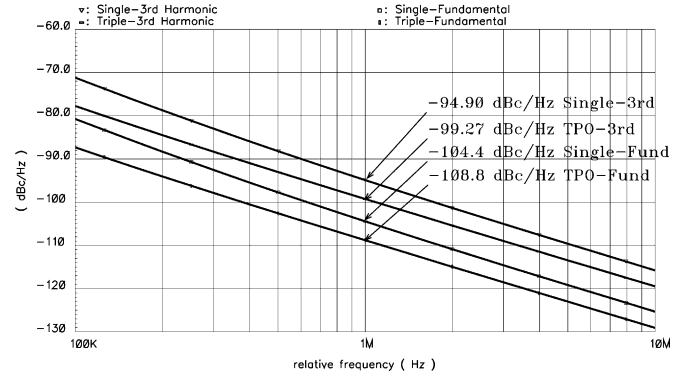


Fig. 4. An example of phase noise behavior at the fundamental and third harmonic frequencies of a standalone oscillator compared to an oscillator in triple push configuration under the same operating conditions.

oscillators together improves the timing of noise generators relative to the oscillation cycle, and an improved noise performance is expected without additional power consumption.

#### A. Comparison Between $N$ -Push Oscillators and Frequency Multipliers in Silicon-Based Technologies

Fig. 5 compares alternative approaches for silicon integrated mm-wave frequency generators using frequency multipliers [11], [12], [22] to the proposed approach based on  $N$ -push operation. In the architecture shown in Fig. 5(a) [11], [22], a frequency synthesizer that operates at  $\sim 20$  GHz is used to feed a tuned amplifier, whose operation band is selected at the third harmonic frequency of the fundamental signal. Thus, the tuned amplifier boosts the third harmonic signal while it suppresses other frequency components.

An alternative approach based on the use of frequency triplers can also be seen in Fig. 5(b) [12], where an external frequency source that operates at the fundamental frequency ( $\sim 20$  GHz) is applied to a hard limiter stage to attenuate the fundamental signal, while boosting third harmonic component. This signal is injected into an oscillator that operates at the third harmonic frequency of the fundamental signal. As the oscillator is already operating at the same frequency, the loop locks to third harmonic and all other frequency components are suppressed. The oscillator’s output is further amplified by a tuned amplifier.

Finally, the proposed approach is shown in Fig. 5(c), where three coupled fundamental oscillators generate identical signals with  $2\pi/3$  phase intervals. Thus, the fundamental and second harmonic rejection is inherent in the triple push operation, provided that accurate phase matching between the core oscillators is maintained. This is in contrast to the previous approaches based on frequency tripler, where the tuned amplifier is responsible for harmonic suppression. While in the case of frequency triplers in general, a passive network can be used to isolate the third harmonic, in silicon-based technologies, the output power at the third harmonic is typically low and a tuned amplifier is needed to raise the output power to practical limits. This tuned amplifier can present a trade-off between output power and tuning range as reported in [12]. However, architectures based

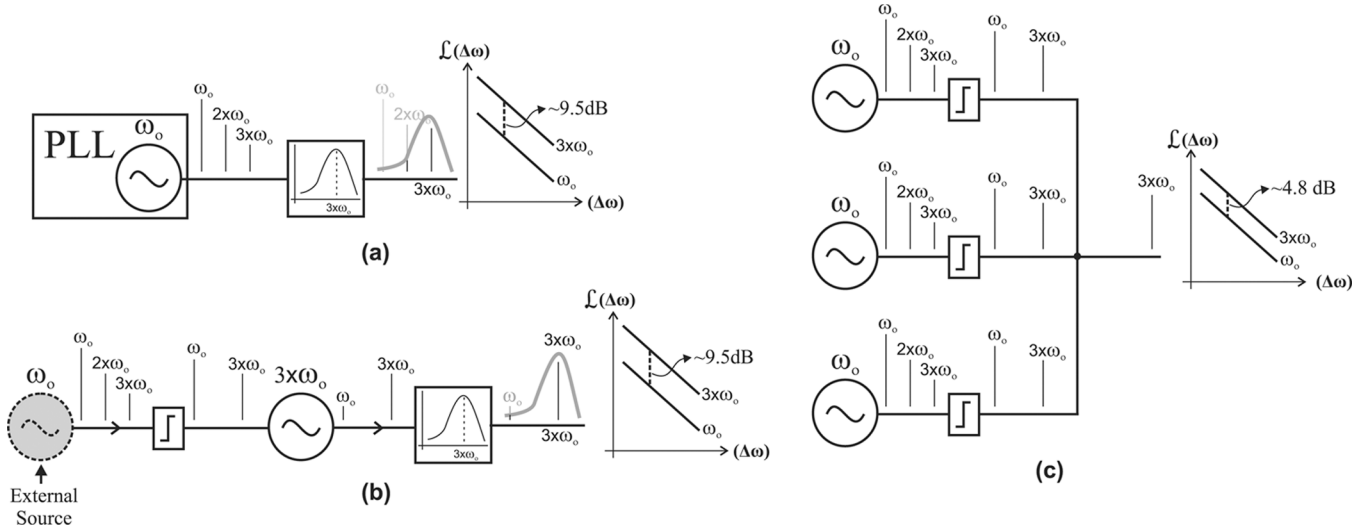


Fig. 5. Comparison between different harmonic-based architectures for mm-wave signal generation. (a) A 20 GHz PLL followed by a frequency tripler [11], (b) injection-locked frequency tripler [12], (c) triple push oscillator.

on frequency multipliers are also less sensitive to matching compared to N-push oscillators.

For phase noise performance, all harmonic-based systems suffer from phase noise degradation by  $20 \log(N)$ , where  $N$  is the harmonic order. This is approximately 9.5 dB for the third harmonic components. However, the mutual coupling of the triple push topology shown in Fig. 5(c) improves the fundamental oscillators' phase noise performance by  $10 \log(N)$  with respect to that of uncoupled single ended oscillator [27]. Thus, triple push oscillator's third harmonic output has theoretically a 4.7 dB better phase noise performance with respect to the former techniques. The main disadvantage of the proposed topology compared to previously reported approaches based on frequency multipliers is its single ended operation, which is a common feature of all N-push oscillators.

#### IV. ANALYSIS OF TRIPLE-PUSH OSCILLATORS

The operation of coupled oscillator systems in terms of its various oscillation modes and their stability is traditionally explained using the eigenvalues and eigenvectors of the impedance/admittance matrix which describes the coupling network associated with these modes [28], [30]–[32]. While these approaches are valid, they lack the physical insight into the oscillation operation. In what follows, the coupling phenomena among unit oscillators in an N-push architecture is analyzed using nonlinear injection-locking theory. It is worth noting that a similar analysis has been pursued by York in his studies on quasi-optical oscillator arrays for beam forming [33].

In this paper, we focus on triple push oscillators rather than higher order push oscillators such as quadrature-push oscillators ([34], [35]). This is due to the fact that N-push oscillators as in any harmonic based oscillator rely on harmonic frequency generation, where the harmonic energy decreases with increasing the number of harmonics. Thus, additional buffer stages are typically required to provide a given signal swing, which would increase the power consumption. In addition, lower order push oscillators are more amenable to monolithic integration given the

complexity of integrating multiple tanks in a given area. Higher order coupled oscillators will also have more unwanted oscillation modes that have to be suppressed. Thus, choosing a triple push operation would provide a good balance between the signal power at the oscillator output and the frequency of the core oscillator units that will directly feed the divider chain.

Fig. 2 shows the conceptual operation of triple-push oscillators. It is formed of three identical fundamental oscillators, whose outputs are connected to a common load. To analyze the coupling between the three oscillators, we use the model shown in Fig. 6, which is based on the injection-locking phenomenon. In this model, two of the oscillators act as injection sources, while the third is represented by its equivalent circuit. For the given model, (2) can be written based on KCL.

$$I_{inj1}e^{j\theta_1} + I_{inj2}e^{j\theta_2} = V_{osc}e^{j\theta}(G1 - Gm) + C \frac{d}{dt} (V_{osc}e^{j\theta}) + \frac{1}{L} \int_0^t V_{osc}e^{j\theta} d\tau \quad (2)$$

Equation (2) is difficult to solve and introduces a common mathematical problem seen in former analyses of systems described using injection locking phenomena [36], [37]. This integro-differential equation can be solved by making various approximations. In this paper, we use the low-pass filter analogy and the approximation based on this analogy [36]. Thus, we multiply both sides of (2) by  $e^{-j\theta}$ :

$$I_{inj1}e^{j(\theta_1-\theta)} + I_{inj2}e^{j(\theta_2-\theta)} = V_{osc}(G1 - Gm) + C \frac{dV_{osc}}{dt} + \frac{1}{L} \left[ \underbrace{e^{-j\theta} \int_0^t V_{osc}e^{j\theta} d\tau}_F \right] \quad (3)$$

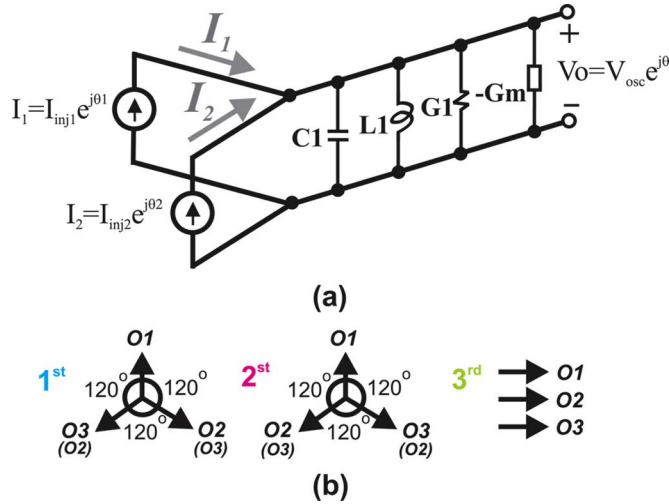


Fig. 6. (a) Equivalent circuit using injection-locking phenomena, (b) possible oscillation modes under triple push operation.

Under the assumption that the injected signal  $\omega_{inj}$  is close to the free running frequency of the oscillator  $\omega_o$ , the expression  $F$  in (3) can be written as in the following:

$$F \simeq -j \frac{V_{osc}}{\omega_o^2} \left( 2\omega_o - \frac{d\theta}{dt} \right). \quad (4)$$

Substituting (4) in (3) and considering real and imaginary parts separately, while assuming  $V_{osc} = I_{osc} Q \omega_o L1$ , the equations that model the amplitude and the phase dynamics can be given as

$$C \frac{dV_{osc}}{dt} + V_{osc} (G1 - Gm) \simeq I_{inj1} \cos(\theta_1 - \theta) + I_{inj2} \cos(\theta_2 - \theta) \quad (5)$$

$$\frac{d\theta}{dt} \simeq \omega_o + \frac{\omega_o}{2Q} \left[ \frac{I_{inj1}}{I_{osc}} \sin(\theta_1 - \theta) + \frac{I_{inj2}}{I_{osc}} \sin(\theta_2 - \theta) \right]. \quad (6)$$

To find the operation modes of the oscillator, we define the phase of each fundamental oscillator as  $\theta_1 = \omega_{osc} t$ ,  $\theta_2 = \omega_{osc} t + \psi_2$ , and  $\theta_3 = \omega_{osc} t + \psi_3$ , where  $\psi_i$  shows the phase difference with respect to reference oscillator. The solution sets for the unknown  $\psi_i$ s determine the possible operation modes of the triple-push oscillator. Substituting  $\theta_i$ s in (6) while assuming that all the oscillators are balanced, we can write the phase equation for each oscillator. Thus, the following equation set can be obtained for the coupled system:

$$\begin{aligned} \omega_{osc} &\simeq \omega_o + \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(\psi_2) + \sin(\psi_3)] \\ \omega_{osc} &\simeq \omega_o + \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(-\psi_2) + \sin(\psi_3 - \psi_2)] \\ \omega_{osc} &\simeq \omega_o + \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(-\psi_3) + \sin(\psi_2 - \psi_3)]. \end{aligned} \quad (7)$$

Mathematically, the equation set has several solutions, however only few of them correspond to unique modes of operation. For the solution set of  $\{\psi_2, \psi_3 = 2\pi/3, 4\pi/3\}$ , we obtain triple-push operation, while  $\{\psi_2, \psi_3 = 0, 0\}$  set shows undesired even-mode or in phase oscillation.

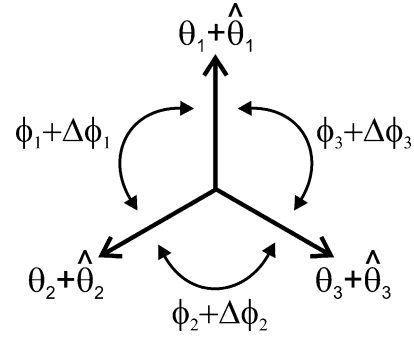


Fig. 7. Perturbation analysis for studying the stability of triple-push oscillation mode.

Once the analysis for the fundamental harmonic is completed, the same analysis can be used to find the steady state phases of second and third harmonic. Intuitively, we can state that the second harmonics for the oscillators would have a phase of  $\theta_2'' = 2(\omega_{osc} t + \psi_2)$  and  $\theta_3'' = 2(\omega_{osc} t + \psi_3)$ , while the third harmonic phases would be  $\theta_2''' = 3(\omega_{osc} t + \psi_2)$  and  $\theta_3''' = 3(\omega_{osc} t + \psi_3)$ . Thus, we obtain the phase portrait shown in Fig. 6(b), which shows the inherent advantage of triple push operation; third harmonic boosting with fundamental and second harmonic rejection. In what follows, we will use the above equations to study the stability of triple push oscillators as well as their sensitivity to mismatch.

#### A. Stability of Oscillation Modes

The above analysis indicates that the oscillator may oscillate in more than one mode, where each mode would be associated with different phase sequence. However, not all of these modes are considered stable. While we show the stability of the triple push oscillation mode in this section, we will be addressing how to suppress other potentially stable modes in Section V. To study the stability of the triple push mode  $\{\psi_1, \psi_2, \psi_3 = 0, 2\pi/3, 4\pi/3\}$ , we will use perturbation analysis. Note that the stability of the oscillator is defined in terms of the phase differences between the fundamental oscillator units rather than their absolute values. The phase differences between the oscillators shown in Fig. 7 can be defined as in the following:

$$\begin{aligned} \phi_1 &= \theta_2 - \theta_1 \\ \phi_2 &= \theta_3 - \theta_2 \\ \phi_3 &= \theta_1 - \theta_3. \end{aligned} \quad (8)$$

To test the stability of the triple-push oscillation mode, we apply a small amount of phase perturbation  $\hat{\theta}_i$  to each phase and observe if the perturbation decays as time passes. For this purpose, we can rewrite each phase as

$$\begin{aligned} \theta_1 &= \omega_{osc} t + \hat{\theta}_1 \\ \theta_2 &= \omega_{osc} t + 2\pi/3 + \hat{\theta}_2 \\ \theta_3 &= \omega_{osc} t + 4\pi/3 + \hat{\theta}_3 \end{aligned} \quad (9)$$

Thus, (6) and (9) will lead us to equation set (10) and matrix (11), shown at the bottom of the next page. In (10), the non-linear terms can be linearized around 0 as the perturbation is

considered small enough. Thus, the matrix form given in (11) that models the stability of the system is obtained. The system stability can then be checked by inspecting the eigenvalues of matrix  $M$ , which are

$$\lambda_1 = 0 \quad (12a)$$

$$\lambda_2 \simeq -\frac{(1.125 + j0.64)\omega_o I_{inj}}{I_{osc} Q} \quad (12b)$$

$$\lambda_3 \simeq -\frac{(1.125 - j0.64)\omega_o I_{inj}}{I_{osc} Q}. \quad (12c)$$

Two of the eigenvalues given in (12) have negative real parts, which indicates stable oscillations, while the third one is equal to zero. This result agrees with prior analysis performed by York [33] on the stability of loosely-coupled  $N$  sinusoidal oscillators, where an  $N \times N$  stability matrix is obtained for the system and one of the eigenvalues is always equal to zero. This is a result of the arbitrary assignment of the phase reference, and the stable solution in this case corresponds to all but one of the eigenvalues having negative real parts [38].

### B. Inaccuracy in Triple Push Operation Due to Mismatches

Mismatch between the three oscillator units comprising the triple push oscillator causes the reduction in the fundamental and second harmonic suppression. It might even lead to complete suppression of the triple push operation. A typical  $N$ -push oscillator is formed of an array of core coupled oscillators, each followed by hard-limited buffer stage to boost the harmonic level. Thus, the buffer stages would be insensitive to any amplitude mismatch between the core oscillator units but fully respond to their individual phase variations. Mismatch can arise between the three core oscillations in their respective injection currents, oscillator currents, and tank resonance frequencies, as well as tanks' quality factors. Let us assume a reference oscillator and consider the mismatch as that between the reference oscillator and the remaining two oscillators. Thus,  $\omega_{o1} = \omega_o, \omega_{o2} = \omega_o + (\Delta\omega)/2, \omega_{o3} = \omega_o - (\Delta\omega)/2$ . The mismatch in the tank losses, injection, and oscillation currents can be represented as

$R1 = R, R2 = R + (\Delta R)/2, R3 = R - (\Delta R)/2, I_{inj1} = I_{inj}, I_{inj2} = I_{inj} + (\Delta I_{inj})/2, I_{inj3} = I_{inj} - (\Delta I_{inj})/2, I_{osc1} = I_{osc}, I_{osc2} = I_{osc} + (\Delta I_{osc})/2, I_{osc3} = I_{osc} - (\Delta I_{osc})/2$ , respectively. We will assume that the mismatches are small enough that the three oscillators remain locked and oscillate at the same frequency. Thus, for the mismatch case, the phases of the oscillators can be expressed as  $\theta_1 = \omega_{osc}t, \theta_2 = \omega_{osc}t + 2\pi/3 + \Delta\psi_2, \theta_3 = \omega_{osc}t + 4\pi/3 + \Delta\psi_3$ . The phase mismatch terms  $\Delta\psi_2$  and  $\Delta\psi_3$  can be found by writing (7) for mismatch case as in the following:

$$\frac{d\theta_1}{dt} = \omega_{o1} + \frac{\omega_{o1}}{2Q_1} \frac{I_{inj1}}{I_{osc1}} \left[ \sin\left(\frac{2\pi}{3} + \Delta\psi_2\right) + \sin\left(\frac{4\pi}{3} + \Delta\psi_3\right) \right] \quad (13a)$$

$$\frac{d\theta_2}{dt} = \omega_{o2} + \frac{\omega_{o2}}{2Q_2} \frac{I_{inj2}}{I_{osc2}} \left[ \sin\left(-\frac{2\pi}{3} - \Delta\psi_2\right) + \sin\left(\frac{2\pi}{3} + \Delta\psi_3 - \Delta\psi_2\right) \right] \quad (13b)$$

$$\frac{d\theta_3}{dt} = \omega_{o3} + \frac{\omega_{o3}}{2Q_3} \frac{I_{inj3}}{I_{osc3}} \left[ \sin\left(-\frac{4\pi}{3} - \Delta\psi_3\right) + \sin\left(-\frac{2\pi}{3} + \Delta\psi_2 - \Delta\psi_3\right) \right]. \quad (13c)$$

The solution to (13) involves additional linearization and simplifications to reach the following compact and useful solution:

$$\Delta\psi_{2,3} \approx \mp Q \frac{2I_{osc}}{3I_{inj}} \frac{\Delta\omega}{\omega_o}. \quad (14)$$

Equation (14) indicates that only the mismatch between the core oscillators' free running frequency ( $\omega_o$ ) causes phase error in triple push operation, and the circuit by nature is insensitive to other sources of mismatch at first order. Monte Carlo simulations in Section V and the experimental results in Section VI will also give more insight into the robustness of the triple push operation.

$$\frac{d\hat{\theta}_1}{dt} = \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(\hat{\theta}_2 - \hat{\theta}_1 + 2\pi/3) + \sin(\hat{\theta}_3 - \hat{\theta}_1 + 4\pi/3)] \quad (10a)$$

$$\frac{d\hat{\theta}_2}{dt} = \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(\hat{\theta}_1 - \hat{\theta}_2 - 2\pi/3) + \sin(\hat{\theta}_3 - \hat{\theta}_2 + 2\pi/3)] \quad (10b)$$

$$\frac{d\hat{\theta}_3}{dt} = \frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} [\sin(\hat{\theta}_1 - \hat{\theta}_3 - 2\pi/3) + \sin(\hat{\theta}_2 - \hat{\theta}_3 - 2\pi/3)] \quad (10c)$$

$$\frac{d}{dt} \begin{bmatrix} \Delta\phi_1 \\ \Delta\phi_2 \\ \Delta\phi_3 \end{bmatrix} = \frac{d}{dt} \begin{bmatrix} \hat{\theta}_2 - \hat{\theta}_1 \\ \hat{\theta}_3 - \hat{\theta}_2 \\ \hat{\theta}_1 - \hat{\theta}_3 \end{bmatrix} = \underbrace{\frac{\omega_o}{2Q} \frac{I_{inj}}{I_{osc}} \begin{bmatrix} -1.5 & 1.5 & 0 \\ 0 & -1.5 & 1.5 \\ 1.5 & 0 & -1.5 \end{bmatrix}}_M \begin{bmatrix} \hat{\theta}_1 \\ \hat{\theta}_2 \\ \hat{\theta}_3 \end{bmatrix} + \begin{bmatrix} C_1 \\ C_2 \\ C_3 \end{bmatrix} \quad (11)$$

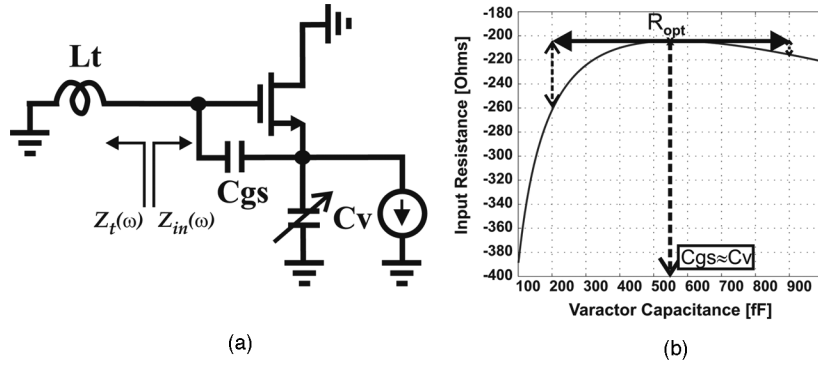


Fig. 8. (a) Schematic of Colpitts oscillator. (b) Variation of negative resistance versus varactor capacitance.

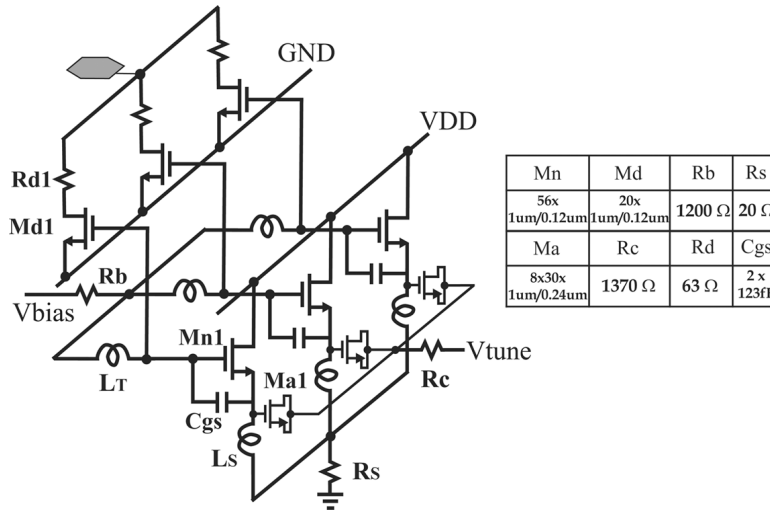


Fig. 9. Schematic of combined VCO/divider.

V. CIRCUIT DESIGN

The N-push operation in the C-VCO/D is satisfied using a triple push oscillator. The core oscillator in the triple push configuration is based on a Colpitts topology as shown in Fig. 8(a). The tank varactor controls the tuning range of the Colpitts oscillator. However, while determining the required range of varactor capacitance  $C_V$  for a specific tuning characteristics, one must also consider the variation in the equivalent negative input resistance of the circuit  $R_x$  with  $C_V$ , where  $R_x$  can be expressed as in the following:

$$R_x = \frac{1}{\text{Re}\{Y_{in}(\omega)\}} = -\frac{gm^2 + \omega^2(C_{gs} + C_v)^2}{\omega^2 gm C_{gs} C_v}. \quad (15)$$

For a given power consumption, the optimum negative input resistance is obtained when varactor capacitance  $C_v$  is equal to  $C_{gs}$ . As can be seen from Fig. 8(b), as  $C_v$  reduces below this point, the input negative resistance decreases rapidly.

The design of MMW colpitts oscillator revolves around the tank design. The tank inductance  $L_t$  is designed for maximum quality factor, while limiting its sensitivity to the parasitic series resistance. For a given power consumption budget, the transistor aspect ratio is selected to exceed a certain transconductance and guarantee the start up of the oscillator, while the remaining capacitors determine the operating frequency. The design process requires many iterations mainly to tolerate the high sensitivity of

the tanks to the parasitics due to low  $LC$  budget at mm-wave frequencies. The transistor level schematic of the combined VCO/Divider (C-VCO/D) is shown in Fig. 9. Three identical core oscillators are coupled to each other at source and gate terminals through the inductor network. The passive coupling network is selected rather than an active network using common-source amplifiers or differential amplifiers for two reasons. First, if the coupling network were implemented using active stages, every fundamental unit oscillator would require two buffers to inject its signal to the other two fundamental oscillators. This would result in a total of 6 buffers for a triple-push VCO just to create the coupling network, excluding the buffers needed to drive the output load. This will ultimately increase the circuit complexity in terms of routing and floor-plan as well as increase the power consumption. Second, adding the buffers would increase the parasitic loading on the oscillator cores, which would limit both the maximum oscillation frequency and the tuning range given the limited  $LC$  budget in the mm-wave range. However, since the fundamental oscillators are coupled together through common nodes and the inductor network rather than active buffer stages, there is no control mechanism to vary the coupling strength, which is a limitation to the current design.

To avoid even mode oscillation, the loads connected to the common nodes of the system ( $R_b$  and  $R_c$  in Fig. 9) should be selected appropriately. Let us consider the equivalent circuit of the

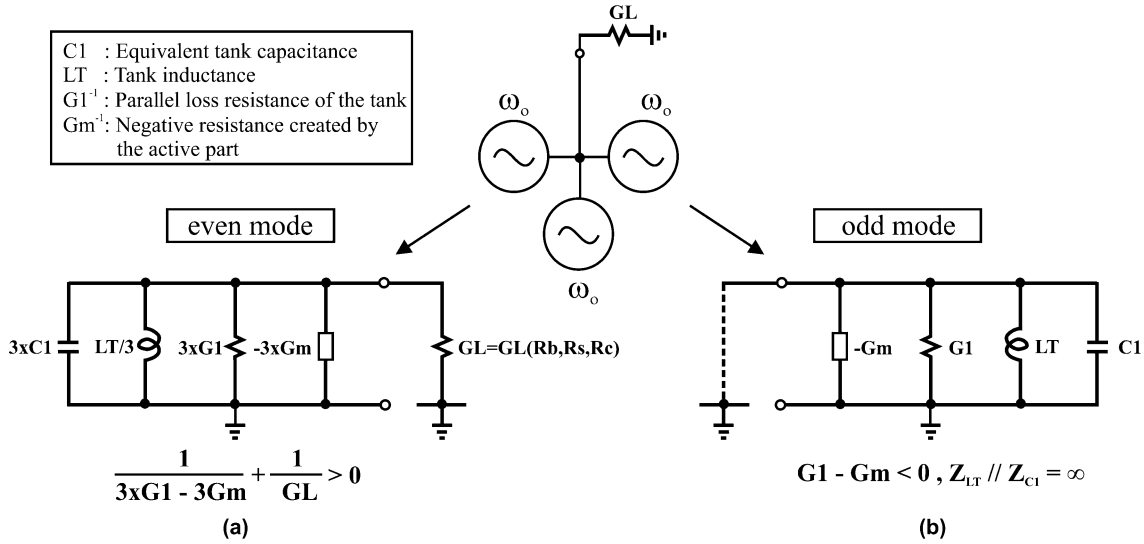


Fig. 10. (a) Even mode and (b) odd mode equivalent circuits.

oscillator system for even mode and odd-mode cases as shown in Fig. 10. For even mode oscillation, since all the oscillators are in phase, a single equivalent tank circuit is created as the parallel equivalent of the three fundamental oscillators. The load of the oscillator is connected in series with the tank which will increase the tank loss. To avoid even mode oscillation, the load resistance has to satisfy the following condition:

$$\frac{1}{3G1 - 3Gm} + \frac{1}{GL} > 0. \quad (16)$$

For the odd-mode (triple-push) operation, the common mode becomes a virtual ground and the load resistance does not have any effect on the oscillation condition, which in this case is given by

$$G1 - Gm < 0 \quad (17a)$$

$$Z_{LT} // Z_{C1} = \infty. \quad (17b)$$

While the core oscillators are connected together to meet the phase condition for triple-push operation, the buffer stages implemented using common source amplifiers with resistive loads, are used to combine and amplify the 3rd harmonic signal. Given the low output power limitation of harmonic based oscillators, this additional power boosting is required to enhance the output signal level. The output buffers are combined in an open drain configuration and drive the output pad as shown in Fig. 9. Using octagonal geometry for the output pad, its capacitance is kept as low as 32 fF. The bandwidth of the output determined by the pad capacitance together with other parasitics and the 50  $\Omega$  load is estimated to be around 80 GHz. In our implementation, the floor-plan limitations as will be discussed in the next subsection restricted the employment of a reactive component (*inductor*) in the buffer design as the drain load. This has limited the non-linearity of the buffer stage and reduced the achievable value of third harmonic power.

To verify the stability of the designed triple push oscillator and verify the analysis given in Section IV.A, the setup shown in Fig. 11(a) is used, where the triple-push oscillator is simulated at its steady state for certain period of time and then arbitrary

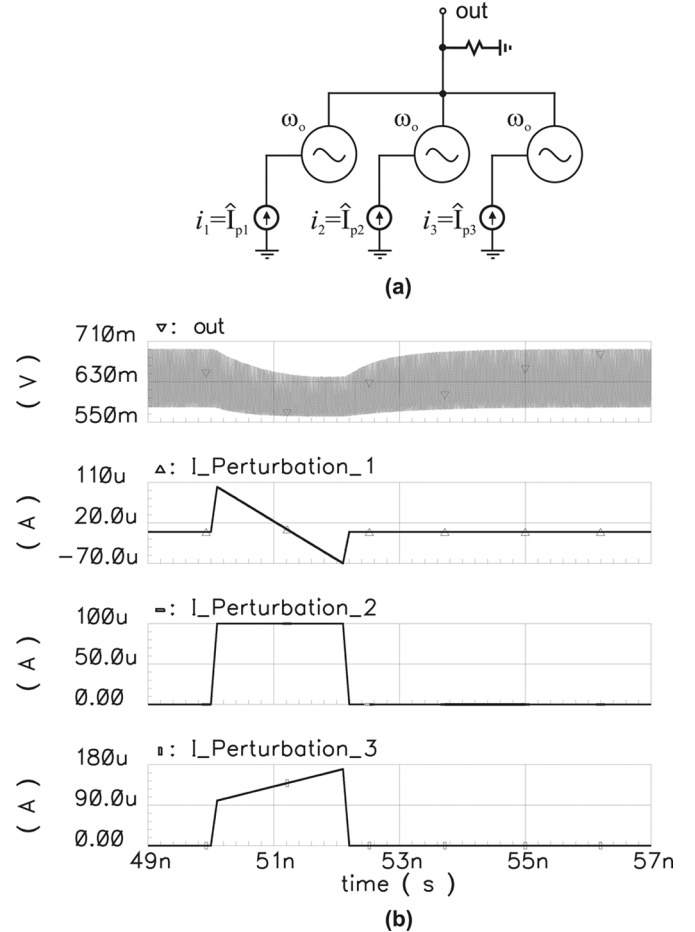


Fig. 11. (a) Perturbation test simulation setup. (b) Perturbation currents and oscillator output waveforms.

current perturbations are applied to the tanks of each fundamental oscillator for a limited time. The output waveforms shown in Fig. 11(b) show that the system recovers from the transient caused by perturbation currents. In fact, we observed the same stable behavior in the measurements of a prior 30 GHz triple-push oscillator prototype [39].



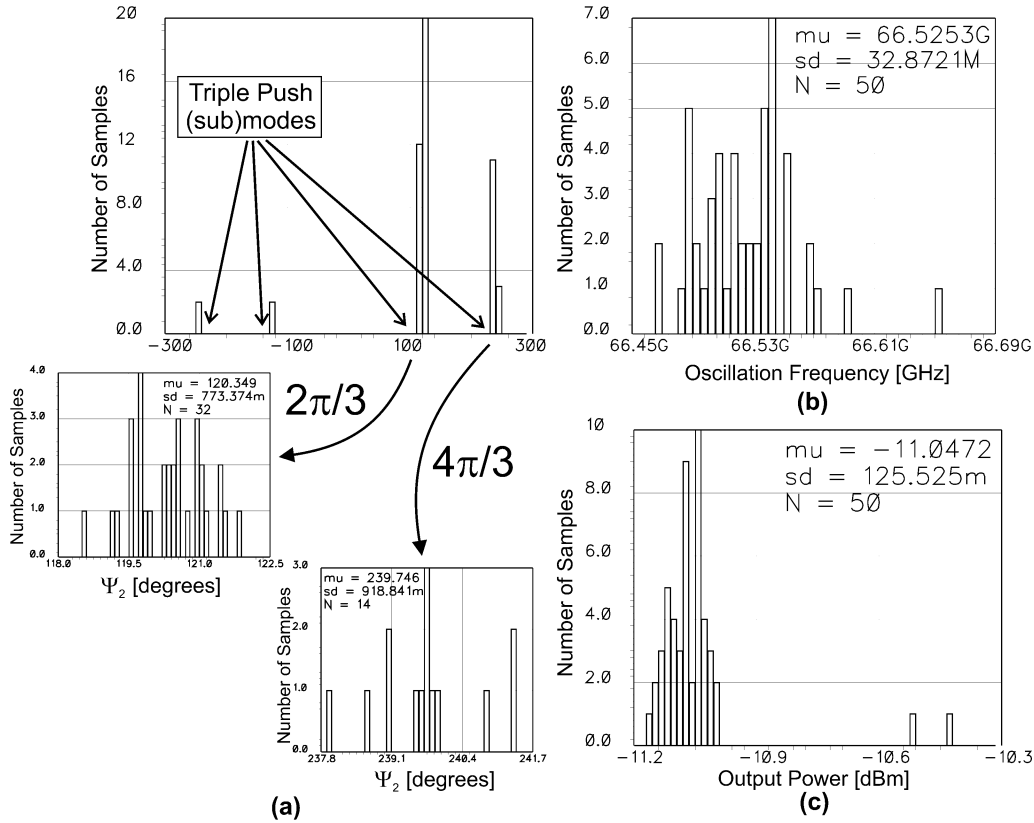


Fig. 12. Monte Carlo mismatch simulations showing (a) phase, (b) oscillation frequency, and (c) output power variations.

The effect of mismatch between fundamental oscillators in 60 GHz triple push configuration is investigated using Monte Carlo simulations. For the shown 50 Monte Carlo runs, although mismatches between the oscillators created different free running oscillation frequencies for the fundamental oscillators, all the oscillators were locked to a single oscillation frequency. However, for the same initial conditions, the mismatches between the unit oscillators put the TPO in different submodes, in which different fundamental oscillators can lead or lag, as long as 120° (or 240°) phase difference is kept.

As it can be seen from Fig. 12(a), there are two dominant submodes in this simulation setup with a phase error standard deviation less than 1 degree. The output frequency variation is less than 33 MHz around 66 GHz [Fig. 12(b)], while the output power varies in a range of 0.2 dBm [Fig. 12(c)]. The simulation results above show the robustness of the triple push operation against free running oscillation frequency variations between fundamental oscillators due to devices' variations.

A. Layout Considerations

Floor planing and layout are extremely critical for mm-wave frequencies, particularly for the case of the proposed circuit based on triple-push operation. If we consider the floor plan shown in Fig. 13(a), where the resonator inductors and source inductors are grouped separately, the interconnect length in this case is comparable to the resonator inductor and the circuit tends to occupy large area. In addition, its connection to the output RF pad becomes problematic. The second floor plan shown in Fig. 13(b) uses the technique of nested inductors [14], thus the

interconnect length and die area are greatly reduced and the RF pad can be connected directly to the output node. The top two metal layers are used to realize the resonator and source inductors. Extensive EM simulations are performed to select the proper layer for the resonator inductor. Although the 8th metal layer is thicker than 7th metal, according to Momentum simulation results, 7th metal (Cu) gives better Q with respect to 8th metal for the same geometry. This can be attributed to 8th metal's slightly higher sheet resistance and higher sidewall capacitance. To relax the routing and obtain a more compact structure, the 8th metal is used for the source inductor. Since the nested configuration may cause undesired loss due to the coupling between source and resonator inductors, the resonator inductor is simulated over a wideband as a stand-alone inductor and in nested configuration. According to Momentum simulation results, the resonator inductor has a negligible Q loss at 20 GHz as shown in Fig. 13(d).

B. Discussion

The main constituents of the triple push oscillator TPO are the array of unit oscillators and the buffer stages acting as a signal combiner. Fundamental oscillators establish the phase condition required for triple push operation. Any deviation from the target phase condition would result in reduction in the level of fundamental and second harmonic rejection. In addition, since they dominate the phase noise performance of the TPO, the tank Q of fundamental oscillators must be maximized. This comes at the expense of reducing the level of higher harmonic components generated in the core. This tradeoff between phase noise

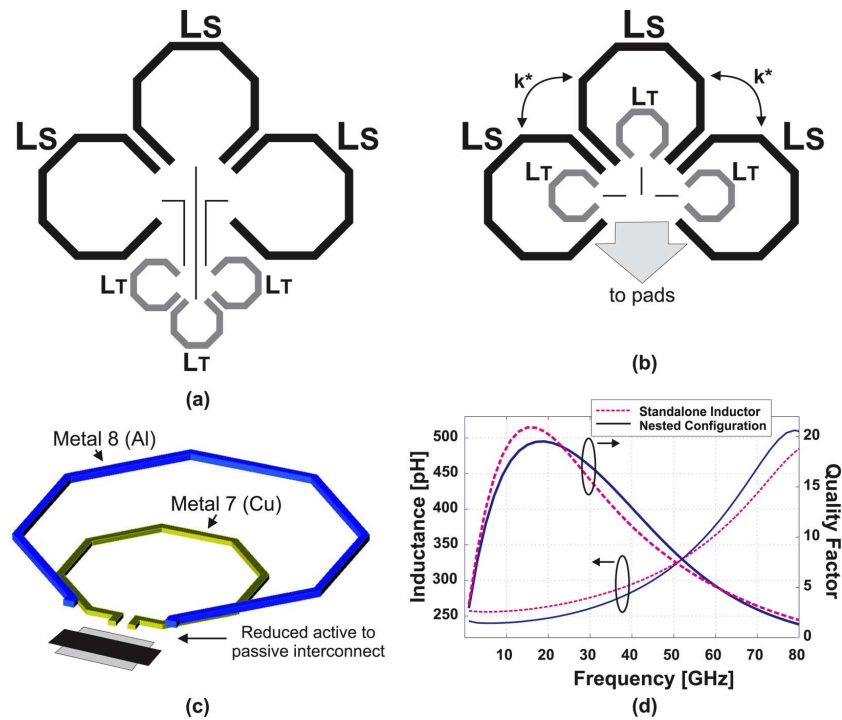


Fig. 13. Effect of floor planning and the coupling between nested inductors on the performance of passives in the proposed circuit. (a) A simple floor plan that separates the tank and source inductances, (b) a compact design based on nested inductors with shorter interconnect length, (c) selection of metal layers for tank and source inductors, (d) deviation of effective inductance and quality factor of tank inductor as a function of the frequency for cases (a) and (b).

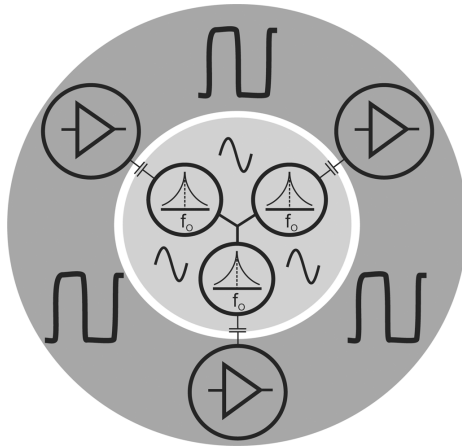


Fig. 14. Conceptual description of the independent functionalities and requirements of the buffer stage and the core amplifiers in the triple push oscillator.

and output power level at the third harmonic can be resolved by careful design partitioning, such that the core oscillator units (inner circle in Fig. 14) are mainly responsible for specific phase noise performance while the buffer stages are responsible for boosting the level of output power at the third harmonic. The buffer stages shown in the outer circle in Fig. 14 should be designed and properly biased such that they operate as highly non-linear or switching class amplifiers (e.g., saturated class A or class E stages).

For a given power budget, independent biasing of the fundamental oscillators and buffer stages is advised to optimize the overall performance, given their different functionalities. In

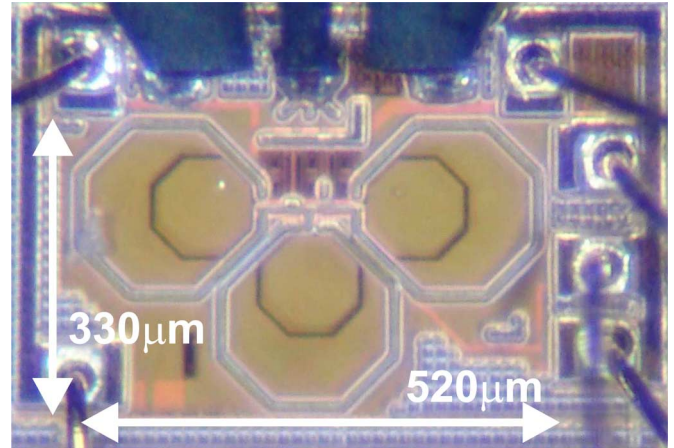


Fig. 15. Die microphotograph.

our current implementation however, the fundamental oscillators and active combiners are biased from a single source due to floor-plan limitations. To enhance the output power level, the bias voltage is set to a higher voltage value than what would be typically required just to enable the driver stage. However, this causes the saturation of the signal swing at the fundamental oscillators, wasting some portion of the total power consumption and deteriorating the phase noise performance.

## VI. EXPERIMENTAL RESULTS

The triple push oscillator acting as C-VCO/D is implemented in an eight-metal  $0.13 \mu\text{m}$  IBM CMOS technology. The microphotograph of the fabricated C-VCO/D is shown

TABLE II  
C-VCO/D DESIGN PARAMETERS

Osc. Name	Cs	$L_T$ @19GHz	$Q$ @19GHz	$D$	$W$
C-VCO/D-1	Var.*	262pH	20.5	120 $\mu\text{m}$	5 $\mu\text{m}$
C-VCO/D-2	MIM	262pH	20.5	120 $\mu\text{m}$	5 $\mu\text{m}$
C-VCO/D-3	Var.*	206pH	20.7	100 $\mu\text{m}$	5 $\mu\text{m}$
C-VCO/D-4	Var.*	140pH	21.3	80 $\mu\text{m}$	6 $\mu\text{m}$

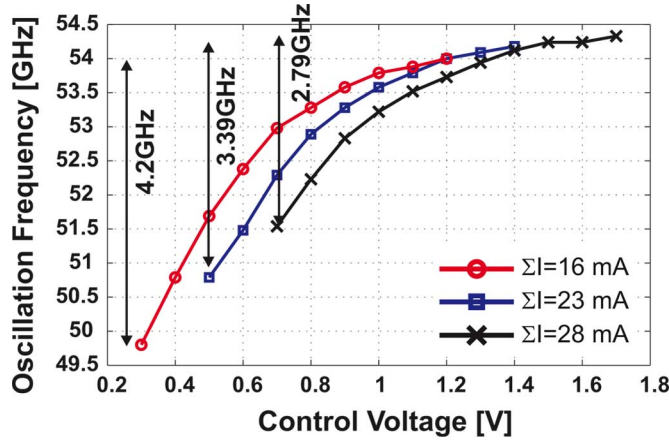


Fig. 16. The measured tuning range of C-VCO/D-1 as function of bias current.

in Fig. 15. The die is mounted on an FR-4 board and all the DC and control inputs are applied through bondwires. The measured single ended mm-wave output is taken from open drain buffers supplied through off-chip bias-T, as shown in Fig. 9. Agilent E4448A spectrum analyzer in conjunction with an Agilent 11970U/11970 V down-conversion mixer are used to test the C-VCO/D’s output. Four different C-VCO/D with three different inductors are realized as shown in Table II. The different versions are used to characterize the interaction between tank design, layout and oscillator performance in terms of tuning range and phase noise as well as account for any modeling inaccuracies.

Fig. 16 shows the tuning characteristics of C-VCO/D-1 for different bias currents at  $V_{DD} = 1.2$  V. The tuning range trend seen in the figure is also observed for other supply voltages. The relatively low tuning range of C-VCO/D-1 can be explained using two possible scenarios. First, since this version has the highest inductor values, the fundamental oscillator cores suffer from higher parasitic magnetic coupling such that distant free running frequencies from the core oscillator units are generated. This mismatch can limit the triple push operation range and the corresponding tuning range. Another possible reason is again related to the inductor size and it may also explain the reduced tuning range for the higher current levels. As the gate bias increases, the core oscillator swing reaches high levels earlier with respect to other versions due to the increased inductor size, while the buffers still require more bias current for a reasonable performance. Given that both the oscillator units and buffer stages share the same gate bias terminal ( $V_{bias}$ ), by increasing the biasing level to reach higher output power, the core swing is forced to its limits, generating other frequency components that may disrupt the triple push operation and drive the oscillator out of lock. This clearly shows the importance of reducing the parasitic magnetic coupling between core oscillators

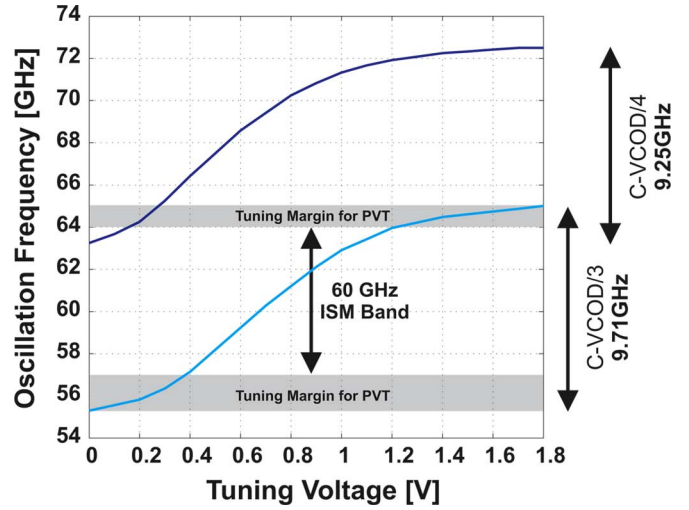


Fig. 17. (a) Tuning characteristics of C-VCO/D-3 and C-VCO/D-4.

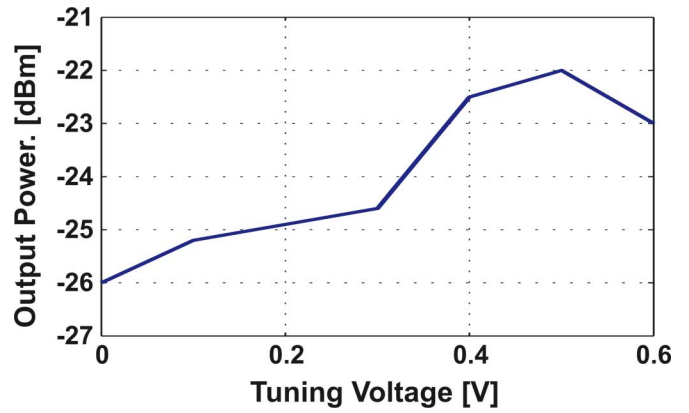


Fig. 18. Variation of output power over the tuning range for C-VCO/D-3.

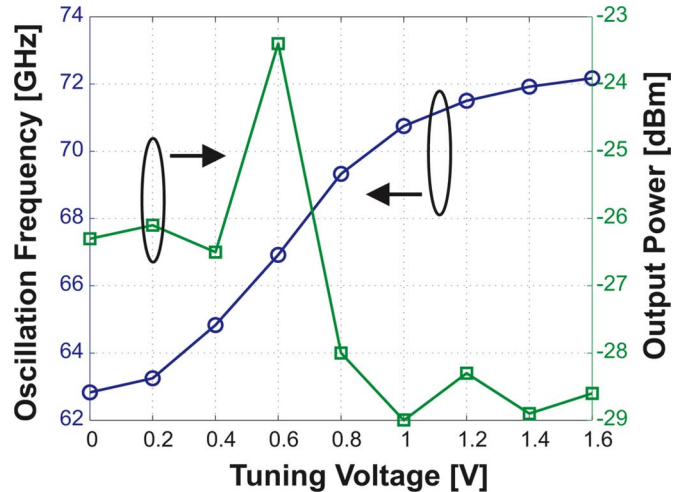


Fig. 19. Measured output power over tuning range for C-VCO/D-4.

through careful layout as well as providing independent bias for the core circuits and the combiner buffers as discussed in Section V.B.

Fig. 17 shows the tuning behavior of C-VCO/D-3 and C-VCO/D-4, with C-VCO/D-3 having  $V_{DD} = 1.4$  V,  $I_{core} = 20$  mA,  $I_{buffer} = 15$  mA, while C-VCO/D-4 has

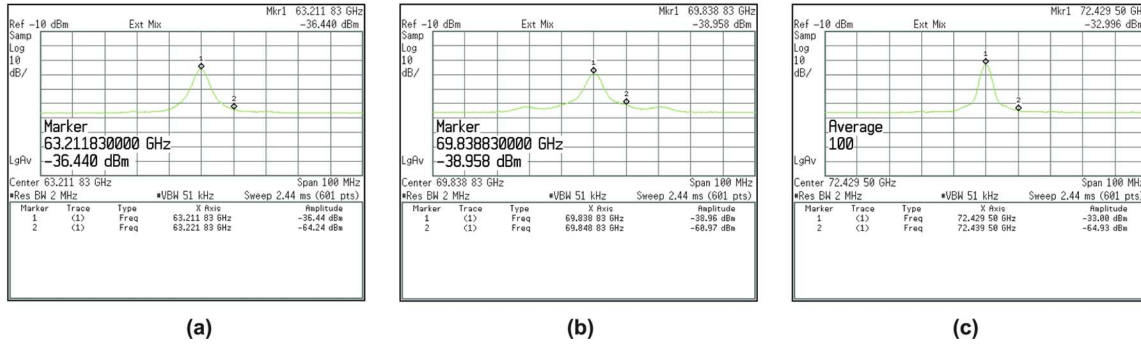


Fig. 20. Measured phase noise for different tuning voltages for C-VCO/D-4, (a)  $V_{Tune} = 0$  V, (b)  $V_{Tune} = 0.8$  V, (c)  $V_{Tune} = 1.6$  V.

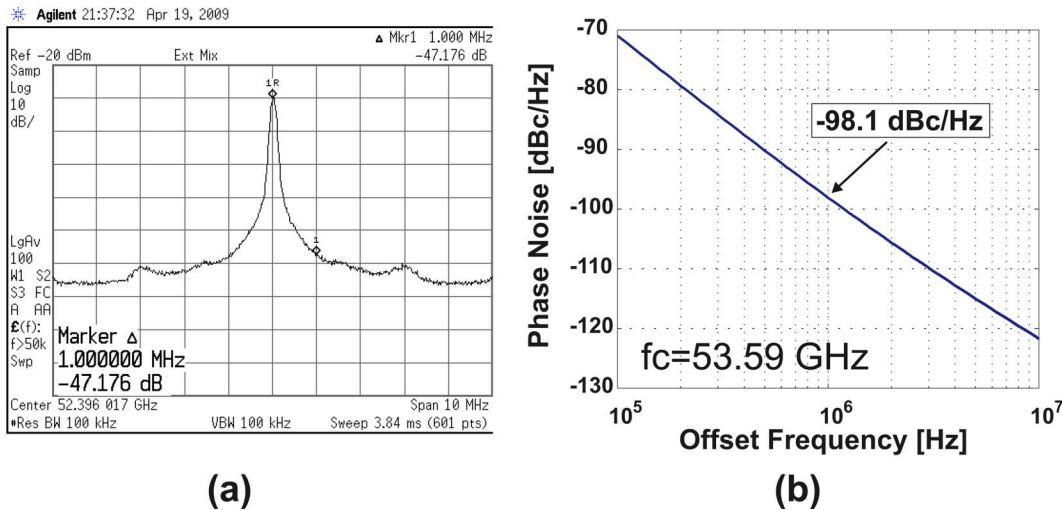


Fig. 21. (a) Measured and (b) simulated phase noise of C-VCO/D-2.

$V_{DD} = 1.5$  V,  $I_{core} = 17$  mA, and  $I_{buffer} = 18$  mA. C-VCO/D-3 has a tuning range of almost 10 GHz which covers all the ISM band, leaving margins at both ends for possible process variations and temperature changes. For the same setup, the deviation of output power with control voltage is given in Fig. 18 for C-VCO/D-3 and Fig. 19 for C-VCO/D-4. The change in output power as function of the control voltage is explained as follows; as the control voltage varies from 0 V to 1.6 V, a peak output power is observed around 0.6 V control voltage, while the output power for the high end of the control voltage is lower than that for the low end. The output power of the fundamental oscillators and thus the triple-push oscillator are determined by parallel equivalent resistance of the tank and the equivalent parallel input negative resistance of the oscillator. The parallel equivalent loss resistance of the tank slightly varies from 300 ohms to 320 ohms as the tuning voltage varies from 0 V to 1.6 V. The deviation of the parallel equivalent loss resistance is determined by the varactor, whose quality factor is low for 0 V control voltage and has its highest value at 1.6 V. Thus, as far as the contribution of the tank is concerned (ignoring the contribution of all other parameters), we expect the highest output power to occur at a control voltage = 1.6 V. However, when it comes to the contribution of negative resistance cell, in contrast to cross-coupled oscillators, the negative resistance of the Colpitts oscillator is not constant over the frequency spectrum and its value changes as a function of the

varactor settings. The negative equivalent parallel resistance of the active part is given in (15) and shown in Fig. 8(b). The best input negative resistance is obtained when varactor capacitance (CV) is equal to gate-source capacitance ( $C_{gs}$ ). Any value of varactor below or above  $C_{gs}$  degrades the negative resistance as shown in Fig. 8(b). In fact, the characteristic of the negative resistance deviation agrees with the deviation of the output power and reveals the mechanism that causes such a variation in the output power. Although the parallel equivalent loss resistance of the tank slightly improves and will increase the output power as the control voltage increases, ultimately, the considerable deviation of input negative resistance dominates and determines the characteristic of the output power variation overshadowing the effect of the parallel equivalent loss resistance of the tank.

The fundamental rejection performance based on extracted simulation results varies between +6.7 dB  $\sim$  +10.5 dB and -6 dB  $\sim$  +5 dB for C-VCO/D-1 and C-VCO/D-4, respectively. The relatively low rejection performance of C-VCO/D-4 can be attributed to its higher operation frequency, which is almost 30% higher than that of C-VCO/D-1. As the operation frequency increases, the impedance between the common nodes of the triple-push oscillator and ground becomes lower, boosting even mode operation and degrading triple-push operation. This change in coupling between fundamental oscillators due to the common-node impedance variation deteriorates the fundamental rejection

TABLE III  
STATE-OF-THE-ART MM-WAVE OSCILLATORS IN SILICON TECHNOLOGIES

VCO	$f_o$ [GHz]	TR [%]	PN <sup>a</sup> [dBc/Hz]	P (core+buffer) [mW]	VDD [V]	Area $\mu\text{m} \times \mu\text{m}$	Tech
H. Wang [16]	49.5	2.21	-99.7@1M	13+4	1.3	519x390	0.25 $\mu\text{m}$ CMOS
M. Tiebout [17]	51.2	1.39	-85@1M	1+8.25	1	500x900	0.12 $\mu\text{m}$ CMOS
C.Cao [40]	56.5	10.27	-108@10M	9.8+8	1.5	500x480	0.13 $\mu\text{m}$ CMOS
F. Ellinger [20]	56.5	14.70	-92@1M	21 <sup>c</sup>	1.5	300x250	90nm SOI CMOS
D. D.Kim [41]	70.2	9.55	-106.1@10M	5.4+4.75	1.2	60x45 <sup>d</sup>	65nm SOI
Borremans [42]	62.1	10	-95@1M	3.9+3.8	1	85x50 <sup>d</sup>	0.13 $\mu\text{m}$ CMOS
	59.1	10.2	-91@1M	3.9+3.8	1		
Lianming [43]	58.4	9.32	-91@M	8.1 <sup>c</sup>	0.7	96x80 <sup>d</sup>	90nm CMOS
	61.7	4.81	-90@1M	1.2 <sup>a</sup>	0.43		
T. Nakamura [44]	52.5	26.5	-108@1M	132 <sup>c</sup>	3	400x420	SiGe BiCMOS
N. Pohl[45]	81	29.6 <sup>b</sup>	-97@1M	240 <sup>c</sup>	5	-	SiGe Bipolar
This Work (C-VCO/D-3)/(C-VCO/D-4)	60/67.8	16.6/13.6	NA/-95@10M	33.6+36.4/18+24.6	1.4/1.5	520x330	0.13 $\mu\text{m}$ CMOS

a. Best-case phase noise within the tuning range, b. with approximately 1.5-9V tuning voltage range, c. Information about the buffer is not available, d. area without bond pads.

performance. Changing the buffer design by employing inductive loads will improve the fundamental rejection performance by boosting the third harmonic power. In a prior publication on 30 GHz triple push oscillator [39], we reported up to 18 dB fundamental rejection using inductively loaded buffers.

The phase noise at the band edges and at the center of tuning voltage for C-VCO/D-4 is characterized as seen in Fig. 20. For a 1.5 V supply and  $I_{\text{core}} = 17$  mA,  $I_{\text{buffer}} = 18$  mA, the phase noise is  $-91$  dBc/Hz at 10 MHz offset from the 63.2 GHz carrier. Similarly, for the same supply and for  $I_{\text{core}} = 12$  mA,  $I_{\text{buffer}} = 16.4$  mA, the phase noise is  $-95$  dBc/Hz at 10 MHz offset from the 72.4 GHz carrier. When using a MIM capacitor rather than a varactor as the case in C-VCO/D-2, the phase noise performance is better as seen in Fig. 21 which shows the measurement result for VDD = 1.4 V,  $I_{\text{core}} = 24$  mA,  $I_{\text{buffer}} = 26$  mA. According to measurement results, C-VCO/D-2 has a phase noise of  $-97.1$  dBc/Hz at 1 MHz offset from the carrier, while the simulated phase noise is  $-98.1$  dBc/Hz for the same bias setup. Considering the noisy supply, it can be stated that the simulations and measurement result are in good agreement with 1 dB error range.

Table III compares the performance of the 60 GHz triple push oscillator with published results to date. While the power consumption is higher than other designs implemented in CMOS technology, the proposed oscillator can function as both an oscillator and divider in a typical phase locked loop. Thus, its power consumption should be compared to the power of the combination of oscillator and injection locked frequency dividers. In addition, by modifying the design to have independent bias for the core oscillator units and the buffer stages as shown in Fig. 14, lower power consumption or higher output power for the same power consumption can be achieved. According to Table III, the proposed design has the best tuning range among the examples implemented in standard CMOS technologies. While [44] and [45] outperform the tuning range of the designed VCO, both suffer from high supply voltage, power dissipation and wide range of control voltage requirements.

## VII. CONCLUSION

This paper proposes the use of N-push operation for combining the functions of the VCO and dividers in the mm-wave

frequency range. If employed in a PLL, the combined VCO/divider (C-VCO/D) would potentially provide wider tuning range than traditional mm-wave PLLs employing injection locked frequency dividers, thus exploiting the full range available in the 60 GHz band (57 GHz–64 GHz). The behavior of triple push oscillators based on injection locking theory is analyzed to study their various oscillation modes, their stability and the effect of mismatch on the oscillator performance. Design guidelines are provided for boosting the third harmonic power at a given power budget. Measured results from multiple versions of the triple push oscillator in 130 nm IBM CMOS technology were presented to validate our findings. The use of N-push operation would facilitate the development of new circuit techniques for mm-wave circuit applications that efficiently utilize the wide bandwidth available and lends itself to operation at even higher frequency at the mm-wave/THz boundary. It can also be used in other applications in the mm-wave range such as frequency dividers, quadrature signal generators, and in phased arrays.

## ACKNOWLEDGMENT

The authors acknowledge helpful discussions with Ahmad Mirzaei of Broadcom Corporation. Special thanks go to RF Micro Devices for board assembly support and to Marianne Santangelo and Mike Selander from Agilent Technologies for assistance with the 60 GHz measurements.

## REFERENCES

- [1] P. Smulders, "Exploiting the 60 GHz band for local wireless multi-media access: Prospects and future directions," *IEEE Commun. Mag.*, vol. 40, no. 1, pp. 140–147, 2002.
- [2] C. H. Doan, S. Emami, D. A. Sobel, A. M. Niknejad, and R. W. Brodersen, "Design considerations for 60 GHz CMOS radios," *IEEE Commun. Mag.*, vol. 42, no. 12, pp. 132–140, 2004.
- [3] S. Reynolds, B. Floyd, U. Pfeiffer, and T. Zwick, "60 GHz transceiver circuits in SiGe bipolar technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, vol. 1, pp. 442–538.
- [4] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Design of CMOS for 60 GHz applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2004, vol. 1, pp. 440–538.
- [5] S. Sarkar, P. Sen, S. Pinel, C. H. Lee, and J. Laskar, "Si-based 60 GHz 2X subharmonic mixer for multi-Gigabit wireless personal area network application," in *IEEE MTT-S Int. Microwave Symp.*, Jun. 2006.
- [6] S. Pellerano, R. Mukhopadhyay, A. Ravi, J. Laskar, and Y. Palaskas, "A 39.1–41.6 GHz fractional synthesizer in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 484–485.

- [7] K.-H. Tsai, J. Wu, and S. Liu, "A digitally calibrated 64.3-to-66.2 GHz phase-locked loop," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2008, pp. 307–310.
- [8] H. Hoshino, R. Tachibana, T. Mitomo, N. Ono, Y. Yoshihara, and R. Fujimoto, "A 60 GHz phase-locked loop with inductorless prescaler in 90 nm CMOS," in *Proc. European Solid-State Conf. (ESSCIRC)*, Sep. 2007, pp. 472–475.
- [9] C. Lee and S. Liu, "A 58–60.4 GHz frequency synthesizer in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 196–197.
- [10] C. Cao and K. O. , "A 50 GHz frequency synthesizer in 0.13  $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1649–1656, Aug. 2007.
- [11] B. A. Floyd, "A 16–18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1076–1086, May 2008.
- [12] W. L. Chan and J. R. Long, "A 56–65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec. 2009.
- [13] B. Catli and M. M. Hella, "A 60-GHz combined CMOS VCO/divider with 10 GHz tuning range," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC 2009)*, Sep. 13–16, 2009, pp. 665–668.
- [14] B. Razavi, "Design of millimeter-wave CMOS radios: A tutorial," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, no. 1, pp. 4–16, Jan. 2009.
- [15] T. O. Dickson, M. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30–100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
- [16] H. Wang, "A 50 GHz VCO in 0.25  $\mu\text{m}$ ," in *IEEE ISSCC Dig. Tech. Papers*, 2001, pp. 372–373.
- [17] M. Tiebout, H. Wohlmuth, and W. Simburger, "A 1 V 51 GHz fully-integrated VCO in 0.12  $\mu\text{m}$ ," in *IEEE ISSCC Dig. Tech. Papers*, 2002, pp. 300–301.
- [18] A. P. van der Wel, S. L. J. Gierkink, R. C. Frye, V. Bocuzzi, and B. Nauta, "A robust 43-GHz VCO in CMOS for OC-768 SONET applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1159–1166, Jul. 2004.
- [19] N. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. Wagner, C. Plett, and G. Tarr, "A 40 GHz VCO with 9 to 15% tuning range in 0.13  $\mu\text{m}$  SOI CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2002, pp. 186–189.
- [20] F. Ellinger, T. Morf, and G. Buren, "60 GHz VCO with wideband tuning range fabricated in VLSI SOI CMOS technology," in *IEEE Int. Microwave Symp. Dig. Papers*, 2004, pp. 1329–1332.
- [21] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66 GHz quadrature PLL in 45 nm digital CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 494–495.
- [22] S. Reynolds, B. Floyd, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec. 2006.
- [23] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1415–1424, Sep. 2004.
- [24] J. Lee, M. Liu, and H. Wang, "A 75-GHz phase-locked loop in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1414–1426, Jun. 2008.
- [25] V. Jain, B. Javid, and P. Heydari, "A 24/77 GHz dual-band BiCMOS frequency synthesizer," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC 2008)*, Sep. 21–24, 2008, pp. 487–490.
- [26] J. Jeong and Y. Kwon, "A fully integrated V-band PLL MMIC using 0.15- $\mu\text{m}$  GaAs pHEMT technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1042–1050, May 2006.
- [27] H. Chang, X. Cao, U. Mishra, and R. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 5, pp. 604–615, May 1997.
- [28] A. Georgiadis, A. Collado, and A. Suarez, "New techniques for the analysis and design of coupled-oscillator systems," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 11, pp. 3864–3877, Nov. 2006.
- [29] D. K. Shaeffer and S. Kudszus, "Performance-optimized microstrip coupled VCOs for 40-GHz and 43-GHz OC-768 optical transmission," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1130–1138, Jul. 2003.
- [30] F. Ramirez, M. Penton, S. Sancho, and A. Suarez, "Stability analysis of oscillation modes in quadruple-push and rucker's oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 11, pp. 2648–2661, Nov. 2008.
- [31] A. Collado and A. Georgiadis, "Nonlinear mode analysis and optimization of a triple-push oscillator," *IEEE Microw. Compon. Lett.*, vol. 18, no. 8, pp. 545–547, Aug. 2008.
- [32] Y.-L. Tang and H. Wang, "Triple-push oscillator approach: Theory and experiments," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1472–1479, Oct. 2001.
- [33] R. York, "Nonlinear analysis of phase relationships in quasi-optical oscillator arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 10, pp. 1799–1809, Oct. 1993.
- [34] H. Xiao, T. Tanaka, and M. Aikawa, "A Ka-band quadruple-push oscillator," in *IEEE MTT-S. Dig.*, Jun. 2003, pp. 889–892.
- [35] S. Yen and T. Chu, "An Nth-harmonic oscillator using an N-push coupled oscillator array with voltage-clamping circuits," in *IEEE MTT-S. Dig.*, Jun. 2003, pp. 2169–2172.
- [36] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrizi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.
- [37] A. Goel and H. Hashemi, "Injection locking in concurrent dual-frequency oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 8, pp. 1834–1845, Aug. 2008.
- [38] F. Verhulst, *Nonlinear Differential Equations and Dynamical Systems*. Berlin, Germany: Springer, 1990.
- [39] B. Catli and M. M. Hella, "A 30-GHz triple-push oscillator on silicon for mm-wave applications," in *IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 24–27, 2009, pp. 2037–2040.
- [40] C. Cao and K. K. O, "Millimeter-wave voltage-controlled oscillator in 0.13  $\mu\text{m}$ ," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1297–1304, Jun. 2006.
- [41] D. D. Kim, H. Wohlmuth, and W. Simburger, "A 70 GHz manufacturable complementary LC-VCO with 6.14 GHz tuning range in 65 nm SOI CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 540–541.
- [42] J. Borremans, M. Dehan, K. Scheir, M. Kuijk, and P. Wambacq, "VCO design for 60 GHz using differential shielded inductors in 0.13  $\mu\text{m}$ ," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, 2008, pp. 135–138.
- [43] L. Lianming, P. Reynaert, and M. Steyaert, "Design and analysis of a 90 nm mm-wave oscillator using inductive-division LC tank," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1950–1958, Jul. 2009.
- [44] T. Nakamura, T. Masuda, K. Washio, and H. Kondoh, "A 59 GHz push-push VCO with 13.9 GHz tuning range using loop-ground transmission line for a fullband 60 GHz transceiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 496–497.
- [45] N. Pohl, H.-M. Rein, T. Musch, K. Aufinger, and J. Hausner, "SiGe bipolar VCO with ultra-wide tuning range at 80 GHz center frequency," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2655–2662, Oct. 2009.



**Burak Çatlı** (S'96) received the B.S. and M.S. degrees in electronic engineering from Istanbul Technical University, Istanbul, Turkey, in 1998 and 2001, respectively. He is currently working toward the Ph.D. degree in the Electrical, Computer, and Systems Engineering Department at Rensselaer Polytechnic Institute, Troy, NY.

He was a graduate student and research assistant in the Electronic and Communication Engineering Department, Istanbul Technical University between 1998 and 2005. From 1998 to 2005, he was a design engineer with the ETA-IC Design Center, Istanbul, Turkey, developing RF front-end blocks and high-speed high-resolution data converter systems for industrial and military applications. During summers of 2006 and 2007, he was with RF Micro Devices, Boston, MA, and during summer of 2008, he was with Qualcomm Inc., Santa Clara, CA. His research interests are in the area of analog and mm-wave circuit design for integrated communication systems.

Mr. Çatlı was awarded at the 2007 Analog Devices Mixed Signal Design Contest for the best industrial grade design and is recipient of 2007 Veera and Arjun Saxena Fellowship in Microelectronics.



**Mona Mostafa Hella** (S'96–M'01) received the B.Sc. and Masters degrees with Honors from Ain-Shams University, Cairo, Egypt, in 1993 and 1996, and the Ph.D. degree from the Ohio State University, Columbus, in 2001, all in electrical engineering.

From 1993 to 1997, she was a teaching and research assistant at Ain Shams University. From 1997 to 2001, she was a research assistant at the Ohio State University. She was with the Helsinki University of Technology (HUT), Espoo, Finland, as

a visiting scholar in the summer of 1998, and with the analog group at Intel Corporation, Chandler, AZ, in summer 1999. She was a senior designer at Spirea AB, Stockholm, Sweden, working on CMOS power amplifiers from 2000 to 2001. From 2001 to 2003, she was a senior designer at RFMD Inc, Billerica, MA, working on optical communication systems and silicon-based wireless systems. She joined the Electrical, Computer and Systems Engineering Department at Rensselaer Polytechnic Institute, Troy, NY, as an Assistant Professor in 2004. Her research interests include the areas of mixed-signal and RFIC design for wireless and wire-line applications.

## Triple Push Operation for Combined Oscillation/Division Functionality in Millimeter-Wave Frequency Synthesizers