ECSE - 2210

Microelectronics Technology

Spring 2014

Final Exam

Solution

Problem 1 : Si n-channel MESFET

with $L_G = 1.0\,\mu m$ $W_{ch} = 0.3\,\mu m$ $Z = 100\,\mu m$

and $N_D = 1 \times 10^{17}\,cm^{-3}$

(a) Phosphorus (P) can be used as an n-type dopant. P is a group-V element. Si is a group IV element. Since P has one more valence electron than Si, P acts as a donor.

(b) Barrier height $e\Phi_B = 1\,eV$ or $\Phi_B = 1.0\,V$

Depletion width of metal-semiconductor junction:

$$W_D = \sqrt{\frac{2\varepsilon}{eN_D}\left(\Phi_B - V_{GS}\right)}$$

Solving this eqn. for V_{GS} and using $W_D = W_{ch}$ and $V_{GS} = V_{PO}$, we obtain:

$$\left(\Phi_B - V_{PO}\right) = \frac{eN_D}{2\varepsilon} W_{ch}^2$$

$$-V_{PO} = \frac{eN_D}{2\varepsilon} W_{ch}^2 - \Phi_B$$

$$= \frac{1.6 \times 10^{-19}\,C\ 10^{17}\,cm^{-3}\ Vm}{2 \times 11.9 \times 8.85 \times 10^{-12}\,As}\left(0.3 \times 10^{-4}\,cm\right)^2 - 1.0\,V$$

$$-V_{P0} = \frac{1.6\ 10^{-2}\ \mathrm{cm}^{-3}\ V\ 100\,\mathrm{cm}}{210.6 \times 10^{-12}}\ 9 \times 10^{-10}\ \mathrm{cm}^{2} - 1.0V$$ ③

$$= \frac{160 \times 9}{210.6} V - 1.0V = 6.84V - 1.0V = 5.84V$$

$$\Rightarrow V_{P0} = \underline{\underline{-5.84V}}$$

(c) Resistance of channel at $V_{GS} = 0$.

Depletion width at $V_{GS} = 0$:

$$W_D = \sqrt{\frac{2\varepsilon}{eN_D}\Phi_B}$$

$$= \sqrt{\frac{2 \times 11.9 \times 8.85 \times 10^{-12}\ \mathrm{As}\quad 1.0\,\mathrm{V}}{1.6 \times 10^{-19}\,\mathrm{C}\ 10^{17}\,\mathrm{cm}^{-3}\ \mathrm{Vm}}}$$

$$= \sqrt{131.6 \times 10^{-10}\ \mathrm{cm}^{3} \frac{1}{100\,\mathrm{cm}}} = \sqrt{131.6 \times 10^{-12}}\ \mathrm{cm}$$

$$= 11.5 \times 10^{-6}\,\mathrm{cm} = \underline{\underline{0.115\,\mu\mathrm{m}}}$$

Neutral (i.e. electrically conductive) channel height:

$$h = W_{ch} - W_D = 0.3\,\mu\mathrm{m} - 0.115\,\mu\mathrm{m} = \underline{\underline{0.185\,\mu\mathrm{m}}}$$

Resistance of channel:

$$R_{ch} = \rho \frac{l}{A} = \frac{1}{\sigma}\frac{L_G}{Z h} = \frac{1}{en\mu}\frac{L_G}{Z h}$$

$$R_{ch} = \frac{Vs}{1.6\times10^{-19}C \; 10^{17}\,cm^{-3} \; 1500\,cm^2} \; \frac{1\,\mu m}{100\,\mu m \; 0.185\,\mu m}$$

$$= \frac{Vs}{1.6 \times 15 \; As \; cm^{-1}} \; \frac{1}{18.5 \times 10^{-4}\,cm}$$

$$= 22.5 \frac{V}{A} = \underline{\underline{22.5\,\Omega}}$$

(d) Channel resistance at $V_{GS} = -10V$.

We calculated $V_{PO} = -5.84\,V$

Because V_{GS} exceeds V_{PO}, the channel is completely pinched off. Therefore the conductive channel height is zero ($h = 0$).

$$\Rightarrow \quad R_{ch} \underline{\underline{= \infty}}$$

Problem 2: GaN LED $P_{out} = 100\,mW$

$I_{Input} = 100\,mA$

(a) GaN bandgap energy $E_g = 3.425\,eV$

$$\Rightarrow E = h\nu = h\frac{c}{\lambda}$$

$$\Rightarrow \lambda = \frac{hc}{E_g} = \frac{6.626\times10^{-34}\,Js\; 3\times10^{8}\,\frac{m}{s}}{3.425\,eV}$$

$$= \frac{19.9\times10^{-26}\,J\,m}{3.425\times1.6\times10^{-19}\,CV} = 3.63\times10^{-7}\,m$$

$$= \underline{\underline{363\,nm}}$$

(b) Photon flux = No. of photons per sec.

$$P_{out} = h\nu \times \text{Photon flux}$$

$$\Rightarrow \text{Photon flux} = \frac{P_{out}}{h\nu} = \frac{100\,mW}{3.425\,eV}$$

$$= \frac{0.1\,J s^{-1}}{3.425\times1.6\times10^{-19}\,CV} = \underline{\underline{1.82\times10^{17}\,\frac{1}{s}}}$$

(c) Electron flux = No. of electrons injected per sec.

$$\text{Electron flux} = \frac{I}{e} = \frac{100\,mA}{1.6\times10^{-19}\,C} = \frac{0.1\,A}{1.6\times10^{-19}\,As}$$

$$= \underline{\underline{6.25\times10^{17}\,\frac{1}{s}}}$$

(d) Quantum efficiency = QE

$$QE = \frac{\text{Photon flux}}{\text{Electron flux}} = \frac{\text{No. of photons per sec.}}{\text{No. of electrons per sec.}}$$

$$= \frac{1.82 \times 10^{17} \frac{1}{s}}{6.25 \times 10^{17} \frac{1}{s}} = 0.291 = \underline{\underline{29.1\%}}$$

(e) Improving power efficiency of an LED.

(i) Reduce series resistance, R_s.

A reduced R_s will produce less heat and thus increase the power efficiency.

(ii) Increase the purity of the semiconductor material.

Fewer impurities will cause less non-radiative recombination (recall "luminescence killers") thereby increasing the power efficiency.

Problem 3: Si pnp bipolar junction transistor

$\beta = 50 \quad W_B = 1.5\,\mu m \quad N_D = 5\times10^{17}\,cm^{-3} \quad \beta = 50$

(a) Current amplification in common-base configuration

$\beta = \frac{\alpha}{1-\alpha}$ Solving this eqn. for α:

$$(1-\alpha)\,\beta = \alpha$$

$$\left(\frac{1}{\alpha} - 1\right)\beta = 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\alpha = \frac{1}{\frac{1}{\beta}+1} \Rightarrow \alpha = \frac{\beta}{\beta+1}$$

$$\alpha = \frac{50}{50+1} = \frac{50}{51} = 0.98$$

(b) Base trasport factor.

Preliminary step: $L_p = \sqrt{D_p \tau} = \sqrt{12\,\frac{cm^2}{s}\,10^{-6}\,s}$

$= 3.46\times10^{-3}\,cm = 34.6\,\mu m$

Base transport factor

$$B = 1 - \frac{1}{2}\left(\frac{W_B}{L_p}\right)^2 = 1 - \frac{1}{2}\left(\frac{1.5\,\mu m}{34.6\,\mu m}\right)^2$$

$= 0.999$

(c) Emitter efficiency

$$\alpha = \gamma B \Rightarrow \gamma = \frac{\alpha}{B} = \frac{0.98}{0.999} = \underline{\underline{0.981}}$$

(d) Emitter doping

Preliminary step: $L_n = \sqrt{D_n \tau} = \sqrt{39 \frac{cm^2}{s} 10^{-6} s}$

$$= 6.24 \times 10^{-3}\ cm = \underline{\underline{62.4\ \mu m}}$$

Emitter efficiency:

$$\gamma = 1 - \frac{D_n}{D_p} \frac{W_B}{L_n} \frac{N_D}{N_A}$$

Solving this eqn. for N_A yields

$$N_A = (1-\gamma)^{-1} \frac{D_n}{D_p} \frac{W_B}{L_n} N_D$$

$$= (1-0.981)^{-1} \frac{39 \frac{cm^2}{s}}{12 \frac{cm^2}{s}} \frac{1.5\ \mu m}{62.4\ \mu m} \times 5 \times 10^{17} cm^{-3}$$

$$= 52.6 \times 3.25 \times 0.0240 \times 5 \times 10^{17} cm^{-3}$$

$$= \underline{\underline{2.05 \times 10^{18} cm^{-3}}}$$

Problem 4: n-channel MOSFET with SiO_2.

(a) Transconductance in saturation regime

$$g_{m,sat} = \frac{\varepsilon_{ox} \mu_n Z}{d_{ox} L_G} (V_{GS} - V_{th})$$

(b) For $V_{GS} = V_{th} \Rightarrow g_{m,sat} = 0$

(c) The transconductance can be increased by:

(i) Reducing L_G (gate length)

(ii) Reducing d_{ox} (oxide thickness)

(iii) Increasing ε_{ox} (of the SiO_2)

(d) Methods employed:

(i) Scaling down the lateral dimensions of the MOSFET including L_G.

(ii) Scaling down the vertical dimensions of the MOSFET including d_{ox}

(iii) Use an alternative oxide (other than SiO_2) that has a higher relative dielectric constant (ε_r) than SiO_2.