

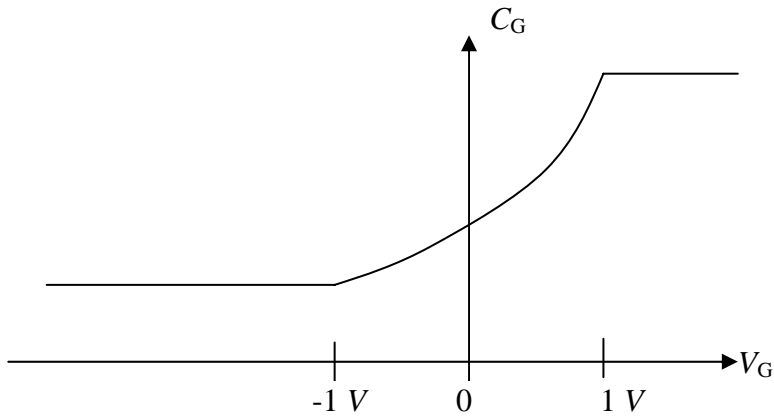
**ECSE-2210 Microelectronics Technology**  
**Fall 2005**  
**Class Activity 31**

Consider a MOS capacitor fabricated on a p-Si doped to  $10^{17} \text{ cm}^{-3}$  acceptors. Assume that the oxide thickness is  $x_{\text{ox}} = 20 \text{ nm} = 200 \text{ \AA}$ ,  $\Phi_{\text{ms}} = -1.05 \text{ eV}$ , and ignore  $Q_i$ . Plot the  $C_G$ - $V_G$  characteristics if the gate voltage is changed very slowly from  $-5 \text{ V}$  to  $+5 \text{ V}$ . Calculate all numerical values.

1. For the above case, qualitatively plot the  $C_G$ - $V_G$  characteristics if the gate voltage is rapidly changed from  $-5 \text{ V}$  to  $+5 \text{ V}$ .
2. (If time permits) Calculate all numerical values for problem 2. (Hint: Use equation 16.28 relating  $V_G$  to  $(\phi_s)^{1/2}$  and solve for  $(\phi_s)^{1/2}$ . From  $(\phi_s)^{1/2}$  find  $\phi_s$ . Then calculate  $W$ . For  $V_G$  in equation 16.28, use  $6.05 \text{ V}$  taking into account the flat-band voltage  $V_{\text{FB}} = -1.05 \text{ V}$ ).

3. Explain why a DRAM cell needs refreshing every few milliseconds.

4. The following  $C$ - $V$  curve is taken from a MOS capacitor fabricated on Si. The oxide thickness is  $x_{\text{ox}} = 0.1 \mu\text{m}$  and the gate metal is chosen such that  $\phi_{\text{ms}}$  is zero.



a. Calculate the net interface charges present in the oxide in  $\text{C}/\text{cm}^2$ .

b. What will be the threshold voltage, if there were no interface charges?

c. Is the substrate p-type or n-type?

