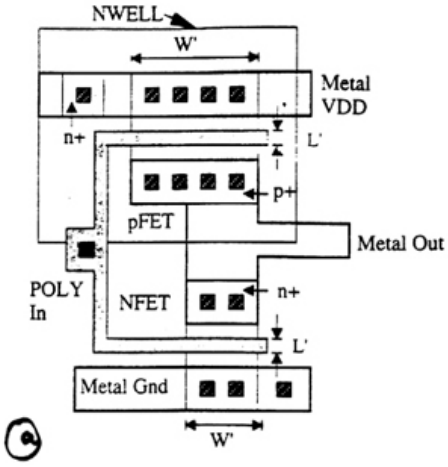
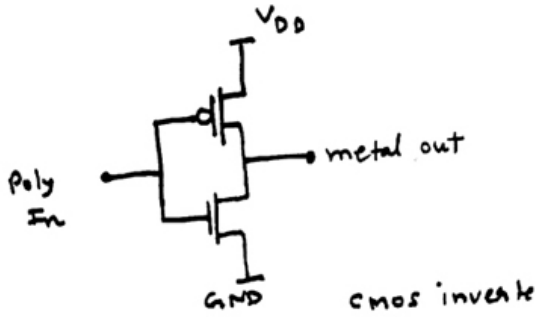
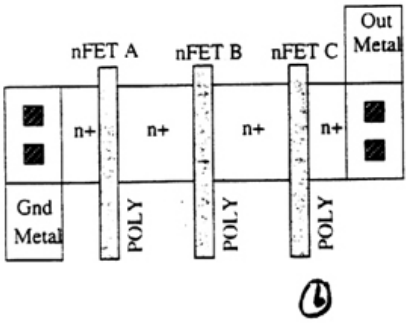
ECSE-2210 Microelectronics Technology
Fall 2005
Class Activity 34
(Refer to class handout)

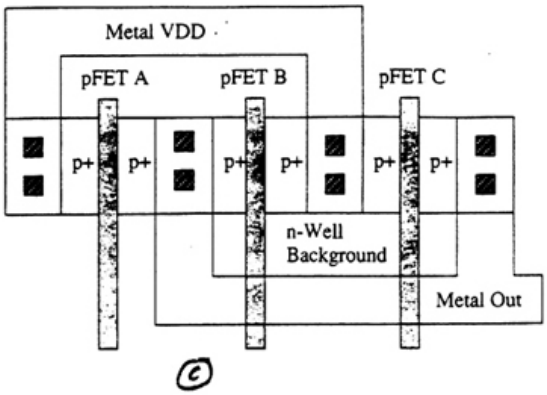
1. Masks should be designed such that the ploy-gate area overhangs the active area by a distance "*d*" as shown in the notes. Explain why.

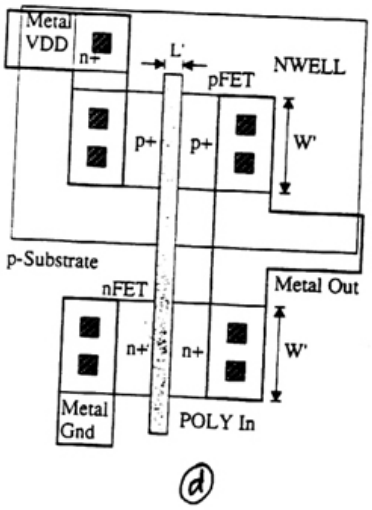
2. Some basic CMOS circuit layouts are shown on the next page. Draw the circuit they represent. The first one is done for you.

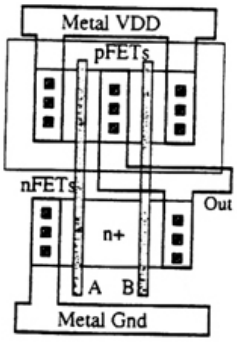

NWELL
W'
Metal
VDD
n+
L'
p+
pFET
Metal Out
POLY
In
NFET
n+
L'
Metal Gnd
W'
a

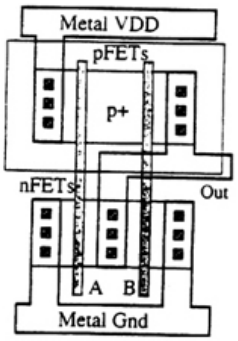

VDD
metal out
Poly
In
GND
cmos inverte


nFET A
nFET B
nFET C
Out
Metal
n+
n+
n+
n+
Gnd
Metal
POLY
POLY
POLY
b


Metal VDD
pFET A
pFET B
pFET C
p+
p+
p+
p+
p+
p+
n-Well
Background
Metal Out
c


Metal
VDD
n+
L'
pFET
NWELL
p+
p+
W'
p-Substrate
nFET
Metal Out
n+
n+
W'
Metal
Gnd
POLY In
d


Metal VDD
pFETs
nFETs
Out
n+
A
B
Metal Gnd
e


Metal VDD
pFETs
p+
nFETs
Out
A
B
Metal Gnd
f