

**ECSE-2210 Microelectronics Technology**  
**Fall 2005 Homework 10**

Reading Assignment: Chapter 17. Chapter 18 (pg. 645 – 662)

1. A MOSFET made with  $n^+$  poly-silicon gate has the following characteristics:

Oxide thickness  $x_{ox} = 500 \text{ \AA}$   
Doping in Si:  $N_A = 10^{16} \text{ cm}^{-3}$   
Interface oxide charges  $Q_i = 6.4 \times 10^{11} \times 1.6 \times 10^{-19} \text{ C/cm}^2$   
Area  $A = 1 \text{ cm}^2$

- a. Calculate the flat-band voltage  $V_{FB}$  for this device (Hint: Since the gate is made of  $n^+$ -poly-silicon, assume that the gate Fermi-level is at the conduction band edge. Since  $\Phi_{ms} = \Phi_m - \Phi_s$ , the magnitude of  $\Phi_{ms}$  in this case will be equal to  $(1/q)[E_F(\text{gate}) - E_F(\text{silicon})]$ ).
  - b. Calculate the threshold voltage,  $V_T$ , if the device were ideal. (This is the threshold voltage if the  $\Phi_{ms}$  were zero and there were no interface charges).
  - c. Calculate the actual threshold voltage,  $V_T$ , for this device taking into account  $\Phi_{ms}$  and the interface charges.
  - d. Plot the high frequency  $C_G - V_G$  characteristics for this device. Mark important points in the graph. (Ignore the presence of Source/Drain for this particular case).
  - e. Suppose we want to increase the threshold voltage by 1V (i.e.,  $\Delta V_T = +1 \text{ V}$ ), calculate the number of (**boron or phosphorus: choose one**) ions that should be implanted to silicon.
2. Suppose one makes an identical MOSFET as above, except that the gate material is made up of  $p^+$  silicon instead of  $n^+$  silicon. What will be the actual threshold voltage of the device? (Hint: No need to do detailed calculation here. Check which terms changes, and make the appropriate corrections.)