

# Chapter 17-1. MOSFET

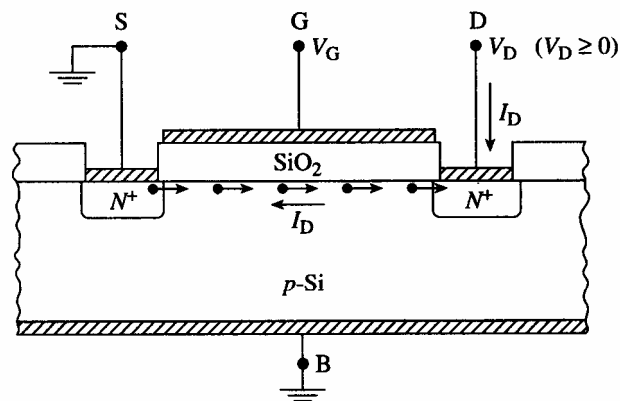
MOSFET based ICs have become dominant technology in the semiconductor industry.

We will study the following in this chapter:

Qualitative theory of operation

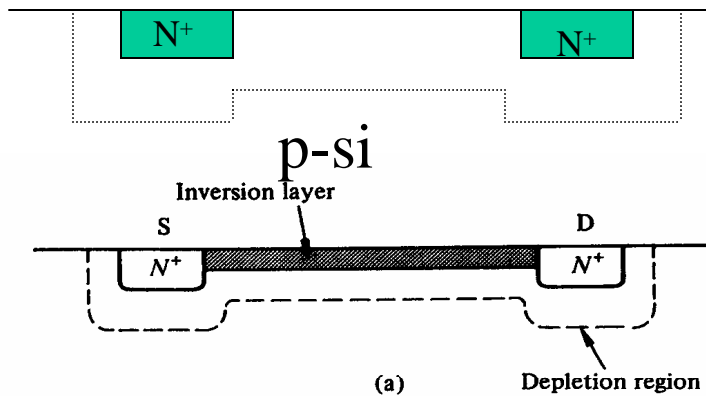
Quantitative  $I_D$  vs.  $V_{DS}$  characteristics

Small-signal equivalent circuits.



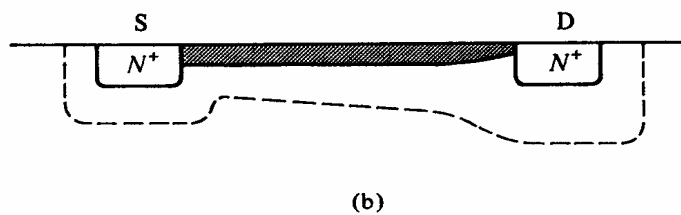
N-channel MOSFET  
Substrate: p-type Si

# Qualitative discussion: NMOS

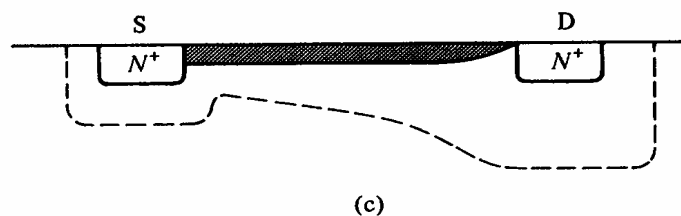


$0 < V_G < V_T$ ;  $V_{DS}$  small or large  
no channel, no current

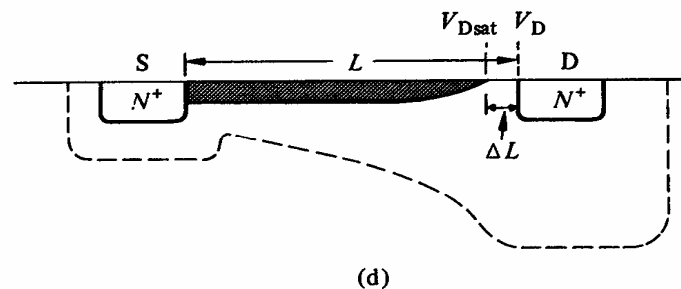
$V_G > V_T$ ;  $V_{DS} \approx 0$   
 $I_D$  increases with  $V_{DS}$



$V_G > V_T$ ;  $V_{DS}$  small,  $> 0$   
 $I_D$  increases with  $V_{DS}$ , but  
rate of increase decreases.



$V_G > V_T$ ;  $V_{DS} \approx \text{pinch-off}$   
 $I_D$  reaches a saturation value,  $I_{D,sat}$   
The  $V_{DS}$  value is called  $V_{DS,sat}$



$V_G > V_T$ ;  $V_{DS} > V_{DS,sat}$   
 $I_D$  does not increase further,  
saturation region.

$I_D$ - $V_{DS}$  characteristics for NMOS derived from qualitative discussions

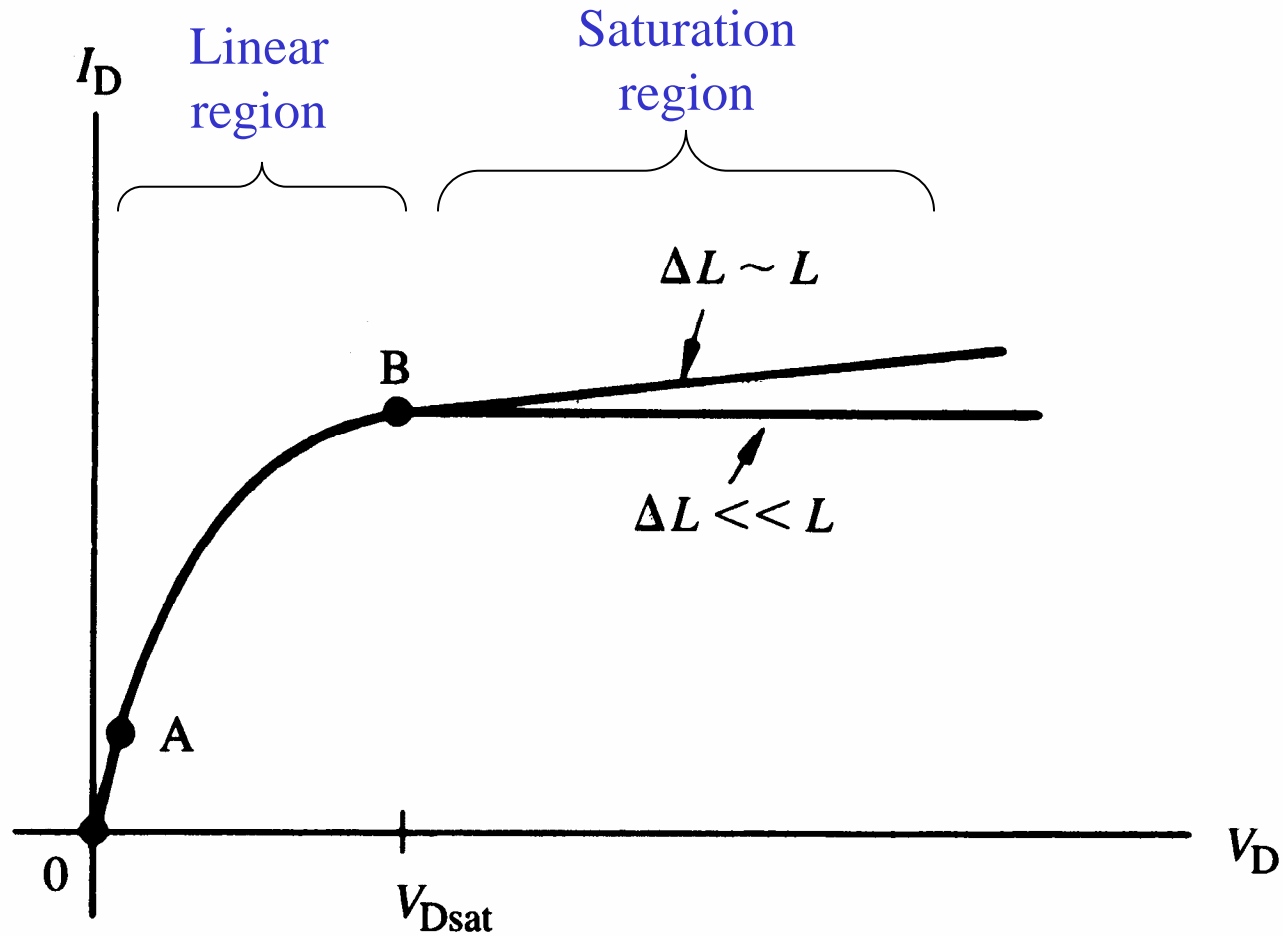


Figure 17.3

$I_D$ - $V_{DS}$  characteristics expected from a long channel ( $\Delta L \ll L$ ) MOSFET (n-channel), for various values of  $V_G$

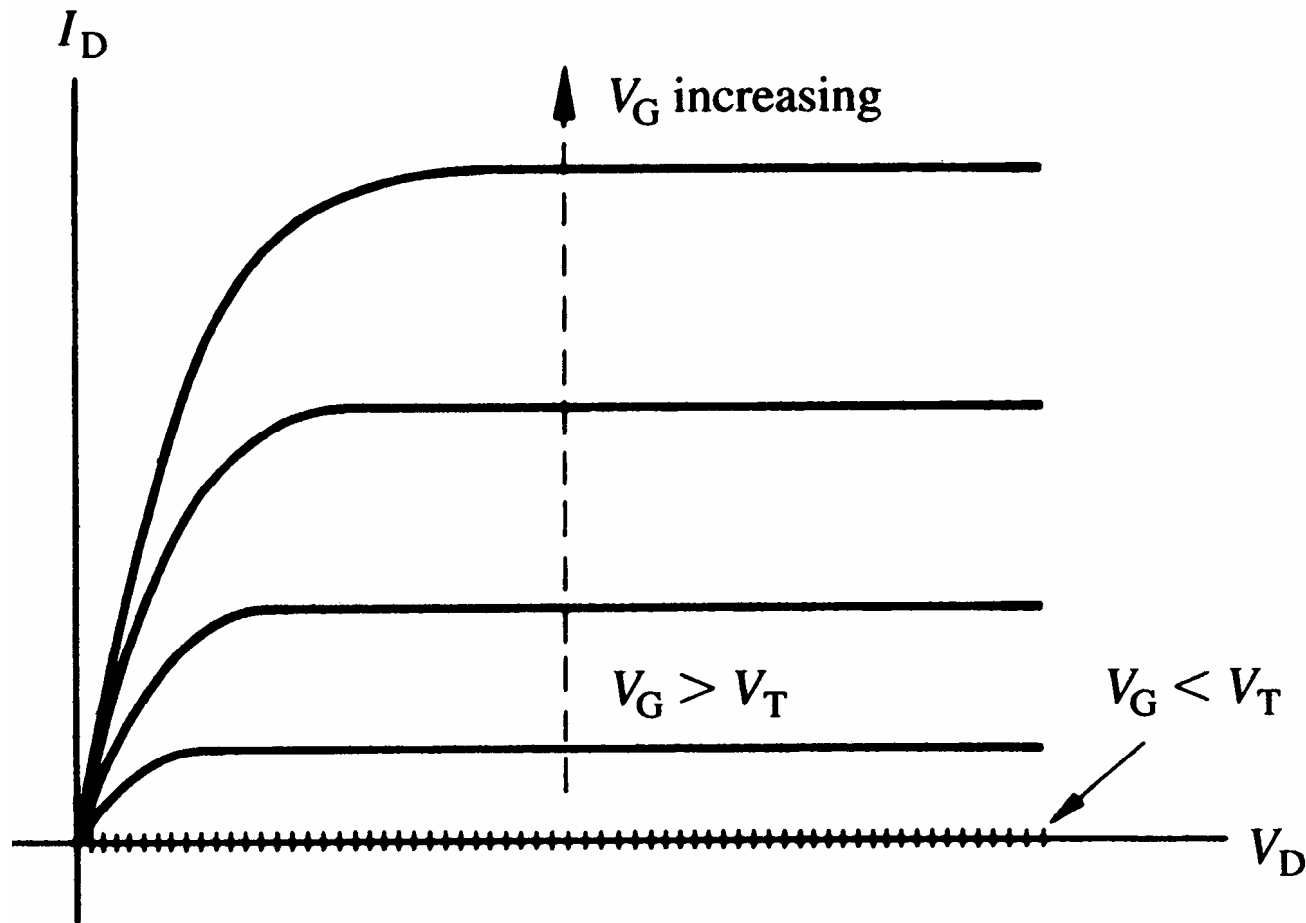


Figure 17.4

## Threshold voltage for NMOS and PMOS

When  $V_G = V_T$ ,  $\phi_s = 2\phi_F$ ; using equation 16.28, we get expression for  $V_T$ .

$$V_T = 2\phi_F + \left( x_{\text{OX}} \frac{\epsilon_{\text{Si}}}{\epsilon_{\text{OX}}} \left[ \frac{2qN_A}{\epsilon_{\text{Si}}} 2\phi_F \right]^{1/2} \right)$$

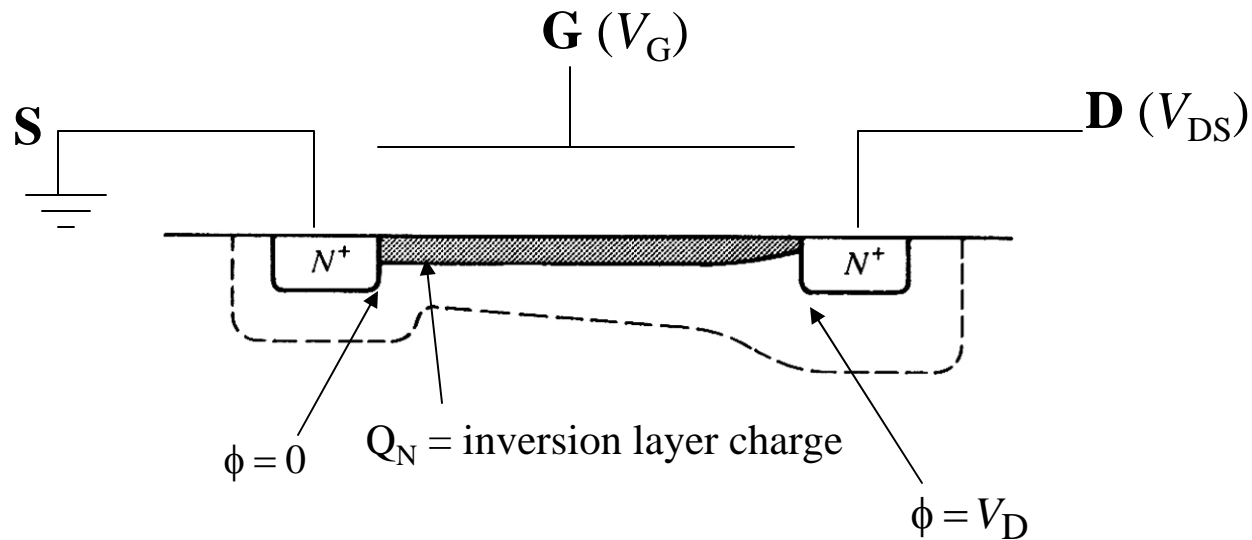
Ideal n-channel  
(p-silicon) device  
both terms positive

$$V_T = 2\phi_F + \left( -x_{\text{OX}} \frac{\epsilon_{\text{Si}}}{\epsilon_{\text{OX}}} \left[ \frac{2qN_D}{\epsilon_{\text{Si}}} / 2\phi_F / \right]^{1/2} \right)$$

Ideal p-channel  
(n-silicon) device  
both terms negative

$$\epsilon_{\text{Si}} / \epsilon_{\text{OX}} = (\epsilon_{\text{Si}} \epsilon_0) / (\epsilon_{\text{OX}} \epsilon_0) = 11.9 / 3.9 \approx 3$$

## Quantitative $I_D$ - $V_{DS}$ relationships



Let  $\phi$  be the potential along the channel

For  $V_G < V_T$ , Inversion layer charge is zero.

For  $V_G > V_T$ ,  $Q_n(y) = -Q_G = -C_{ox} (V_G - \phi - V_T)$

In general,  $J_n = q \mu_n n E$  when the diffusion current is neglected.  
Here, current  $I_D$  is the same everywhere, but  $J_n$  (current density) can vary from position to position.

Device structure, dimension, and coordinate orientations assumed in the quantitative analysis

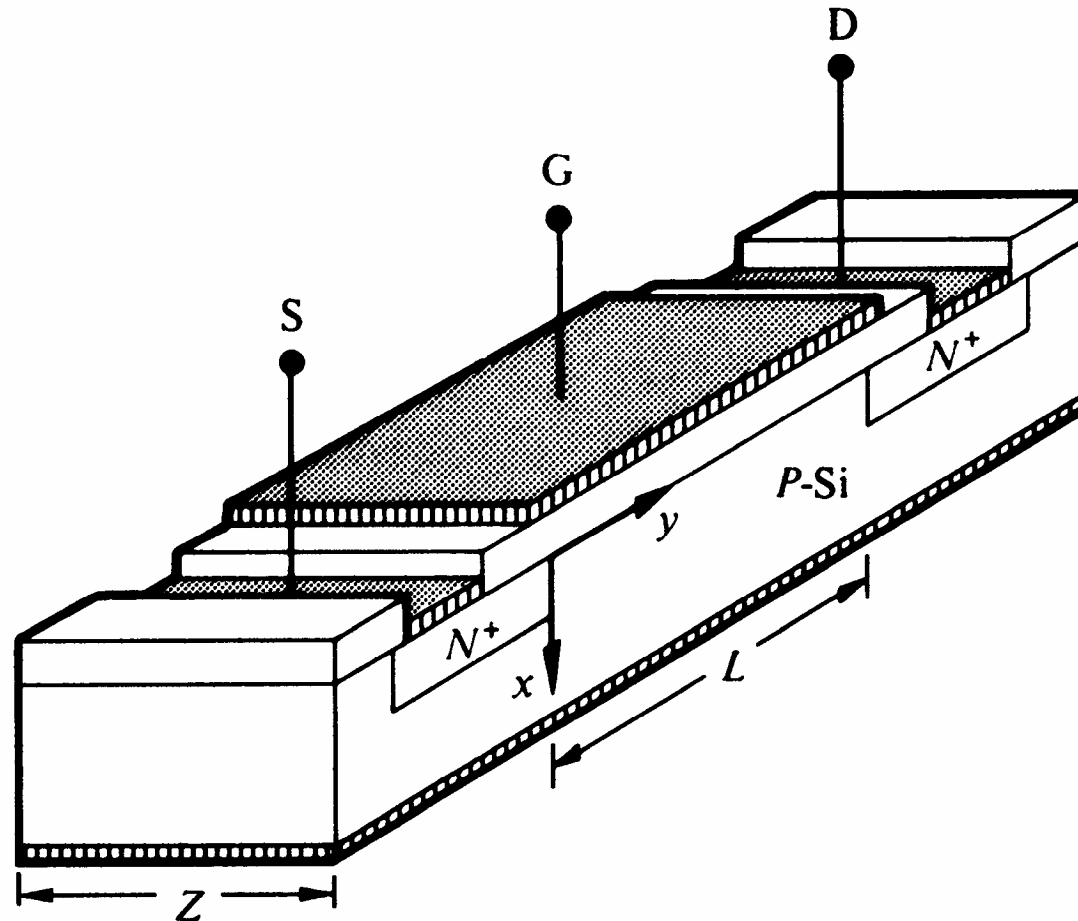


Figure 17.6

## Quantitative $I_D$ - $V_{DS}$ relationships (Shockley model)

$$J_n = J_{ny} = q\mu_n nE = -q\mu_n n \frac{d\phi}{dy} \quad \text{since } E(y) = -\frac{d\phi}{dy}$$

To find current, we have to multiply the above with area, but  $J_{ny}$ ,  $n$ , etc. are functions of  $x$  and  $z$ . Hence,

$$\begin{aligned} I_D &= \iint J_{ny} \, dx \, dz = Z \int J_{ny} \, dx = -Z\mu_n \frac{d\phi}{dy} \int qn \, dx \\ &= -Z\mu_n \frac{d\phi}{dy} Q_n(y) \quad Q_n(y) = \text{charge / unit area} \end{aligned}$$

Integrating the above equation, and noting that  $I_D$  is constant, we get

$$I_D = -\frac{Z}{L} \mu_n \int_0^{V_{DS}} Q_n(y) \, d\phi$$

Since we know expression for  $Q_n(y)$  in terms of  $\phi$ , we can integrate this to get  $I_D$

## Quantitative $I_D$ - $V_{DS}$ Relationships (cont.)

$$I_D = \frac{Z\mu_n}{L} C_{ox} \left[ (V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad 0 < V_{DS} < V_{DS,sat} \ ; \ V_G > V_T$$

$I_D$  will increase as  $V_{DS}$  is increased, but when  $V_G - V_{DS} = V_T$ , pinch-off of channel occurs, and current saturates when  $V_{DS}$  is increased further. This value of  $V_{DS}$  is called  $V_{DS,sat}$ . i.e.,  $V_{DS,sat} = V_G - V_T$  and the current when  $V_{DS} = V_{DS,sat}$  is called  $I_{D,sat}$ .

$$I_{D,sat} = \frac{Z\mu C_{ox}}{2L} (V_G - V_T)^2 \quad V_D > V_{DS,sat} \ ; \ V_G > V_T$$

Here,  $C_{ox}$  is the oxide capacitance per unit area,  $C_{ox} = \epsilon_{ox} / x_{ox}$

## Example 1

Plot the  $I_D$  vs.  $V_{DS}$  characteristics for an NMOS with the following parameters:

Substrate doping:  $10^{16} \text{ cm}^{-3}$ . Oxide thickness = 100 nm

Gate width = 15  $\mu\text{m}$ ; Gate length = 1  $\mu\text{m}$ . Assume  $\mu_n = 500 \text{ cm}^2/(\text{Vs})$

Find  $C_{ox}$ :  $C_{ox} = \epsilon_{ox} / x_{ox} = 33.3 \text{ nF/cm}^2$

$$V_T = 2\phi_F + \left( x_{ox} \frac{\epsilon_{Si}}{\epsilon_{ox}} \left[ \frac{2qN_A}{\epsilon_{Si}} 2\phi_F \right]^{1/2} \right) = 2.15 \text{ V}$$

$$I_{D,sat} = \frac{Z\mu C_{ox}}{2L} (V_G - V_T)^2 \quad V_{DS} > V_{DS,sat} \quad ; \quad V_G > V_T$$

$$V_{DS,sat} = V_G - V_T$$

Find  $I_{D,sat}$  for different values of  $V_G$  and plot the graph