

## Chapter 18. Non-ideal MOS

So far, we have discussed MOS characteristics making some assumptions - calling it “**ideal**”.

- Assumed that the  $\Phi_M = \Phi_S$ , i.e. the bands are flat when no voltage is applied.
- Assumed that the oxide and oxide-semiconductor interface are free of charges.

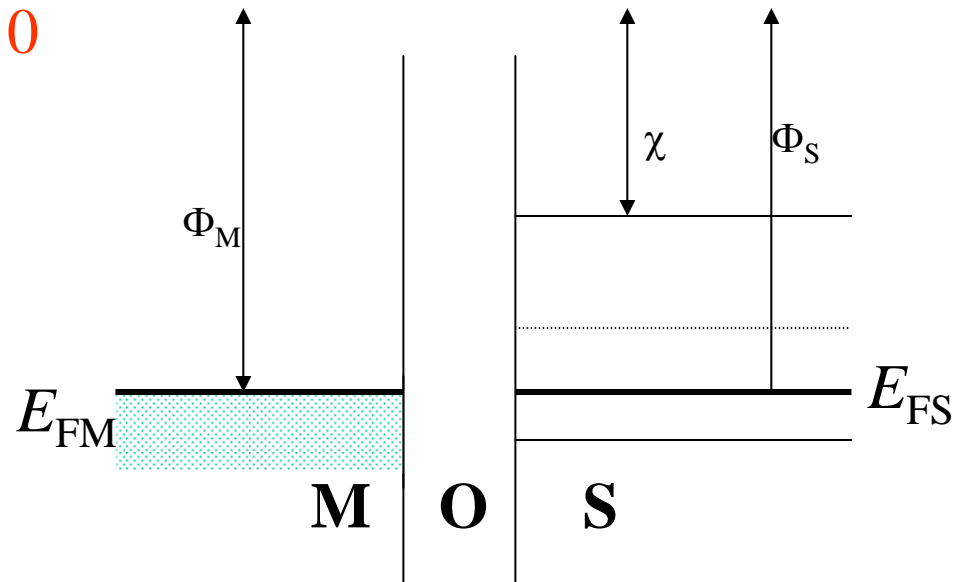
These assumptions do not hold good in an actual MOS device, and we have to consider the deviations from the ideal case. For the purpose of discussions, we call these as “**real**”.

# Metal-semiconductor work function difference - ideal

When  $\Phi_M = \Phi_S$ , the Fermi level is aligned before we make the device. So, when the MOS structure is made, the band remains flat when the applied gate voltage is zero.

Assumption  $\Phi_{MS} = \Phi_M - \Phi_S = 0$

Flat band condition



# Metal-semiconductor work function difference - real

$\Phi_M$  depends on the metal.

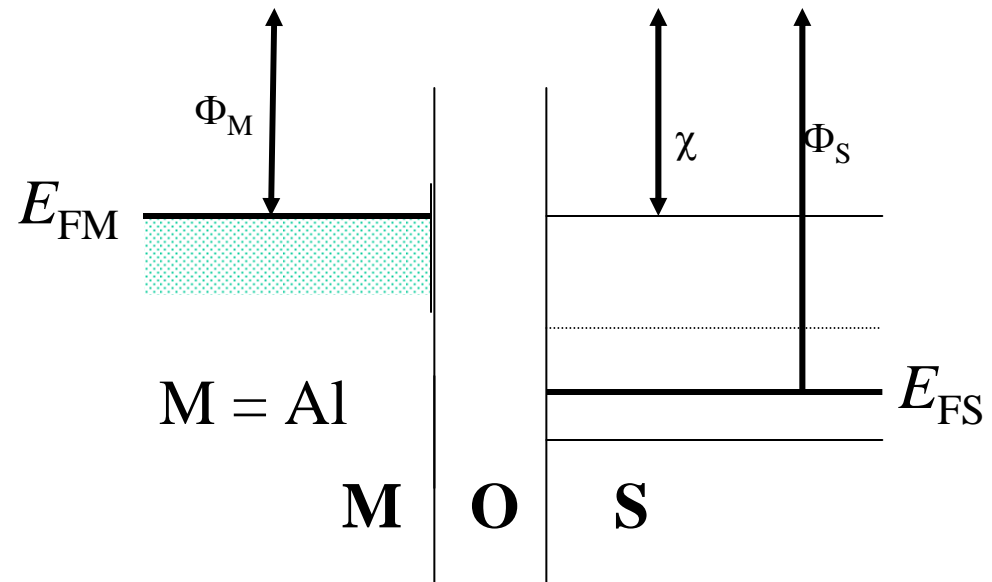
Example:  $\Phi_M(\text{Al}) \approx 4 \text{ eV}$ ,  $\Phi_M(\text{Au}) \approx 5.1 \text{ eV}$

$\Phi_S$  depends on the semiconductor doping.

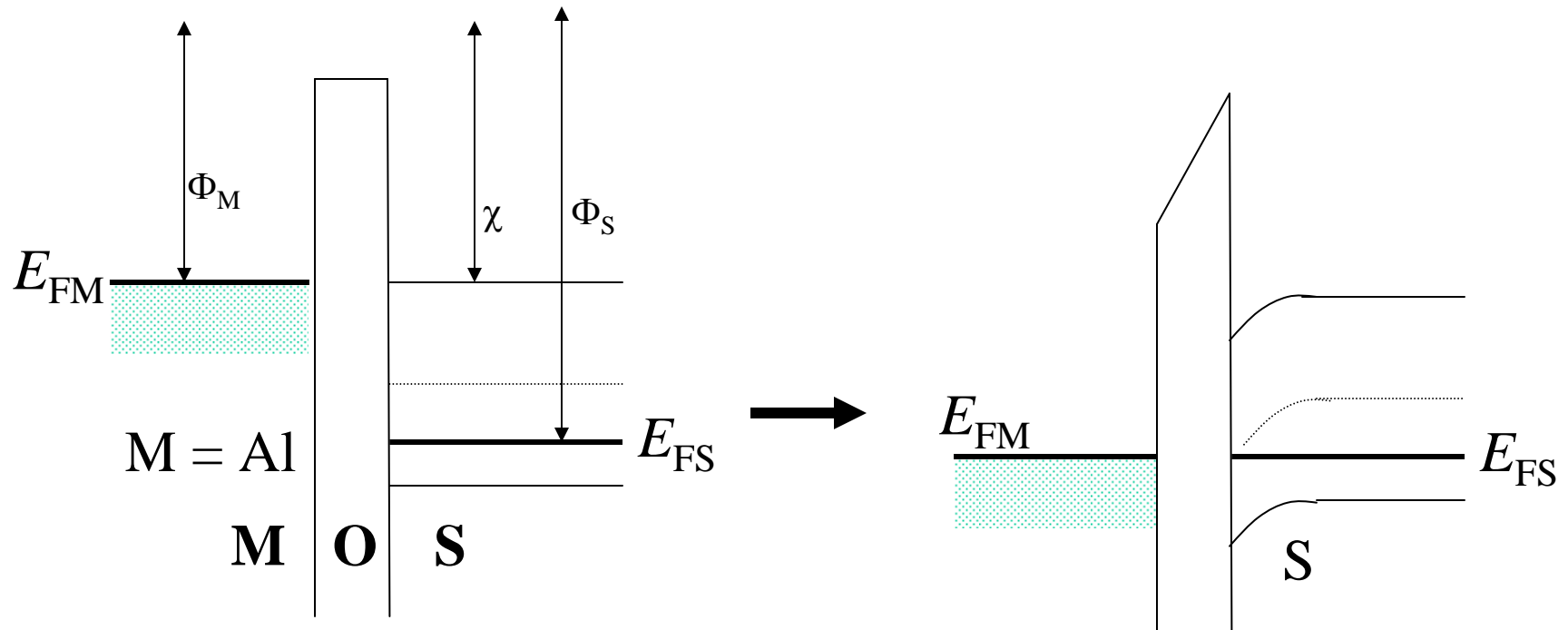
$$\Phi_S = \chi + (E_C - E_F)_{\text{FB}}$$

So,  $\Phi_{\text{MS}} = \Phi_M - \Phi_S \neq 0$   
in a “**real**” device.

So, actual band alignment before making the MOS-C structure looks as shown for Al-Si (p)



# Band diagram for $\Phi_{MS} = \Phi_M - \Phi_S \neq 0$



We have to apply a gate voltage =  $\Phi_{MS}/q$  to get flat-band condition.

## Polysilicon gate MOS

Modern day devices generally use heavily doped polysilicon as the gate material.

For p<sup>+</sup>-polysilicon gate,  $E_{FM}$  can be assumed to be at  $E_V$ .

For n<sup>+</sup>-polysilicon gate,  $E_{FM}$  can be assumed to be at  $E_C$ .

Question: If the substrate is intrinsic silicon, and the gate material is p<sup>+</sup>-polysilicon, calculate  $\Phi_{MS}$ . ( $\Phi_{MS} = E_g / 2 = 0.55 \text{ eV}$ )

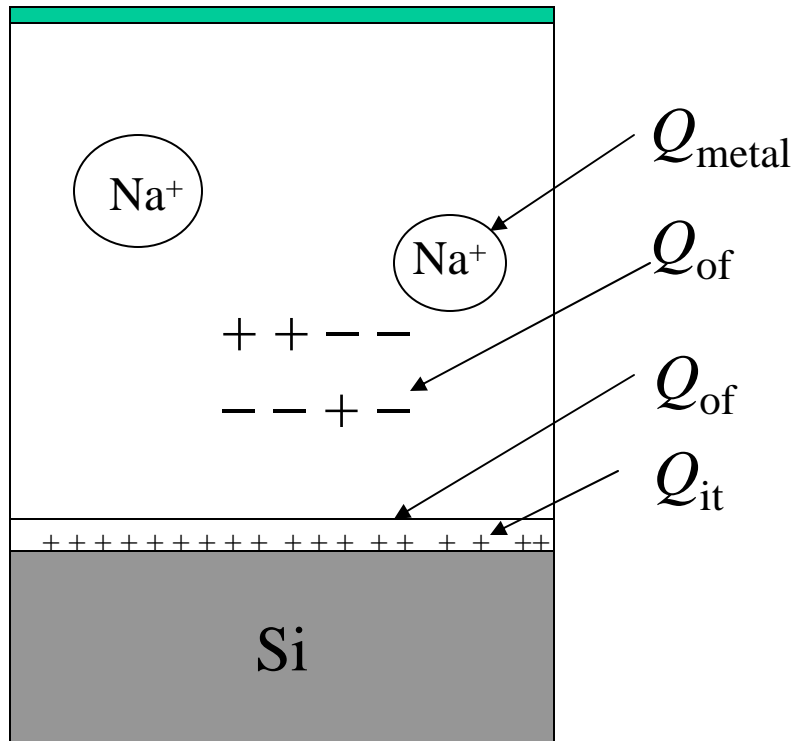
What is the voltage that has to be applied to the gate to get flat-band condition?  $V_G = 0.55 \text{ eV}/q = 0.55 \text{ V}$

Question: If the substrate is n<sup>+</sup>-silicon, and the gate material is p<sup>+</sup>-polysilicon, calculate  $\Phi_{MS}$ . ( $\Phi_{MS} = + 1.1 \text{ eV}$ )

Show  $\Phi_{MS}$  by drawing the band diagram.

## Interface and oxide charges

For the “ideal” device, we have assumed that the oxide and the interface is devoid of any excess charges. This is not true in practice.



Assume that all these charges are situated close to the interface on the oxide side (even though they aren't) and their concentration is  $\approx Q_i$  Coulombs/cm<sup>2</sup>.

$Q_i$  = net interface charges in C/cm<sup>2</sup>

## Effect of interface charges, $Q_i$ (C/cm<sup>2</sup>)

The interface charge  $Q_i$  in the oxide (assumed positive) will induce some negative charges ( $-Q_i$  /cm<sup>2</sup>) in the semiconductor. The effect is as though we have applied a positive gate voltage to the gate, and the negative charges in the semiconductor causes band bending. To get “flat-band” condition, we have to apply a negative voltage to the gate.

$$\left. \begin{array}{l} \text{Voltage to be applied to the} \\ \text{gate to get flat-band condition} \end{array} \right\} = -\frac{Q_i}{C_{\text{OX}}} \quad \text{where} \quad C_{\text{OX}} = \frac{\epsilon_{\text{OX}}}{x_{\text{OX}}}$$

$Q_i$  is usually positive (but can be both positive or negative in general).

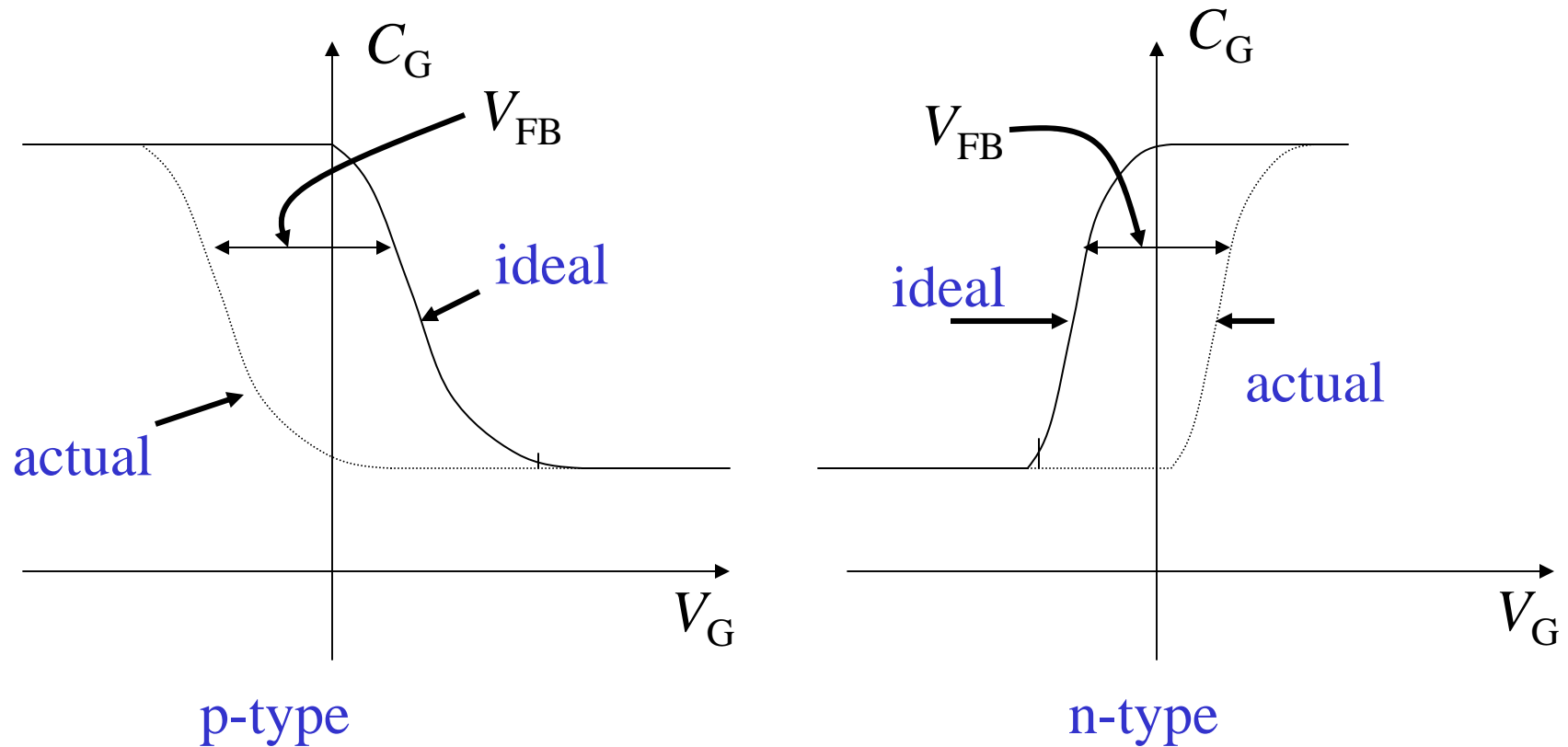
## Effects of work function difference and interface charges

If we consider the effects of work function difference and the interface charges, the silicon band diagram may not be “flat” even when no voltage is applied to the gate. Hence, a correction has to be applied to the threshold voltage calculations carried out earlier assuming “ideal” MOS conditions.

$$V_{\text{FB}} = \frac{1}{q} \Phi_{\text{MS}} + \left( -\frac{Q_{\text{i}}}{C_{\text{ox}}} \right) = \text{voltage to be applied to the gate to get flat band condition.}$$

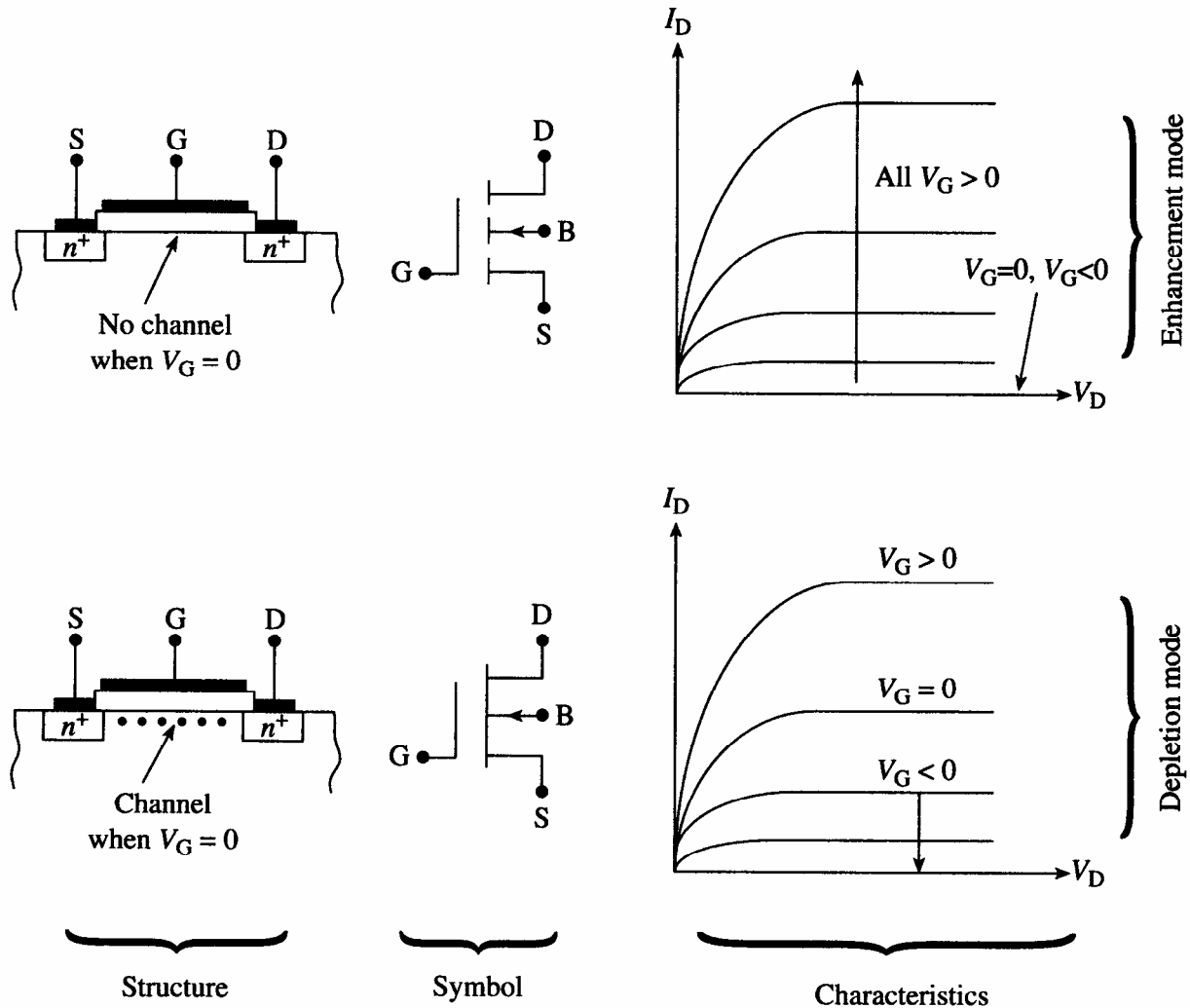
$$V_{\text{T}} = V_{\text{FB}} + V_{\text{T}}' \quad \text{where } V_{\text{T}}' \text{ is the threshold voltage assuming ideal conditions (using equation 17.1 in text).}$$

# Effects of $\Phi_{MS}$ and $Q_i$ on $C_G$ - $V_G$ characteristics of MOS-capacitor



A horizontal shift in C-V curve is observed. Routinely used to characterize MOS-C during IC fabrication.

# Enhancement and depletion mode MOSFETs

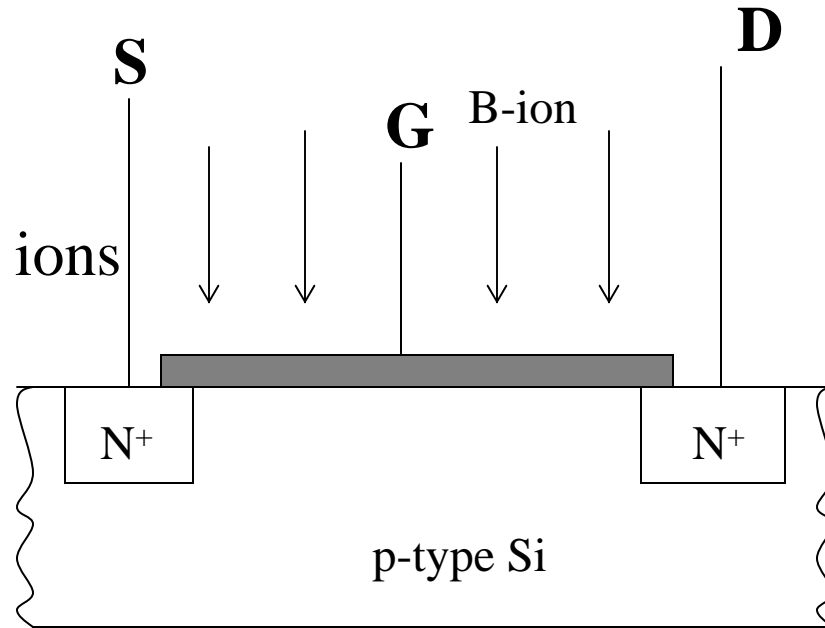


Device is "off" when  $V_G = 0 \Rightarrow$  enhancement-mode MOSFET  
 Device is "on" when  $V_G = 0 \Rightarrow$  depletion-mode MOSFET

# Threshold adjustment using ion implantation

Boron  $\rightarrow$  (+) ions

Phosphorous  $\rightarrow$  (-) ions



$$\Delta V_T = \frac{Q_{\text{ion}}}{C_{\text{OX}}}$$

$$= - \left[ \frac{-qB_{\text{dose}}}{C_{\text{OX}}} \right]$$

= positive shift for acceptor implantation

$$= - \left[ \frac{qP_{\text{dose}}}{C_{\text{OX}}} \right]$$

= negative shift for donor implantation

$B_{\text{dose}}$  = # of boron ions/cm<sup>2</sup> ;  $P_{\text{dose}}$  = # of phosphorus ions/cm<sup>2</sup>

## Example 1

Consider an NMOS with oxide thickness of 0.1  $\mu\text{m}$ . The threshold voltage measured to be 0.5 V. Calculate the boron or phosphorous ions to be implanted to make  $V_T$  equal to 2 V.

$\Delta V_T = +1.5 \text{ V} \rightarrow$  a positive shift. So use boron ions

$$C_{\text{ox}} = \frac{3.9 \times 8.85 \times 10^{-14} \text{ F/cm}}{0.1 \times 10^{-4} \text{ cm}} = 3.45 \times 10^{-8} \text{ F/cm}^2$$

$$\Delta V_T = - \left[ - \frac{q B_{\text{ions}}}{C_{\text{ox}}} \right] \quad \text{Calculate density of B ions. } (3.2 \times 10^{11} \text{ ions/cm}^2)$$

During IC fabrication, ion-implantation is routinely used to tailor the the threshold voltage MOSFET device.