

ECSE 2210 Microelectronics Technology

Sample Quiz 3

SOLUTIONS

- General note: -  $kT = 0.0259 \text{ eV}$ ;  $kT/q = 0.0259 \text{ V}$   
 - Electric field is denoted by  $\mathcal{E}$  in the text  
 -  $\epsilon_{Si} = 3\epsilon_{ox} = 10^{-12} \text{ F/cm}$

**Problem 1** Consider a MOS capacitor fabricated on a p-type silicon substrate doped to  $5 \times 10^{16} \text{ cm}^{-3}$ . The gate material is  $n^+$  polysilicon. Assume that the gate Fermi level is at the band edge. The device has the following parameters:

Oxide charges  $Q_i = 10^{-8} \text{ C/cm}^2$  Oxide thickness  $x_{ox} = 500 \text{ \AA}$

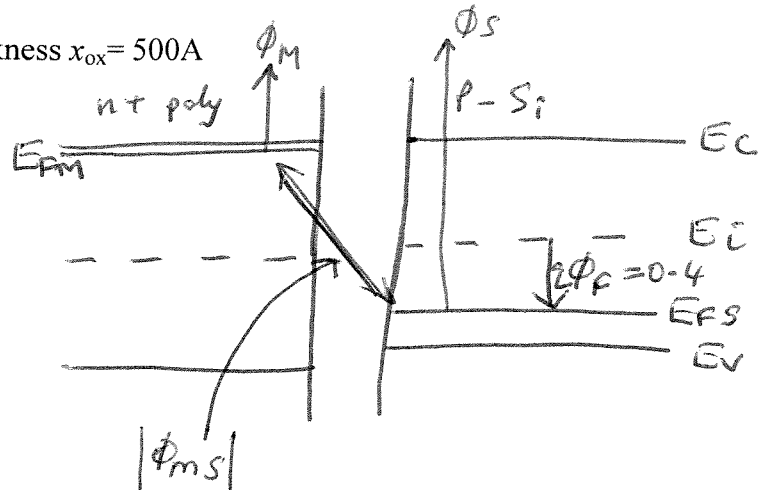
a. Determine the  $\Phi_{MS}$  value for this device.

$$\phi_F = kT \ln \frac{5 \times 10^{16}}{10^{10}} = 0.4 \text{ eV}$$

$$\phi_F = 0.4 \text{ V}$$

$$\Phi_{MS} = \Phi_m - \Phi_s = -(0.55 + 0.4)$$

$$= -0.95 \text{ eV}$$



b. Calculate the gate oxide capacitance  $C_{ox}$  per unit area in  $\text{F/cm}^2$ .

$$C_{ox} = \frac{\epsilon_{ox}}{x_{ox}} = \frac{1/3 \times 10^{-12} \text{ F/cm}}{500 \times 10^{-8}} = 66.6 \times 10^{-9} \text{ F/cm}^2$$

c. Calculate the total gate capacitance  $C_G$  at **high frequency** in  $\text{F/cm}^2$  when the device is under inversion.

$$W_T = \sqrt{\frac{2\epsilon_{Si}}{qN_A} \cdot 2\phi_F} = \sqrt{\frac{2 \times 10^{-12}}{2 \times 5 \times 10^{16}} \times 2 \times 0.4} = 1.41 \times 10^{-5} \text{ cm}$$

$$C_{S_{min}} = \frac{\epsilon_{Si}}{W_T} = 70.7 \times 10^{-9} \text{ F/cm}^2$$

$$C_G (\text{at inversion}) = \frac{C_{ox} C_S}{C_{ox} + C_S} = 34.3 \times 10^{-9} \text{ F/cm}^2$$

d. What is meant by the term “flat band voltage”? Describe it in a sentence or two. Calculate its value.

$$V_{FB} = \frac{\Phi_{MS}}{q} + \left( -\frac{Q_i}{C_{ox}} \right) = -0.95 \text{ V} + \left( -\frac{10^{-8} \text{ C/cm}^2}{66.6 \times 10^{-9} \text{ F/cm}^2} \right) = \underline{\underline{-1.1 \text{ V}}}$$

Voltage to be applied to the gate to get flat band condition

e. Calculate the threshold voltage  $V_T$ .

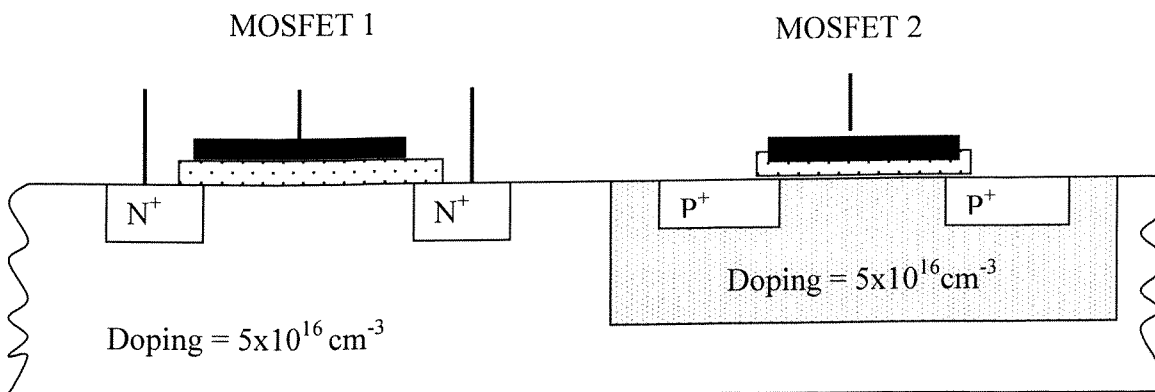
$$V_T' = 2\phi_F + \frac{q\epsilon_{Si}\chi_{op}}{60\pi} \sqrt{\frac{2qNA}{\epsilon_{Si}} 2\phi_F}$$

$$= 2 \times 0.4 + 3 \times 500 \times 10^{-8} \sqrt{\frac{2 \times 1.6 \times 10^{-19} \times 5 \times 10^{16} \times 2 \times 0.4}{10^{-12}}}$$

$$= 2.5V$$

$$V_T = V_{FB} + V_T' = -1.1 + 2.5 = \underline{\underline{+1.4V}}$$

**Problem 2** Consider a CMOS fabricated on a silicon substrate doped to  $5 \times 10^{16} \text{cm}^{-3}$ . The gate material is Al which has a work function  $\Phi_M$  value of 4.2eV. Assume that the  $\chi$  value for Si is 4.0eV. The oxide thickness is 500Å. The field oxide is not shown. Neglect the presence of oxide charges.



a. First identify each device. MOSFET 1 is (NMOS, PMOS: choose one), and MOSFET 2 is (NMOS, PMOS: choose one).

The substrate is (n-type, p-type, intrinsic, cannot tell), and the well is (n-type, p-type, intrinsic, cannot tell). Circle the correct answer.

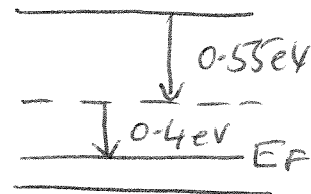
b. Determine the  $\Phi_{MS}$  value and the flat band voltage of MOSFET 1. (Hint:  $\chi$  value is the energy difference between the conduction band and the vacuum level).

$$\phi_m = 4.2 \text{ eV}$$

$$\phi_s = 4 + 0.55 + 0.4 = 4.95 \text{ eV}$$

$$\phi_{ms} = 4.2 - 4.95 = -0.75 \text{ eV}$$

$$V_{FB} = -0.75 \text{ V}$$



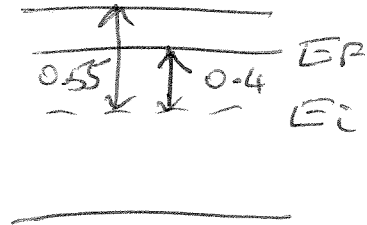
c. Determine the  $\Phi_{MS}$  value and the flat band voltage of MOSFET 2.

$$\phi_m = 4.2 \text{ eV}$$

$$\phi_s = 4 + (0.55 - 0.4) \\ = 4.15 \text{ eV}$$

$$\phi_{ms} = \phi_m - \phi_s = 4.2 - 4.15 \\ = 0.05 \text{ eV}$$

$$\underline{\underline{V_{FB} = 0.05 \text{ V}}}$$



d. Determine the threshold voltage of MOSFET 1 and MOSFET 2.

From Problem 1,  $|V_T'| = 2.5 \text{ V}$ .

MOSFET 1       $V_T = V_T' + V_{FB} = 2.5 - 0.75 \\ = 1.75 \text{ V}$

MOSFET 2       $V_T = V_T' + V_{FB} \\ = -2.5 + 0.05 \text{ V} \\ = -2.45 \text{ V}$

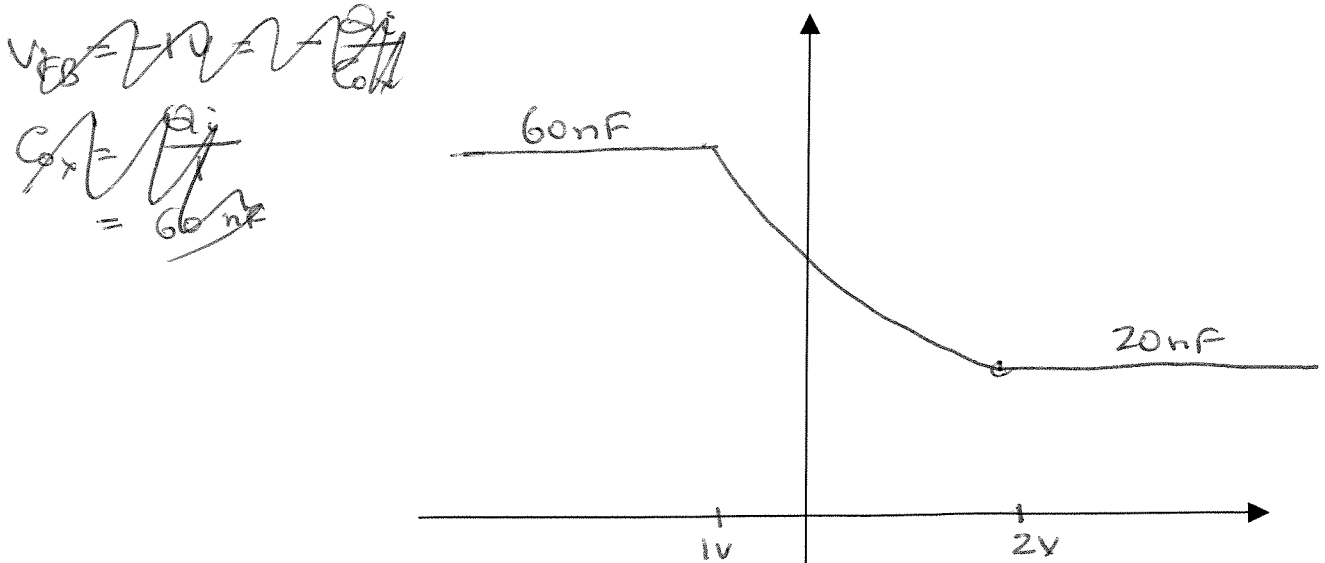
Note : MOSFET 1 is nmos,  $V_T' = (+)$   
MOSFET 2 is pmos,  $V_T' = (-)$

Since both has the same substrate doping magnitude,  $|V_T'|$  is the same for both

### Problem 3

Consider a n-channel MOSFET. The threshold voltage is 2V and the flat band voltage is -1V. The  $\Phi_{MS}$  value for this device is zero. The oxide capacitance is 60nF/cm<sup>2</sup> and the gate capacitance at high frequency is 20nF/cm<sup>2</sup>. Neglect the presence of S/D for the C-V curves.

- a. Plot the C-V characteristics at high frequency and low frequency. Mark all the relevant numerical data on the graph.



- b. Determine the oxide charges if any in C/cm<sup>2</sup>.

$$\begin{aligned} \text{Oxide Charges} &= -C_{ox} V_{FB} = -60 \times 10^{-9} \frac{F}{cm^2} \times (-1V) \\ &= +60 \times 10^{-9} \frac{C}{cm^2} \\ \text{or } &3.7 \times 10^{11} \frac{\text{holes}}{cm^2} \end{aligned}$$

- c. What is the thickness of the oxide?

$$60 \times 10^{-9} \frac{F}{cm^2} = \frac{\epsilon_{ox}}{\alpha_{ox}} \Rightarrow \alpha_{ox} = 555 \text{ \AA} = 55.5 \text{ nm}$$

- d. What is the value of the semiconductor capacitance,  $C_{Smin}$  at inversion? Also, calculate the maximum depletion layer width  $W_T$ .

$$C_{Smin} = 30 \times 10^{-9} \frac{F}{cm^2}$$

$$\frac{1}{C_G} = \frac{1}{C_{Smin}} + \frac{1}{C_{ox}}$$

$\uparrow$  20                       $\uparrow$  60

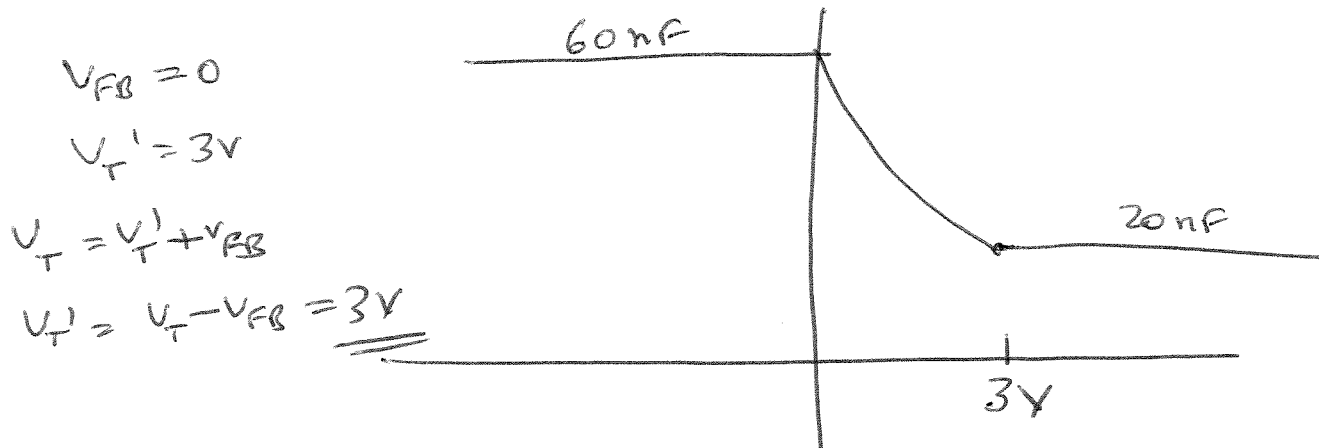
$$C_G = \frac{C_{ox} C_S}{C_{ox} + C_S}$$

$$C_G C_{ox} + C_G C_S = C_{ox} C_S$$

$$C_S (C_{ox} - C_G) = C_G C_{ox}$$

$$W_T = \sqrt{\frac{2\epsilon_{Si}}{qN_A} \cdot 2\phi_F} =$$

e. Replot the C-V curve of part (a) if the oxide charges were zero.

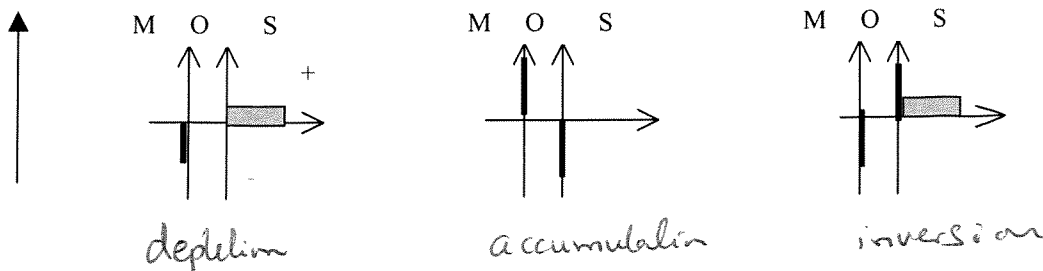


### Problem 4

This problem has several independent parts. Most of the questions do not require extensive calculations

a. The following three figures show the charge density  $\rho$  in ideal MOS structures. Label each figure correctly with “flat band”, or “threshold” or “accumulation” or “depletion” or “inversion”. The substrate is (**n-type, p-type, cannot tell**). Choose one.

$\rho$  positive

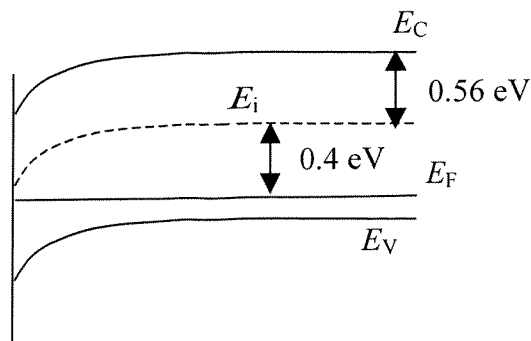


b. The energy band diagram for an ideal MOS-capacitor (MOS-C) is shown below. The surface potential is  $0.25V$ . This structure is in (**depletion, accumulation, inversion: choose one**). Calculate the depletion layer width  $W$ .

$$W = \sqrt{\frac{2\epsilon_{Si} \phi_s}{q N_A}}$$

$$= 79 \text{ nm}$$

$$0.4 = kT \ln \frac{N_A}{n_i} \Rightarrow N_A = 5 \times 10^{16} \text{ cm}^{-3}$$



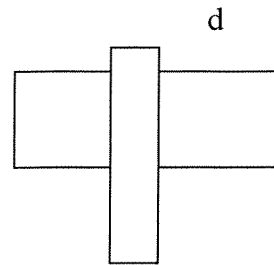
- c. A silicon substrate is implanted with boron ions at an energy of 100 keV. The ion dose is  $10^{13} \text{ cm}^{-2}$ . Assume a range  $R_p = 0.15 \mu\text{m}$  and a straggle  $\Delta R_p = 0.05 \mu\text{m}$  for the implantation process. The substrate is doped with  $5 \times 10^{16} \text{ cm}^{-3}$  of arsenic. What is the peak concentration of boron? At what depth this peak concentration is formed?

$$B_{\text{peak}} = \frac{\text{dose}}{\sqrt{2\pi} \cdot \Delta R_p} = \frac{10^{13}}{\sqrt{2\pi} \times 0.05 \mu\text{m}} = 8 \times 10^{17} \text{ cm}^{-3}$$

at  $x = 0.15 \mu\text{m}$  below the surface

- e. Masks should be designed such that the poly-gate area overhangs the active area by a distance "d" as shown. Explain clearly why. Be very clear.

If the overhang were zero, any alignment error will result in S and D being shorted



- f. Two Schottky diodes are made using n-type silicon. Diode A is made using a metal whose work function is 4.5eV where as diode B is made with metal whose work function is 5.0eV. Which one will have lower reverse leakage current? Explain clearly.

$\phi_B$  of A  $<$   $\phi_B$  of B.  
 Since reverse leakage current  $\downarrow$  as  $\phi_B \uparrow$ ,  
 Diode B will have lower  $I_0$ .

- g. A basic CMOS layout is shown below. Draw the circuit it represents.

