ECSE 2210 Microelectronics Technology
Review Questions for Quiz 3

(We will work this out in class on Wednesday, April 23rd)

Problem 1 Consider a MOS capacitor fabricated on a p-type silicon substrate doped to 5×10^{16} cm^{-3}. The gate material is n^+ polysilicon. Assume that the gate Fermi level is at the band edge. The device has the following parameters:

Oxide charges $Q_i = 10^{-8}$ C/cm^2 Oxide thickness x_{ox}= 500 Å

a. Determine the Φ_{MS} value for this device.

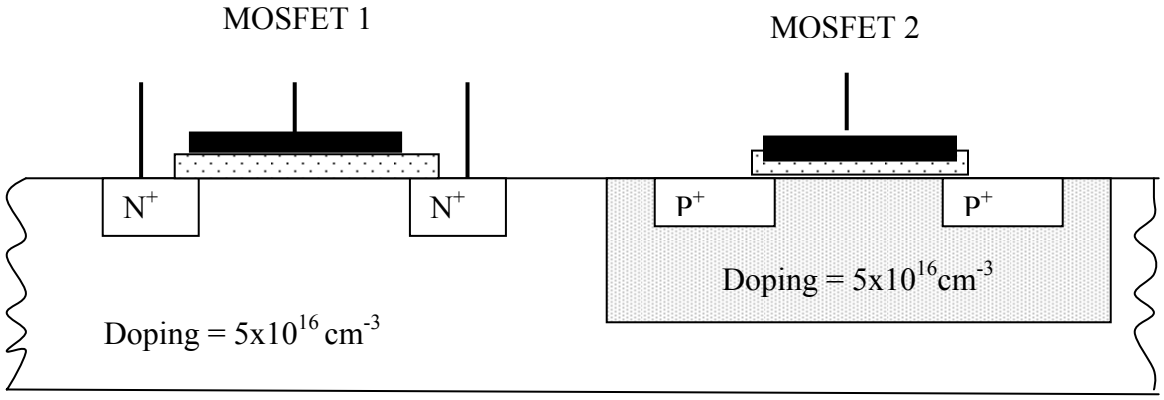
b. Calculate the gate oxide capacitance C_{ox} per unit area in F/cm^2.

c. Calculate the total gate capacitance C_G at **high frequency** in F/cm^2 when the device is under inversion.

d. What is meant by the term "flat band voltage"? Describe it in a sentence or two. Calculate its value.

e. Calculate the threshold voltage V_T.

Problem 2 Consider a CMOS fabricated on a silicon substrate doped to 5×10^{16} cm^{-3}. The gate material is Al which has a work function Φ_M value of 4.2 eV. Assume that the χ value for Si is 4.0 eV. The oxide thickness is 500 Å = 50 nm. The field oxide is not shown. Neglect the presence of oxide charges.



a. First identify each device. MOSFET 1 is **(NMOS, PMOS: choose one),** and MOSFET 2 is **(NMOS, PMOS: choose one).**

The substrate is (**n-type, p-type, intrinsic, cannot tell**), and the well is (**n-type, p-type, intrinsic, cannot tell**). Circle the correct answer.

b. Determine the Φ_{MS} value and the flat band voltage of MOSFET 1. (Hint: χ value is the energy difference between the conduction band and the vacuum level).

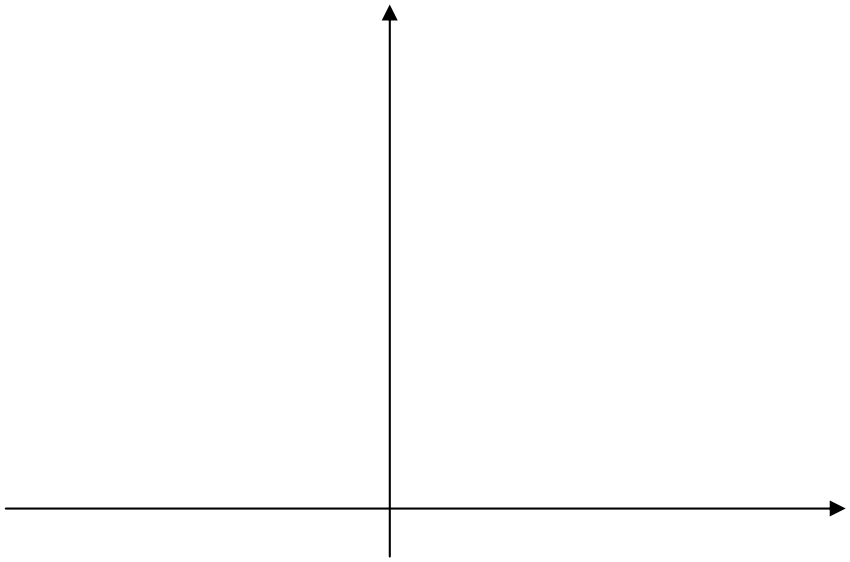
c. Determine the Φ_{MS} value and the flat band voltage of MOSFET 2.

d. Determine the threshold voltage of MOSFET 1 and MOSFET 2.

Problem 3

Consider a n-channel MOSFET. The threshold voltage is 2 V and the flat band voltage is –1 V. The Φ_{MS} value for this device is zero. The oxide capacitance is 60 nF/cm^2 and the gate capacitance at high frequency is 20 nF/cm^2. Neglect the presence of S/D for the C-V curves.

a. Plot the C-V characteristics at high frequency and low frequency. Mark all the relevant numerical data on the graph.



b. Determine the oxide charges if any in C/cm^2.

c. What is the thickness of the oxide?

d. What is the value of the semiconductor capacitance, C_{Smin} at inversion? Also, calculate the maximum depletion layer width W_T.

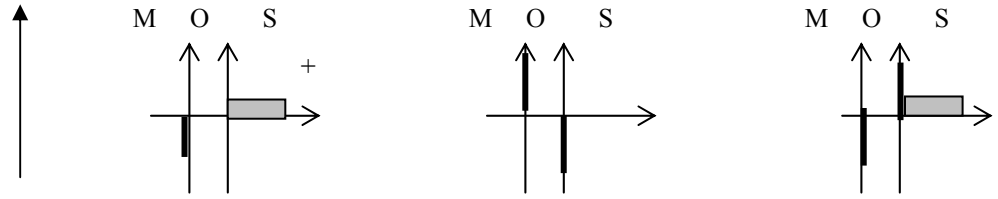
e. Re-plot the C-V curve of part (a) if the oxide charges were zero.

Problem 4

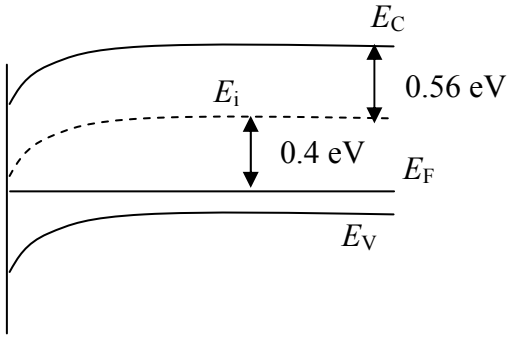
This problem has several independent parts. Most of the questions do not require extensive calculations

a. The following three figures show the charge density ρ in ideal MOS structures.
Label each figure correctly with "flat band", or "threshold" or "accumulation" or "depletion" or "inversion". The substrate is (**n-type, p-type, cannot tell**). Choose one.

ρ positive

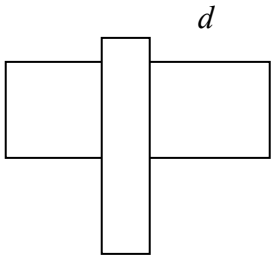


b. The energy band diagram for an ideal MOS-capacitor (MOS-C) is shown below. *The surface potential is 0.25 V*. This structure is in **(depletion, accumulation, inversion: choose one)**. Calculate the depletion layer width *W*.



c. A silicon substrate is implanted with boron ions at an energy of 100 keV. The ion dose is 10^{13} cm^{-2}. Assume a range $R_p = 0.15$ μm and a straggle $\Delta R_p = 0.05$ μm for the implantation process. The substrate is doped with 5×10^{16} cm^{-3} of arsenic.
What is the peak concentration of boron? At what depth this peak concentration is formed?

e. Masks should be designed such that the ploy-gate area overhangs the active area by a distance "*d*" as shown. Explain clearly why. Be very clear.



f. Two Schottky diodes are made using n-type silicon. Diode A is made using a metal whose work function is 4.5 eV where as diode B is made with metal whose work function is 5.0 eV. Which one will have lower reverse leakage current? Explain clearly.

g. A basic CMOS layout is shown below. Draw the circuit it represents.