

**ECSE-2210 Microelectronics Technology**  
**Class Activity 16 – Solution**

1. What is the physical origin of the junction capacitance (or depletion layer capacitance)?

The in and out movement of the majority carriers about the steady state depletion width in response to the applied ac signal gives rise to the junction capacitance. Effectively, it looks like the plus and the minus charges are alternatively being added and subtracted from two planes inside the diode with a width  $W$ , similar to what happens in a parallel plate capacitor.

2. What is the physical origin of the diffusion capacitance?

Changes in the stored minority carriers in the quasi-neutral region in response to the applied ac signal gives rise to the diffusion capacitance. In response to an ac signal, the minority carrier distributions oscillate about their dc values resulting in an additional capacitance.

3. Why is the diffusion capacitance negligible under reverse bias?

The concentration of minority carriers stored in reverse-bias is very small. So, any change will be even smaller.

4. What is the value of the reverse-bias conductance for an ideal diode?

The reverse bias conductance is zero for an ideal diode.

5. Write the equation for the reverse bias conductance for a real  $p^+$ -n diode if  $I_{R-G}$  is dominating in reverse bias.

$$I_{R-G} = -q A n_i W / 2 \tau_0 \text{ with } W = [2\epsilon / q N_D \times (V_{bi} - V_A)]^{1/2}$$

$$\text{So, } dI / dV = q A n_i W / 2 \tau_0 \times [1 / (V_{bi} - V_A)]$$

6. Given a planar  $p^+$ -n Si step junction diode with an n-side doping of  $N_D = 10^{15} \text{ cm}^{-3}$  at  $T = 300 \text{ K}$ , determine the junction capacitance at  $-1 \text{ V}$  reverse bias. Assume that the Fermi-level is at the valence band edge in the  $p^+$ -region. Junction area  $A = 1 \text{ cm}^2$ . At zero bias, will the junction capacitance be higher or lower than the one calculated above? (Hint: Calculate  $V_{bi}$ , then  $W$  and then the junction capacitance).

First find  $V_{bi}$ .

$$V_{bi} = 0.55 \text{ V} + 0.0259 \text{ V} \times \ln (10^{15}/10^{10}) \\ = 0.848 \text{ V}$$

$$W = [2\epsilon_{Si}/qN_D \times (V_{bi} - V_A)]^{1/2}$$

$$W = [(2\epsilon_{Si}/q) \times (1/N_D)(0.848 \text{ V} + 1 \text{ V})]^{1/2} \\ = 1.52 \times 10^{-4} \text{ cm.}$$

$$\text{So, } C_j = \epsilon_{Si} A / W \\ = 10^{-12} \times 1 / 1.52 \times 10^{-4} \\ = 6.57 \text{ nF.}$$

At zero bias, the junction capacitance will be larger than the above value since the depletion layer width will be smaller.

7. A particular ideal p<sup>+</sup>n junction has a reverse saturation current of  $1 \times 10^{-14}$  A. The hole lifetime in the n-side is  $1 \times 10^{-6}$  s. What will be the diode diffusion admittance at a forward bias of 0.6 V? (Write the answer in terms of  $\omega$ ). Draw the small signal equivalent circuit for the diode.

$$I = I_0 \exp(qV/kT)$$

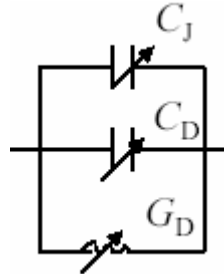
$$I(V = 0.6 \text{ V}) = 1.15 \times 10^{-4} \text{ A}$$

Diffusion conductance:  $G_D = qI / (kT)$   
 $= 1.15 \times 10^{-4} / 0.0259$   
 $= 4.44 \times 10^{-3} \text{ S}$

Diffusion capacitance:  $C_D = qI\tau_p / (kT)$   
 $= 1.15 \times 10^{-4} \times 10^{-6} / 0.0259$   
 $= 4.44 \text{ nF}$

$$\rightarrow Y_D = G_D + j\omega C_D$$

$$= 4.44 \times 10^{-3} \text{ S} + j\omega \times 4.44 \times 10^{-9} \text{ F}$$



The small signal equivalent circuit under forward bias is as shown in the figure above.

8. Consider three p<sup>+</sup>-n junctions as shown below. Which one will have the highest junction capacitance? Which one will have the lowest junction capacitance? Try to understand the physical reasoning.

p <sup>+</sup>	$N_D = 10^{15} \text{ cm}^{-3}$
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p <sup>+</sup>	$N_D = 10^{17} \text{ cm}^{-3}$
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p <sup>+</sup>	intrinsic	$N_D = 10^{15} \text{ cm}^{-3}$
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Of the three diodes I will have the least depletion region width  $W$  and III will have the largest width. As the junction capacitance and the depletion width are inversely proportional to each other, diode III will have the least capacitance and diode I will have the largest capacitance.