ECSE-2210 Microelectronics Technology
Class Activity 28 – Solution

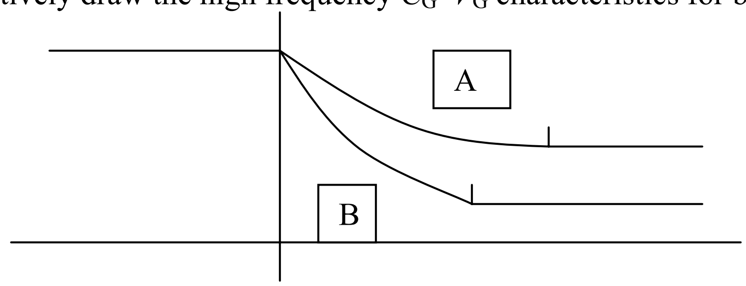
1. Two MOS capacitors are made from different silicon substrates, A and B. All parameters are identical except the substrate doping. Substrate A is doped with 10^{16} cm^{-3} acceptors and substrate B is doped with 10^{14} cm^{-3} acceptors.

   a. Which one will have the higher V_T?

   $$V_T = 2\,\phi_F + \frac{K_s\,x_{ox}}{K_{ox}}\sqrt{\frac{4q\,N_A}{K_s\,\varepsilon_{ox}}\,\phi_F}$$

   Substrate A will have higher V_T. The higher the doping, the higher is ϕ_F. So, we have to apply more gate voltage to get the bands in the surface region to bend down below E_i. Hence the threshold voltage is larger for the MOS-C with higher substrate doping.

   b. Qualitatively draw the high frequency C_G-V_G characteristics for both.



2. An ideal MOS-C is made from p-type Si with a dopant concentration of 2×10^{15} cm^{-3}. The oxide thickness is 0.1 μm, and the junction area $A = 1$ cm^2.

   a. Determine V_T for this device.

   $$V_T = 2\phi_F + \frac{K_s\,x_{ox}}{K_{ox}}\sqrt{\frac{4q\,N_A}{K_s\,\varepsilon_{ox}}\,\phi_F}$$

   $$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right)$$

   $$2\times10^{15} = 10^{10} \exp\left(\frac{E_i - E_F}{0.0259}\right)$$

   $$\phi_F = E_i - E_F = 0.0259 \ln\frac{2\times10^{15}}{10^{10}} = 0.316 \text{ V}$$

   $$V_T = 0.632 + 3\times0.1\times10^{-4}\sqrt{\frac{4\times1.6\times10^{-19}\times2\times10^{15}}{10^{-12}}0.316} = 1.235 \text{ V}$$

   b. Determine the oxide capacitance.

   $$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} = \frac{3.9\times8.85\times10^{-14}}{0.1\times10^{-4}} = 3.45\times10^{-8} \text{ F/cm}^2$$

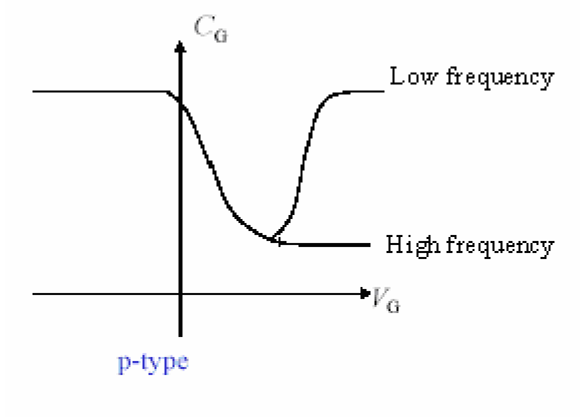
   c. Determine the semiconductor capacitance when $V_G = V_T$.

$$W_T = \sqrt{\frac{2K_s \varepsilon_{ox}}{q N_A} 2\phi_F} = 0.628 \ \mu\text{m}$$

$$C_{ox} = \frac{\varepsilon_S}{W_T} = \frac{10^{-12}}{0.628 \times 10^{-4}} = 1.59 \times 10^{-8} \ \frac{\text{F}}{\text{cm}^2}$$

d. Determine the total high frequency steady-state gate capacitance when $V_G = V_T$ and $V_G > V_T$. Plot the C_G-V_G characteristics.

$C_G (V_G = V_T) = C_{ox} C_s / (C_{ox} + C_S) = 1.07 \times 10^{-8}$ F/cm^2



e. Suppose the gate voltage is zero at $t = 0$, and *rapidly* changes from $V_G = 0$ to $V_G = 5$V. Determine the total gate capacitance at $t = 0^+$. (Hint: First find $\phi_s^{1/2}$ using equation 16.28. Then find W using equation 16.15.)
If we substitute x for $\phi_s^{1/2}$ equation 16.28 becomes: $5 = x^2 + 0.758\, x$
➔ $x = \phi_s^{1/2} = (1.9 \text{ V})^{1/2}$ and $\phi_s = 3.6$ V
➔ $W = 1.5$ µm
➔ $C_s = 6.66 \times 10^{-9}$ F/cm^2
➔ $C_G = C_{ox} C_s / (C_{ox} + C_s) = 5.5 \times 10^{-9}$ F/cm^2

f. For $V_G > V_T$, an inversion channel forms. The inversion channel will consist of (electrons, **holes**: choose one). If the MOSFET is made using the above substrate, the device is called (n-channel, **p-channel**: choose one) MOSFET.

g. Suppose a gate-voltage of 5 V is applied to the MOSFET gate. Assume V_D is close to zero. Determine the inversion layer charge Q_{inv} in C. (Hint: Q_{inv} is almost zero when $V_G = V_T$).
$V_T = 1.24$ V. When $V_G = V_T$, the inversion layer just starts to form.
For $V_G > V_T$, there will be more inversion layer charges than dopant atoms in the interface region. Hence, $C_{ox} (V_G - V_T) = Q_{inv}$.
$Q_{inv} = (5 - 1.235) \times 3.45 \times 10^{-8} = 1.29 \times 10^{-7}$ C/cm^2
Note: Q_{inv} corresponds to 7.8×10^{11} electrons/cm^2.

h. Suppose a drain voltage of 4 V is applied while the gate voltage is 5 V. What will be the inversion layer charge, Q_{inv} at the source end? What will be inversion layer charge, Q_{inv} at the drain end?
At the source end, Q_{inv} will be the same as above.
At the drain end, the difference between the gate voltage and the drain side is less than the threshold voltage, i.e., $(V_G - V_D) = 5\ V - 4\ V = 1\ V < V_T$. Therefore, the inversion layer charge is zero. ("Pinch-off" condition)