



- d. Determine the total high frequency steady-state gate capacitance when  $V_G = V_T$  and  $V_G > V_T$ . Plot the  $C_G$ - $V_G$  characteristics.
- e. Suppose the gate voltage is zero at  $t = 0$ , and *rapidly* changes from  $V_G = 0$  to  $V_G = 5\text{V}$ . Determine the total gate capacitance at  $t = 0^+$ . (Hint: First find  $\phi_s^{1/2}$  using equation 16.28. Then find  $W$  using equation 16.15. )
- f. For  $V_G > V_T$ , an inversion channel forms. The inversion channel will consist of (electrons, holes: choose one). If the MOSFET is made using the above substrate, the device is called (n-channel, p-channel: choose one) MOSFET.
- g. Suppose a gate-voltage of 5 V is applied to the MOSFET gate. Assume  $V_D$  is close to zero. Determine the inversion layer charge  $Q_{\text{inv}}$  in C. (Hint:  $Q_{\text{inv}}$  is almost zero when  $V_G = V_T$ ).
- h. Suppose a drain voltage of 4 V is applied while the gate voltage is 5 V. What will be the inversion layer charge,  $Q_{\text{inv}}$  at the source end? What will be inversion layer charge,  $Q_{\text{inv}}$  at the drain end?