ECSE-2210 Microelectronics Technology
Class Activity 31 – Solution

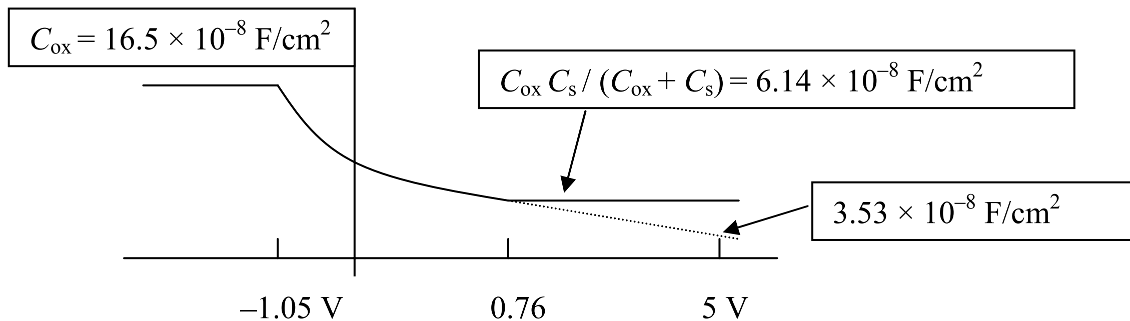
Consider a MOS capacitor fabricated on a p-Si doped to 10^{17} cm^{-3} acceptors. Assume that the oxide thickness is x_{ox} = 20 nm = 200 Å, Φ_{ms} = – 1.05 eV, Ignore Q_i. Plot the C_G-V_G characteristics if the gate voltage is changed very slowly from – 5 V to + 5 V. calculate all numerical values.

C_{ox} = (0.33 × 10^{-12} F/cm) / (200 × 10^{-8} cm) = 16.5 × 10^{-8} F/cm^2
V_{FB} = – 1.05 V since Q_i is negligible.
ϕ_F = 0.0259 V ln (10^{17} / 10^{10}) = 0.417 V

Find W_t when ϕ_s is $2\phi_F$. This is the threshold condition. If you find the semiconductor capacitance at this condition, then we know the total capacitance when $V_G = V_T$.
Then draw a smooth curve (see below)
$W_T = [(2\ \varepsilon_s / q\ N_A)\ \phi_s]^{1/2}$ = 0.102 µm
$C_s = \varepsilon_s / W_T$ = 9.8 × 10^{-8} F/cm^2
V_T' (ideal case) = 1.81 V
V_T = V_{FB} + 1.81 V = 0.76 V

Note: For further understanding refer to solutions class activity 30

1. For the above case, qualitatively plot the C_G-V_G characteristics if the gate voltage is rapidly changed from – 5 V to + 5 V.



2. (If time permits) Calculate all numerical values for problem 2. ***Hint***: Use equation 16.28 which relates V_G to $\phi_s^{1/2}$ and solve equation for $\phi_s^{1/2}$. From $\phi_s^{1/2}$ find ϕ_s. Then calculate W. For V_G in equation 16.28, use 6.05 V taking into account the flat-band voltage V_{FB} = – 1.05 V.

   Use equation 16.28 relating V_G to $\phi_s^{1/2}$ and solve for $\phi_s^{1/2}$. From $\phi_s^{1/2}$, find ϕ_s, then find W. From W find C_s, then find $C_G = C_{ox}\ C_s / (C_{ox} + C_s)$.
   6.05 V = ϕ_s + 1.073 V$^{1/2}$ × $\phi_s^{1/2}$ (6.05 V because V_{FB} = – 1.05 V, and we find ϕ_s for gate voltage of 5 V).

So, $\phi_s = 3.92$ V

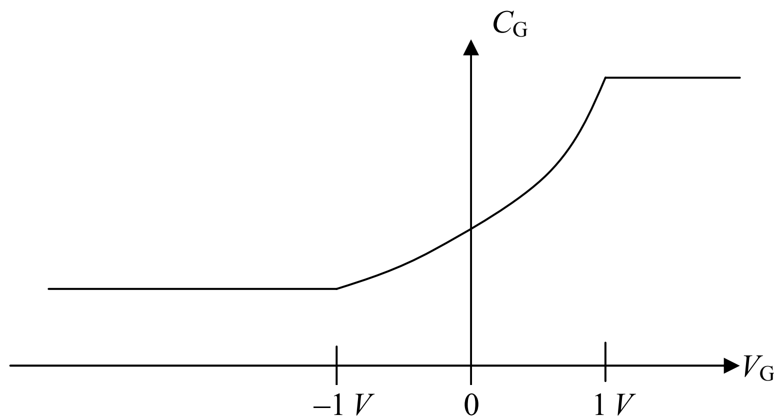
$$W = \sqrt{\frac{2 K_s \varepsilon_0}{q N_A} \phi_s} = 0.221\ \mu\text{m}$$

$C_s = 4.52 \times 10^{-8}$ F/cm^2

$C_{ox} C_s / (C_{ox} + C_s) = 3.53 \times 10^{-8}$ F/cm^2

3. Explain why a DRAM cell needs refreshing every few milliseconds.
   The deep depletion condition remains only for a few milliseconds. If deep depletion condition is called “1”, then this “1” will become “0” after a few milliseconds. So, we need refreshing to maintain “1”. We need to refresh the DRAM to essentially remove the thermally generated carriers that make the state go from ON to OFF.

4. The following C-V curve is taken from a MOS capacitor fabricated on Si. The oxide thickness is $x_{ox} = 0.1$ μm and the gate metal is chosen such that ϕ_{ms} is zero.



   a. Calculate the net interface charges present in the oxide in C/cm^2.
      From the figure $V_{FB} = 1$V

$$V_{FB} = \frac{1}{q}\Phi_{ms} + \left(-\frac{Q_i}{C_{ox}}\right)$$

      It is given that Φ_{MS} is zero. Therefore the $V_{FB} = -Q_i / C_{ox}$
      $Q_i = -2.08 \times 10^{11} \times q$. ($q = 1.6 \times 10^{-19}$ C)

   b. What will be the threshold voltage, if there were no interface charges?
      If there were no interface charges, accumulation would extend until V_G is 0 V and MOSFET would be in depletion untill – 2 V. The above curve would have to shift left by 1 V.
      $V_T = -2$ V

c. Is the substrate p-type or n-type?
   The substrate is n-type because we have a p-channel MOSFET with threshold voltage that is negative.

5 Consider a MOS-C on p-Si. When the gate voltage is swept from 0 V to $V_G > V_T$, an inversion layer forms, but it may take a few milliseconds. Mention a few methods to speed up this process.

Here are some ways you can increase the chances of forming an inversion layer quickly:

a. Have n^+ source and drain overlapping the gate (like MOSFET). This will be the source of electrons.
b. Shine light on the samples. Similar to a CCD camera.
c. Increase the temperature. This will increase the generation rate.
d. Decrease the carrier lifetime by introducing mid-gap levels.

6 The C_G-V_G characteristic of a NMOS transistor (at both high and low frequency) is similar to the C-V characteristics of a MOS-Capacitor at low frequency. Can you explain why?
The high frequency characteristic of the MOSFET is similar to the low frequency characteristics of MOS-C because the source and the drain supply the minority carriers require for the structure to follow the ac fluctuations of the gate when the device is inversion biased. Now you can turn on/off a MOSFET at high frequency.