ECSE-2210 Microelectronics Technology
Homework 10 – Solution

Reading Assignment: Chapter 17 and Chapter 18 (pg. 645 – 662)

1. A MOSFET made with n^+ poly-silicon gate has the following characteristics:

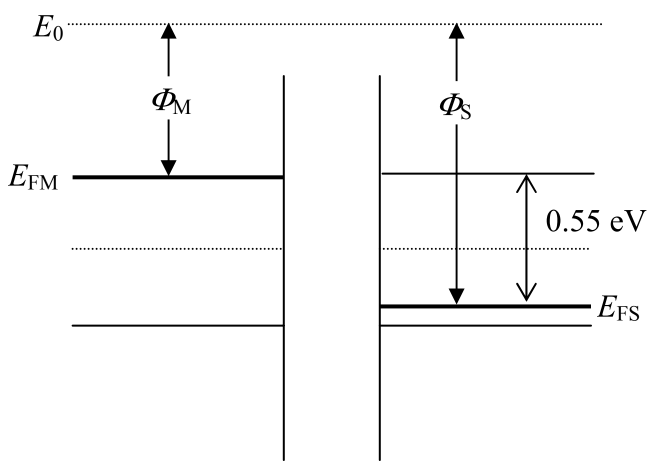
Oxide thickness $x_{ox} = 500$ Å
Doping in Si: $N_A = 10^{16}$ cm^{-3}
Interface oxide charges $Q_i = 6.4 \times 10^{11} \times 1.6 \times 10^{-19}$ C/cm^2
Area $A = 1$ cm^2

a. Calculate the flat-band voltage V_{FB} for this device (Hint: Since the gate is made of n^+-poly-silicon, assume that the gate Fermi-level is at the conduction band edge. Since $\Phi_{MS} = \Phi_M - \Phi_S$, the magnitude of Φ_{MS} in this case will be equal to $(1/q)$ [E_F(gate) – E_F(silicon)]).

$\phi_F = 0.357$ V

$\Phi_{MS} = 1/q \times [E_F(\text{gate}) - E_F(\text{silicon})] =$
$= -1/q \times E_G(\text{Si})/2 - 0.357 \text{ V} = -0.55 \text{ V} - 0.357 \text{ V} =$
$= -0.907$ V

(To visualize this first, draw the band diagram of the gate silicon and that of the substrate silicon. Align the conduction and valence bands of these two. Then find the difference between the Fermi-levels of these two.)



$C_{ox} = (1/3)\ 10^{-12}$ F/cm / $(500 \times 10^{-8}$ cm$) = 6.66 \times 10^{-8}$ F/cm^2

$V_{FB} = -0.907 + [-(6.4 \times 10^{11} \times 1.6 \times 10^{-19} \text{ C}) / (6.66 \times 10^{-8} \text{ F/cm}^2)] = -2.44$ V

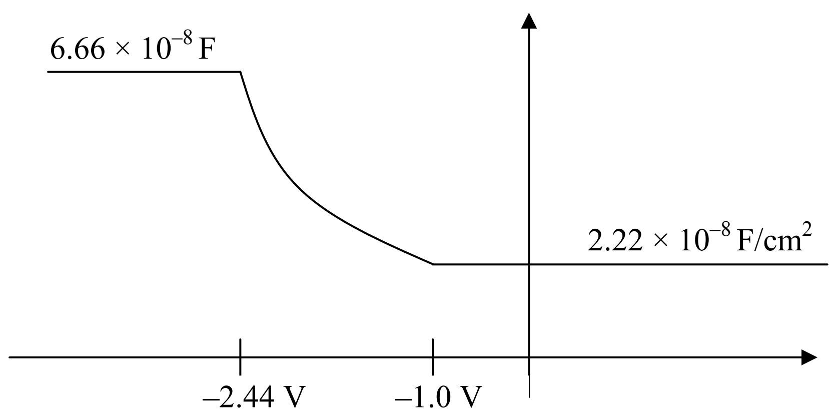
b. Calculate the threshold voltage, V_T', if the device were ideal. (This is the threshold voltage if the Φ_{ms} were zero and there were no interface charges).

V_T'(ideal) = 1.43 V using equation 17.1.

c. Calculate the actual threshold voltage, V_T, for this device taking into account Φ_{ms} and the interface charges.

$V_T(\text{real}) = V_{FB} + V_T(\text{ideal}) \approx -1.0$ V.

d. Plot the high frequency C_G-V_G characteristics for this device. Mark important points in the graph. (Ignore the presence of Source/Drain for this particular case).



$W_T = 0.3$ μm
$C_S = 3.33 \times 10^{-8}$ F
$C_{min} = C_{ox} C_s / (C_{ox} + C_S) = 2.22 \times 10^{-8}$ F/cm^2

e. Suppose we want to increase the threshold voltage by 1V (i.e., $\Delta V_T = +1$ V), calculate the number of (**boron or phosphorus: choose one**) ions that should be implanted into silicon.

Boron is an acceptor, thus the threshold voltage shifts to the positive side after boron implantation.

$\Delta Q = C \Delta V_T$, i.e., $\Delta Q = 6.66 \times 10^{-8}$ F × 1.0 V = 6.66×10^{-8} C
➔ Amount of boron ions to be implanted: 4.1×10^{11} ions/cm^2

2. Suppose one makes an identical MOSFET as above, except that the gate material is made up of p^+ silicon instead of n^+ silicon. What will be the actual threshold voltage of the device? ***Hint***: No need to do detailed calculation here. Check which terms changes, and make the appropriate corrections.

If we make the gate from p+ silicon, the Φ_M value in the above figure will be larger by 1.1 eV. So, Φ_{MS} will be larger by 1.1 eV.
Or: V_{FB} will be larger by 1.1 V and the threshold voltage will be larger by 1.1V as well.