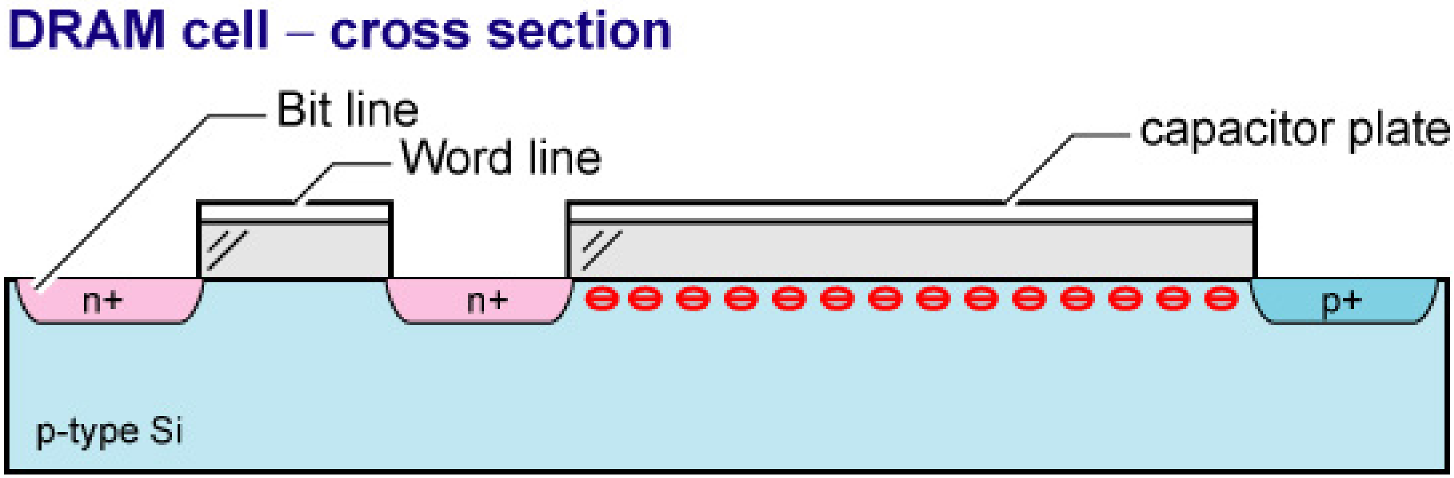
MOSFETS – Advanced topics

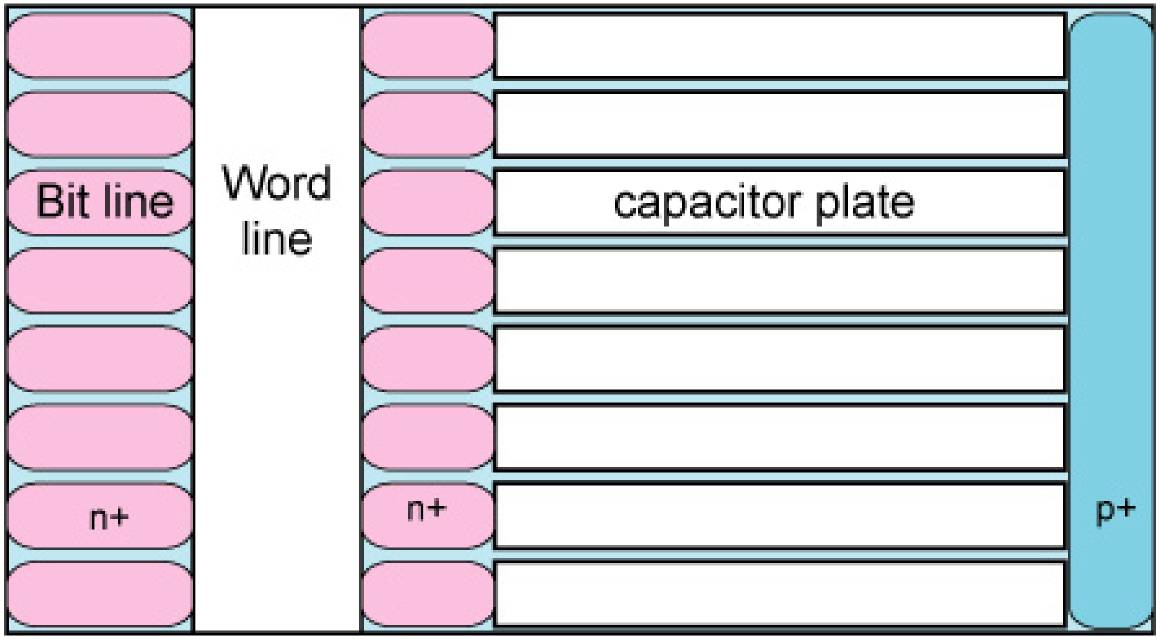
DRAM cell (1 transistor memory cell)



Information is stored in the capacitor. Transistor is used for read and write. Capacitor is leaky ➔ Information needs to be refreshed.

Top view of DRAM cell:

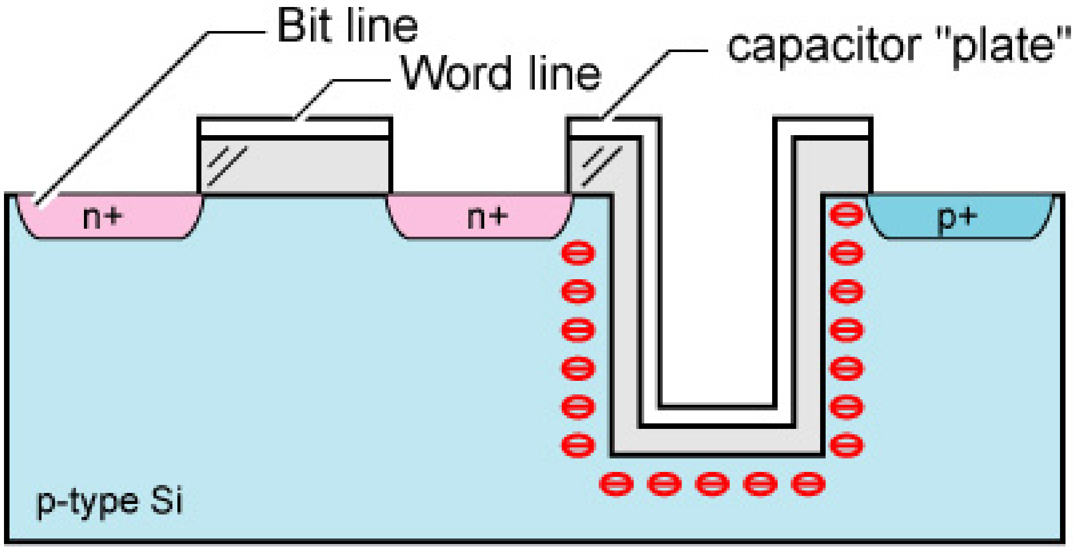
DRAM cell – top view



One word equals 8 bit or a multiple of 8 bits.

DRAM cell with trenched capacitor

**DRAM cell:
modern design**

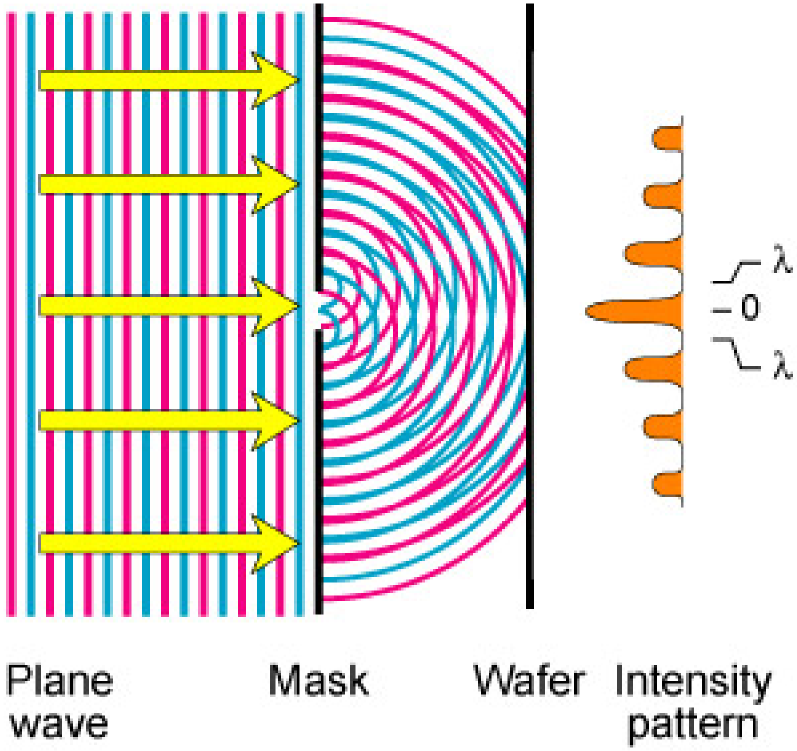


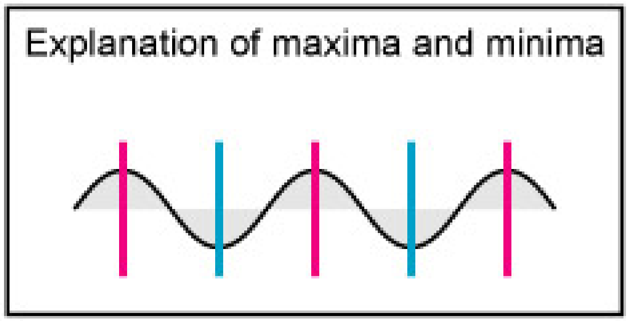
Question: What is the advantage of the modern design?

Lithography

Resolution of optical lithography is limited by diffraction effects.

Diffraction of light passing through a single slit.





Small features are obtained for small values of λ. Typical wavelengths used for lithography are:

Blue	400 nm
UV	310 nm (Xe lamp)
Deep UV	280 nm
Extremely deep UV	190 nm

EUV Prototype in Livermore, CA; EUV = Extreme Ultra Violet

- Photograph shows extreme UV lithography apparatus
- UV requires full encapsulation (Why?)
- Optical lithography still common way to make ICs

Beyond optical lithography

(1) Electron beam lithography

Example: Calculate λ for an electron beam with E = 0.5 keV.

$$E = E_{\text{kin}} = \frac{1}{2} m v^2 = \frac{p^2}{2m}$$

$$\text{DeBroglie relation} \quad p = \hbar k = h / \lambda$$

$$\Rightarrow \lambda = \frac{h}{p} = \frac{h}{\sqrt{2mE}} = 0.5 \text{ Angstroms}$$

(2) X-ray lithography

Consider the properties of X-ray photons:

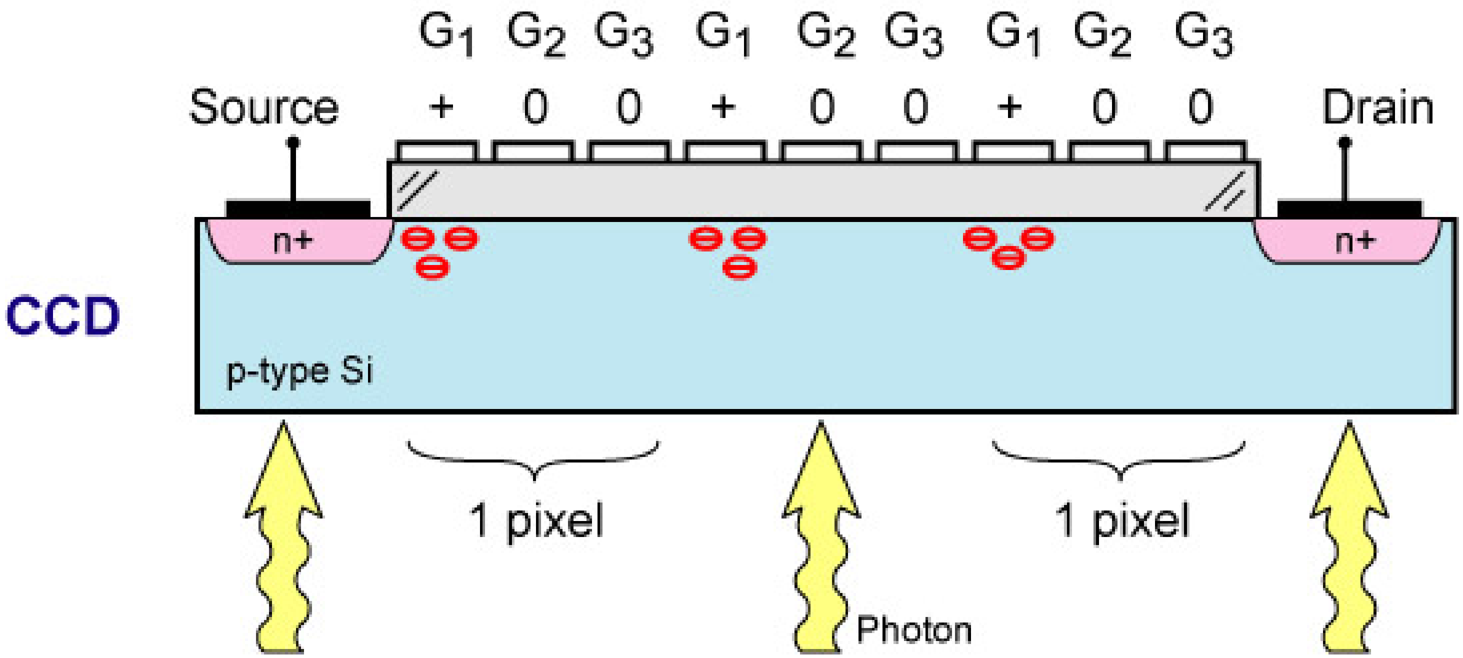
Planck relation: $E = h\,\nu = h\,c\,/\,\lambda$

Example: Calculate λ of x-ray photons with *E* = 20 keV.

Solution: λ = *hc* / *E* = 0.6 Ǻ

Due to the short wavelengths achievable, electron-beam lithography and x-ray lithography can produce patterns with small dimensions. State-of-the-art feature size in 1997 was 0.3 µm and in 2002 was 0.18 µm.

Charge-coupled devices = CCDs



A CCD is like a MOSFET with many gates. G1, G2, and G3 are sequentially positively biased. Charge injected at the source is sequentially transported from gate to gate.

Bias and timing

1st clock cycle

Gate	+	0	0	+	0	0
Channel	–	0	0	0	0	0

2nd clock cycle

Gate	0	+	0	0	+	0
Channel	0	–	0	0	0	0

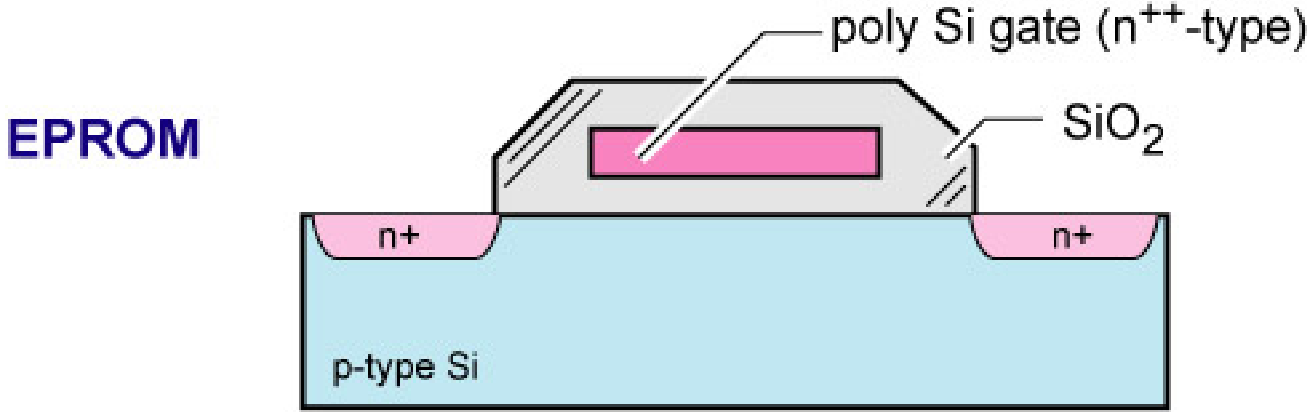
3rd clock cycle

Gate	0	0	+	0	0	+
Channel	0	0	–	0	0	0

In CCDs for optoelectronic applications (*e. g*. CCD detectors), the charge under the gate is generated optically. There is (first) an exposure time and (second) a read cycle. During the exposure time, photo-generated charge accumulates under one positively biased gate (*e. g*. G_1). In the read cycle, the information is read as a voltage at the drain. One pixel (picture dot) consists of three gates.

EPROM (Erasable programmable read-only memory)

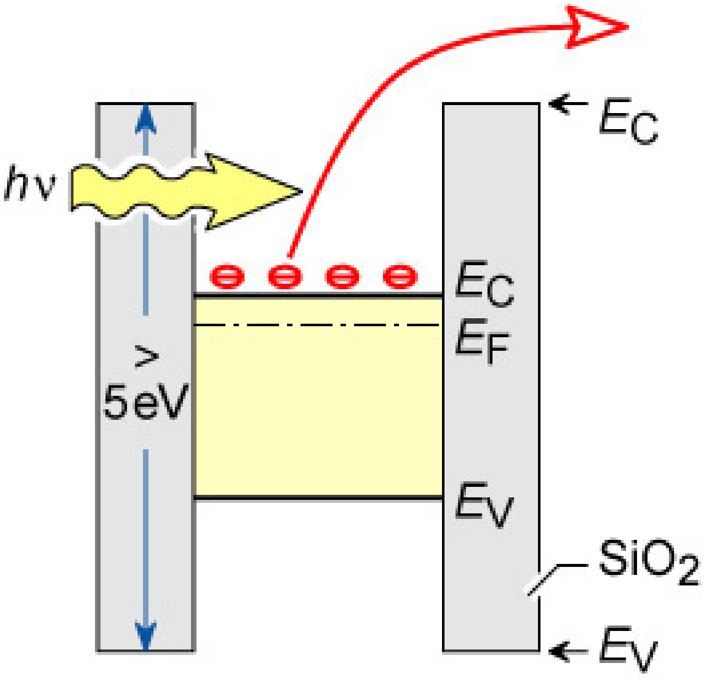
EPROMs consist of MOSFETs whose gate is enclosed in SiO_2.



- The poly-Si gate is “floating”, that is, not connected to an external circuit.
- Any charge in the poly-Si gate is trapped “permanently” (> 5 years), since the gate is surrounded by SiO_2.

- Depending on the charge on the gate, the transistor is either in the "on" or "off" state.

Band diagram



EPROM programming:

An EPROM is programmed by excessive DS voltages. Such high voltages create “hot” electrons which reach the gate.

EPROM erasing:

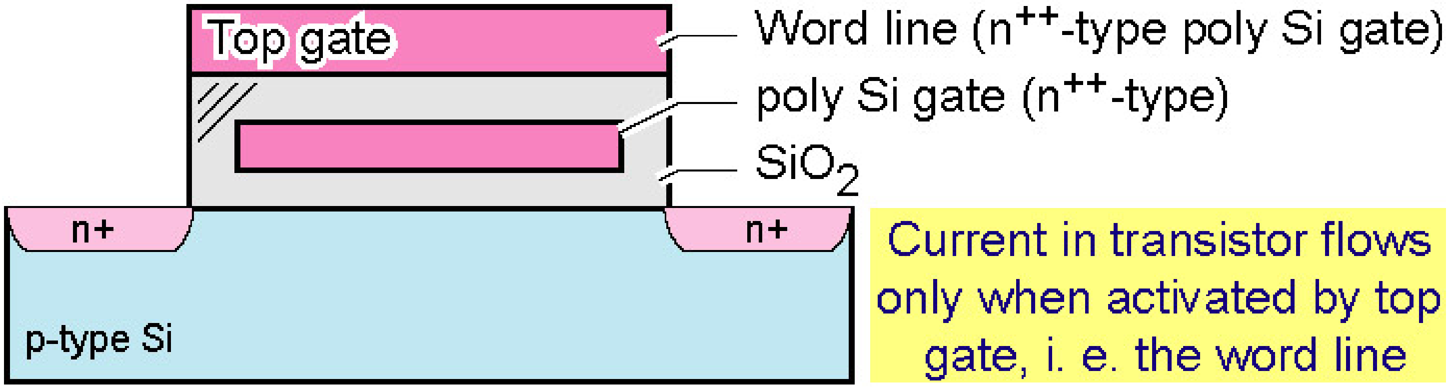
EPROMs can be erased by UV radiation. Electrons are excited high into the band and are then able to leave the gate.

Can EPROMs loose their information? Yes, by tunneling of electrons from the gate to S or D or to the channel. This is a very slow process. **Why?**

EPROM with low power consumption

Assuming that the information stored in a memory chip is 50 % “0s” and 50 % “1s”, half of the EPROM transistors would permanently draw a current. This is problematic for ICs with millions of transistors. The power consumption can be reduced by a second gate (word line) that switches the transistors “on” only when reading the stored information.

EPROM with low power consumption



Current in transistor flows only when activated by top gate, i. e. the word line

Example:

Consider an EPROM transistor (n-channel FET) which is "on" at V_{GS} = 2.0 V. Assume the following additional parameters: L_G = 2 μm, Z = 20 μm, d_{OX} = 100 Å = 100 × 10^{-10} m, ε_r = 11.0.

(a) Calculate the charge on the gate of an EPROM transistor.

(b) Calculate the number of electrons missing on gate.

Solution:

(a) $$Q = CV = \frac{\varepsilon}{d_{OX}} Z \, L_G \, V = 7.8 \times 10^{-13} \text{ C}$$

(b) $$\# \text{ of electrons} = Q/e = 4.8 \text{ million}$$

MOSFET scaling

Scaling of MOSFETs is an advances science.

There are different scaling strategies, namely constant-voltage scaling and constant-field scaling.

There are also fundamental physical limits to scaling. These limits are, tunneling effects, oxide breakdown, avalanche breakdown, and the punch-through effect.