Optically functional surface composed of patterned graded-refractive-index coatings to enhance light-extraction of GaInN light-emitting diodes

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Graded-refractive-index (GRIN) coatings, composed of multiple dielectric layers of TiO_2 and SiO_2 are sputter-deposited on the nitrogen-face of thin-film GaInN/GaN light emitting diodes (LEDs). The thickness and refractive index of each layer in the GRIN stack is designed to minimize light trapping inside the LED caused by total internal reflection at the semiconductor–air interface. Patterning the GRIN stack forms an optically functional surface, which converts trapped modes of light into desirable extracted modes that have preferential directions. Inductively coupled-plasma reactive-ion-etching is used to fabricate various patterns, including arrays of cylindrical pillars and diamond-shaped pillars on the GRIN coatings. In comparison to an uncoated planar reference device, the light-output power is enhanced by 131% and 104% for an array of GRIN diamond-shaped pillars and an array of GRIN cylindrical pillars, respectively. This enhancement in light-output power is comparable to N-face roughened LEDs, which show an enhancement of 124%. In addition, the peak emission intensity of the GRIN LEDs with an array of GRIN pillars is between 25° and 55° off-surface-normal. © *2011 American Institute of Physics*. [doi:10.1063/1.3632072]

I. INTRODUCTION

Total internal reflection (TIR), caused by the high refractive index contrast between the semiconductor of light emitting diodes (LEDs) and the surrounding medium, traps light as guided modes inside the semiconductor.[1] This leads to a significant portion of the light, generated by the active region of the LED, remaining confined inside the semiconductor material. Only a small percentage of light ($\approx 1/4n^2$ per surface, where n is the high refractive index of the semiconductor) is extracted from the LED chip when no techniques promoting light-extraction are used. Various efforts to address this fundamental problem include wet-chemical texturing of the LED chip surface,[2–7] 2D photonic crystals,[8,9] planar graded-refractive-index anti-reflection coatings,[10] patterning of sapphire substrates,[11] and the shaping of LED chips.[12] The fabrication of sub-micron patterns by lithography is elaborate and limits the application of photonic crystals for LEDs. Crystallographic wet chemical texturing is the most popular technique to enhance light extraction of GaInN LEDs, but can be applied only to thin-film LEDs with the nitrogen-face (N-face) GaN surface being exposed.[7] Also, epitaxial growth of a relatively thick GaN layer is required for KOH based wet chemical etching. Due to the crystal-plane dependent etch rate, the surface roughness is highly random and results in a Lambertian emission pattern. In comparison, non-random features of graded-refractive-index (GRIN) patterns can be designed and deliberately fabricated on the surface of an LED chip. The GRIN patterns make the surface of the chip optically functional, i.e., when properly designed, the emission direction can be tailored, increasing the light emission in desired directions and thus eliminating the use of lossy secondary and tertiary optics on the LEDs.

II. THEORETICAL CALCULATION AND DESIGN OF GRIN PATTERNS

The structure of a standard LED is a rectangular parallelepiped with six planar surfaces. Each of these surfaces can be a semiconductor–air/epoxy interface with high refractive index contrast. As shown in Fig. 1(a), only those light rays striking the interface at an angle less than the critical angle, $\theta_c = \sin^{-1}(n_0/n_s)$, can be transmitted to the surrounding medium. Thus, transmittance of light through a planar surface is restricted to an escape cone, which is bounded by the critical angle. When a GaN LED, with emitting wavelength of 450 nm and refractive index $n_s = 2.47$ is surrounded by air, $n_0 = 1$, the critical angle at the interface is only 24°. All rays of light incident at the surface between 24° and 90° are totally internally reflected back into the semiconductor. Assuming isotropic emission inside the GaN LED and using a high-refractive-index approximation, only about $n_0^2/4n_s^2 \approx 4\%$ is extracted through each surface.[1]

For the sake of simplicity, a planar geometry is considered to trace the path of light rays striking the semiconductor–air interface. In case of a cylindrical pillar of refractive index n_p being formed on a semiconductor surface, as shown in Fig. 1(b), light is extracted through the top surface of the pillar as well as the circular surface forming the side of the pillar, thus enhancing the total range of angles which are extracted from

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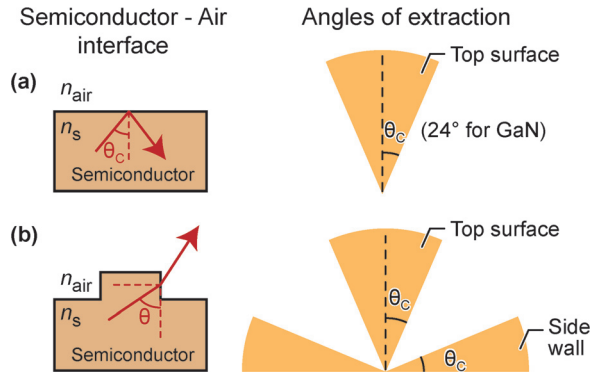

FIG. 1. (Color online) (a) For a planar semiconductor, only those light rays striking the interface at an angle less than the critical angle, θ_c (24° for GaN), are transmitted to the surrounding medium. (b) When a pillar is placed on the semiconductor, light can be extracted through the top surface of the pillar as well as the circular side surface of the pillar.

the semiconductor. If $n_p = n_s = 2.47$ (for GaN), then light striking the semiconductor–pillar interface at angles between $\theta = 66°$ and $\theta = 90°$ could enter the pillar and then be extracted through the sidewall. The probability of a light ray to strike the sidewall after entering the pillar will depend on the height and diameter of the pillar.

Fig. 2 shows a light ray that strikes the semiconductor–pillar interface at an incident angle θ_s, enters the cylindrical pillar at an angle θ_p, and leaves the cylindrical pillar at an angle θ_0. For a ray to trace this path, the ray should not be total internally reflected at the semiconductor–pillar interface or the pillar–air interface. According to Snell's law, a lower and upper bound on the refractive index of the pillar, n_p, avoids TIR at the semiconductor–pillar interface and pillar–air interface, respectively.

Lower Bound: For absence of TIR at the semiconductor-pillar interface,

$$n_p > n_s \sin\theta_s. \tag{1}$$

Upper Bound: For no TIR at the horizontal pillar–air interface,

$$n_0 > n_p \sin(90° - \theta_p). \tag{2}$$

Also from the Snell's law at the semiconductor-pillar interface,

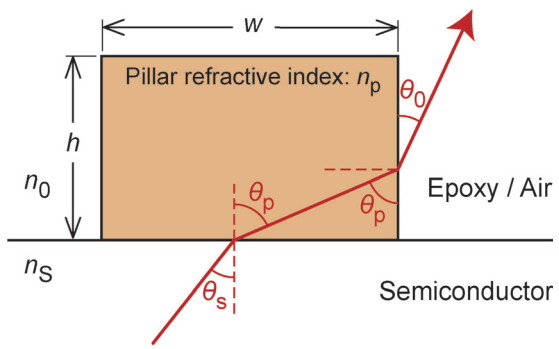

FIG. 2. (Color online) Light ray at an incident angle, θ_s, strikes the pillar of refractive index, n_p, and height, h. The ray leaves the pillar at an angle θ_0.

$$n_s \sin\theta_s = n_p \sin\theta_p. \tag{3}$$

By squaring Eqs. (2) and (3) and adding the LHS and RHS, we get

$$n_0^2 + n_s^2 \sin^2\theta_s > n_p^2. \tag{4}$$

Rearranging Eq. (4) and taking the square root, we get

$$n_p < \sqrt{n_0^2 + n_s^2 \sin^2\theta_s}. \tag{5}$$

For each angle of incidence, θ_s, of a ray striking the semiconductor–pillar interface, there is a lower and upper bound for the refractive index of the pillar, n_p, to avoid TIR, given by Eqs. (1) and (5), respectively. By using different refractive index layers stacked on top of each other, pertaining to a range of angles of incidence at the semiconductor–pillar interface, TIR for all angles above the critical angle can be completely eliminated. Also, the higher refractive index layers need to be stacked at the bottom of the pillar to avoid TIR between these layers.

As shown in Fig. 3, for a GaN LED, the first layer of the pillar with refractive index $n_{p1} = 2.47$ extracts rays with $90° > \theta_s > 66°$. The height of the first layer is chosen such that the ray incident on the semiconductor–pillar interface at 66° necessarily meets the sidewall of the first layer of the pillar. If h_1 is the height of the first layer and w is the diameter of the pillar, the geometric condition that needs to be fulfilled is as follows:

$$h_1 > \frac{w \tan\theta_c}{2}, \text{where} \quad \theta_c = \sin^{-1}\left(\frac{n_0}{n_{p1}}\right). \tag{6}$$

The second layer of the pillar with refractive index $n_{p2} = 2.26$ extracts rays with $66° > \theta_s > 55°$. The height of the second layer is chosen such that the ray incident on the semiconductor–pillar interface at 55° necessarily meets the sidewall of the second layer of the pillar. With 5 layers corresponding to 5 independent ranges of angles listed in Fig. 3, all rays of light incident on the semiconductor–pillar

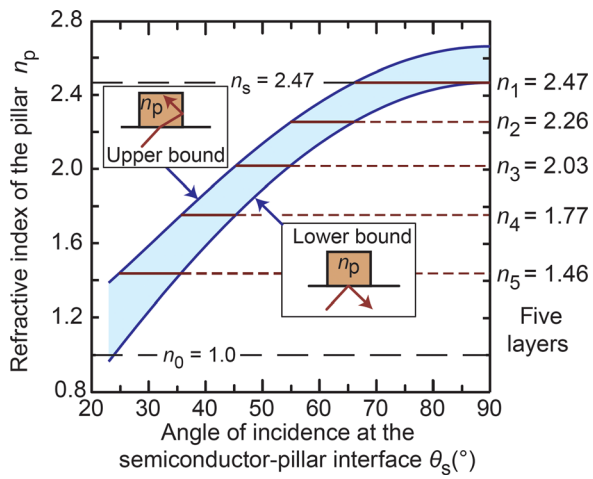

FIG. 3. (Color online) Five discrete layers are designed, using the upper and lower bound of the refractive index, to extract all light incident on the semiconductor–pillar at angles greater than the critical angle, θ_c (24° for GaN).

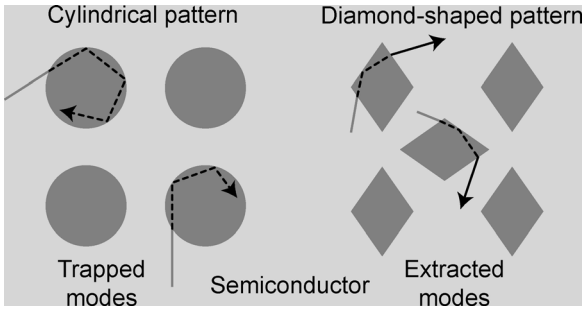

FIG. 4. Schematic showing the top view of cylindrical and diamond-shaped patterns placed on the top surface of the semiconductor. The transparent lines, dashed lines, and solid lines depict the light rays inside the semiconductor, inside the pillars, and extracted by the patterns, respectively.

interface at angles greater than the critical angle 24° can be extracted through the side walls of the different layers of the pillar. For certain spacing between the pillars, the height of each layer in the GRIN stack is a trade-off between (i) maximizing light emitted through the side walls and (ii) lowering the probability of light re-entering a neighboring pillar.

The GRIN patterns are designed to eliminate total internal reflection in the cross-sectional plane normal to the surface of the semiconductor. Light can continue to be trapped in the surface plane of the semiconductor. Few of the light rays inside cylindrical pillars reflect off the side walls and remain trapped. These trapped rays move along the periphery and are often referred to as whispering gallery modes. When the pattern contains pointed shapes, such as a diamond-shape, the light ray reflects at the sharp edges and eventually escapes from the pillar. Fig. 4 depicts trapped modes inside the cylindrical pattern and the extracted modes in a diamond-shaped pattern. Diamond-shaped pillars, when placed complimentary to each other, presumably extract all trapped modes inside the semiconductor.

III. FABRICATION PROCEDURE

Thin-film vertical 1×1 mm^2 GaInN LEDs emitting at 445 nm are used as a reference. They are grown by metal-organic vapor-phase epitaxy on a c-plane sapphire substrate and consist of an undoped GaN buffer layer, an *n*-type GaN layer, a GaInN/GaN multiple quantum-well active region, a *p*-type AlGaN electron blocking layer, and a *p*-type GaN upper cladding layer. A KrF excimer laser is used for a laser lift-off process to separate the GaN from the sapphire substrate. For the planar reference LEDs, the separated N-face GaN surface is planar and has no passivation layer. The roughened reference LEDs have N-face GaN surface roughened by crystallographically wet etching using an aqueous 10% KOH (weight ratio) solution for 4 min at 50 °C.

GRIN patterns are fabricated on the N-face of LEDs with identical epi-structure as follows: Varying compositions of TiO_2 and SiO_2 are sputter-deposited on the N-face of thin film LEDs. Argon and oxygen gases are flown into the sputter chamber at flow rates of 10 sccm and 0.5 sccm, respectively. The pressure of the chamber is maintained at 2 mTorr. The substrate plasma is generated at 100 V bias and the substrate is kept at room temperature during the sputter deposition. Each $(TiO_2)_x(SiO_2)_{1-x}$ layer has a desired x value, which is achieved by adjusting the electrical power applied to the two sputtering targets. Ellipsometry measurements are used to determine the refractive index and thickness of the thin films deposited on the substrates. The refractive index of each $(TiO_2)_x(SiO_2)_{1-x}$ layer depends on the volume ratio of the TiO_2 and SiO_2 mixture. Table I shows the power applied to the TiO_2 and SiO_2 targets, the duration of the sputter-deposition, the measured refractive index, and the measured thickness of the five layers of TiO_2 and SiO_2 that are deposited to form the GRIN stack. The total thickness of the GRIN stack is around 1.6 μm. Additionally, 127 nm of ITO is sputter-deposited to serve as a hard mask for the following inductively coupled plasma (ICP) reactive ion etch (RIE).

Photo-lithography for patterning the ITO hard mask is performed with Shipley Company's S1813: a standard photoresist. Various patterns are formed on the ITO layer, including arrays of cylindrical pillars with diameter 2 μm and spacing 2 μm and diamond-shaped pillars with a longer diagonal of 4.7 μm and a shorter diagonal of 2 μm. The ITO layer is etched under 200 W ICP power and 150 W RIE power with 10 sccm of CH_4, 100 sccm of H_2, and 10 sccm of Cl_2 at 10 mTorr and 50 °C for 300 s to form the ITO hard mask. The GRIN coatings are subsequently etched under 1000 W ICP power and 400 W RIE power with 60 sccm of CHF_3 at 15 mTorr and 50 °C for 160 s. The remaining plasma etch residue along the side walls is removed by dipping the LEDs in AZ 300t (photoresist stripper) at 80 °C for 30 min. Figs. 5(a) and 5(b) show SEM images of an array of GRIN diamond-shaped pillars and an array of cylindrical pillars, respectively, on the N-face GaN thin-film vertical LEDs. The sidewall is near vertical with a tilt angle of less than 5°, and the remaining residue is minimal.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

At an injection current of 4 mA, the forward voltage is around 2.64 V for the planar reference LEDs, 2.7 V for the roughened LEDs, and 2.67 V for the LEDs with GRIN

TABLE I. Thickness and refractive index of each layer in the graded-refractive-index stack is controlled by the power applied to the TiO_2 and SiO_2 targets and the deposition time.

Layer number	Power applied to TiO_2 target	Power applied to SiO_2 target	Deposition time	Measured layer thickness	Measured refractive index
1	200 W	0 W	240 min	333 nm	2.47
2	200 W	50 W	180 min	331 nm	2.26
3	200 W	100 W	120 min	323 nm	1.99
4	200 W	150 W	90 min	330 nm	1.83
5	0 W	200 W	120 min	260 nm	1.46

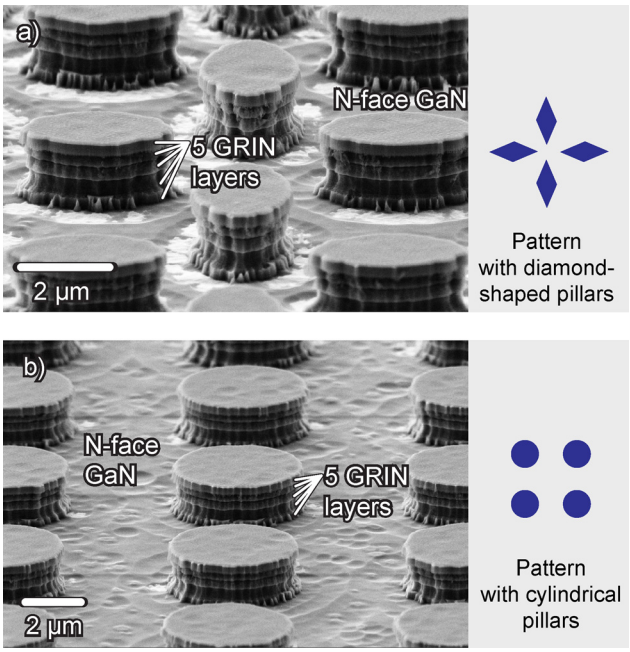

FIG. 5. (Color online) SEM images of (a) an array of diamond-shaped pillars and (b) an array of cylindrical pillars etched under 1 kW ICP power and 400 W RIE power with 60 sccm of CHF_3 at 15 mTorr and 50 °C.

patterns. The light-output power from the LED chip is measured using a lab-made far-field emission setup with a blue-enhanced Si PIN photo-detector that is moved by a rotating arm similar to goniometry. The alignment of samples and non-interference of the probe tips with the measurement are important for a symmetric far-field measurement. The total light-output power is calculated by integrating the voltage measured on a resistive load of the photo-detector at various emission angles. Fig. 6 shows the improvement in total light-output power for the planar reference LEDs, the roughened reference LEDs, and the GRIN LEDs with cylindrical and diamond-shaped patterns. The total light-output power of roughened reference LEDs is enhanced by 124% in comparison to the planar reference LED. The total light-output power is enhanced by 131% and 104% with an array of GRIN diamond-shaped pillars with 4.7 μm longer diagonal (and 2 μm shorter diagonal) and with an array of GRIN cylindrical pillars with 2 μm diameter, respectively. Also, the total light-output power is less for larger width and diameter of the same pattern. Fig. 7 shows far-field emission intensity of the planar reference LEDs, the roughened LEDs, and the GRIN-patterned LEDs. The maximum intensity of light is at 0° (normal to the surface of the LED) and the far-field pattern is Lambertian for both the planar reference and the roughened LED. However, the peak emission intensity of the LED with GRIN pillars is between 25° and 55° off-surface-normal. The strong side emission is consistent with our expectations resulting from theoretical calculations.

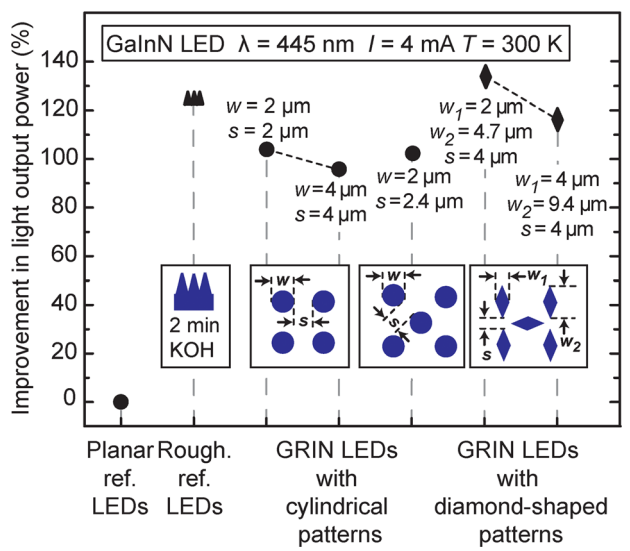

FIG. 6. (Color online) Light-output power of planar reference LEDs, roughened reference LEDs, LEDs with GRIN cylindrical patterns, and LEDs with diamond-shaped patterns.

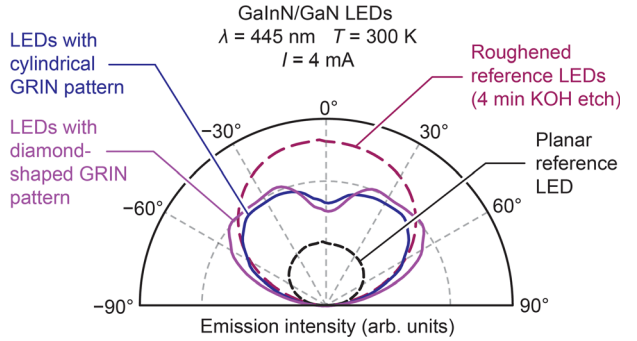

FIG. 7. (Color online) Far-field emission intensity of planar reference LEDs, KOH-roughened reference LEDs, LEDs with GRIN cylindrical patterns with 2 μm diameter, and LEDs with GRIN diamond-shaped patterns with 4.7 μm longer diagonal and 2 μm shorter diagonal.

V. SUMMARY

We have proposed and demonstrated a strategy to design graded-refractive-index patterns that enhance the light extraction of LEDs. GRIN coatings made up of multiple dielectric layers of TiO_2 and SiO_2 are patterned to form pillars by ICP-RIE using the ITO hard mask. In comparison to the planar reference device, the total light-output power is enhanced by 131% and 104% with an array of GRIN diamond-shaped pillars with 4.7 μm longer diagonal (and 2 μm shorter diagonal) and with an array of GRIN cylindrical pillars with 2 μm diameter, respectively. In addition, the peak emission intensity of the LED with an array of GRIN pillars is between 25° and 55° off-surface-normal. The patterned GRIN coatings are a novel type of optically functional surface which can convert trapped modes of light inside a semiconductor into designable modes with desirable properties, such as preferential direction of emission and polarization of light.

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