Inductively coupled plasma etching of graded-refractive-index layers of TiO_2 and SiO_2 using an ITO hard mask

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Transparent dielectric layers with varying compositions of TiO_2 and SiO_2, and ITO are deposited on sapphire and Si substrates by using an RF sputter system. Inductively coupled plasma (ICP) reactive ion etching (RIE) of the ITO hard mask is examined under H_2, CH_4, and Cl_2 chemical environments. The slope of the sidewall and the etch residue on the sidewall of the ITO hard mask are controlled by the flow rates of H_2, CH_4, and Cl_2. ICP-RIE dry etch of TiO_2 and SiO_2 is investigated under fluorinated environments. Comparable etch rates of TiO_2 and SiO_2 (ratio $\approx$ 2:1) and high selectivity $\gg 1$ over ITO are found. Graded-refractive-index (GRIN) layers, made up of multiple dielectric layers of TiO_2 and SiO_2, are patterned to form cylindrical pillars by ICP etching using the ITO hard mask. Fluorine containing residues are identified on the TiO_2 and SiO_2 surfaces. Various etch chemistries are investigated to obtain smooth, vertical, and residue-free sidewalls of the GRIN pillars. © *2011 American Vacuum Society*. [DOI: 10.1116/1.3620494]

I. INTRODUCTION

Applications for thin film TiO_2 include dye-sensitized solar cells,[1] optical waveguides,[2] distributed Bragg reflectors, light-emitting diodes (LEDs),[3,4] and as potential replacements for SiO_2 in advanced gate stacks on metal-oxide semiconductor field effect transistors.[5] TiO_2 and SiO_2 have a high refractive index ($n \approx 2.5$) and a low refractive index ($n \approx 1.5$), respectively, and both are optically transparent in the visible and the near-IR region.[6,7] Varying compositions of TiO_2 and SiO_2 can be cosputtered to deposit thin films of any refractive index between those of TiO_2 and SiO_2. The volume ratio of TiO_2 and SiO_2 in a deposited dielectric film, defined as "x" in $(TiO_2)_x(SiO_2)_{1-x}$, determines the refractive index of the composite material. Deposition of thin dielectric layers of different compositions of TiO_2 and SiO_2 forms a stack of graded-refractive-index (GRIN) layers. GRIN layers have been used as antireflection coatings for applications such as solar cells[8] and as optical interference filters.[9]

Further applications of GRIN layers rely on the development of etching methods that are suitable for patterning both TiO_2 and SiO_2 thin films. One application of such a patterned stack of GRIN layers is to enhance light extraction efficiency of an LED.[10] Various wet etch solutions for TiO_2 and SiO_2, including H_2SO_4, HCl/HNO_3, HF/NH_4F, and HO/HNO_3, have been reported.[11–13] However, inductively coupled plasma (ICP) reactive ion etching (RIE), being anisotropic, is necessary for etching deep trenches with vertical sidewalls. In this paper, we report on the etch rates, fluorine based residues, and the sidewall profiles of a GRIN layer-stack of TiO_2 and SiO_2, under ICP-RIE. The ICP-RIE is done under different fluorine-based plasma chemistries and plasma powers using a ITO hard mask.

II. FABRICATION

During the cosputtering of TiO_2 and SiO_2 sputtering targets, $(TiO_2)_x(SiO_2)_{1-x}$ layer with a desired x value is achieved by adjusting the electrical power applied to the two sputtering targets. For calibration, different powers were applied to the TiO_2 and SiO_2 targets to deposit dielectric layers on polished Si substrates. Argon and oxygen gases were flown into the sputter chamber at flow rates of 10 and 0.5 sccm, respectively. The pressure of the chamber was 2 mTorr. 100 V was applied to the substrate plasma and the substrate was kept at room temperature during the sputter deposition. Ellipsometry measurements are used to determine the refractive index and thickness of the thin films deposited on the substrates. The refractive index of SiO_2 and TiO_2 at a wavelength of 450 nm is 1.46 and 2.47, respectively. The refractive index (n) of the dielectric layer is dependent on the volume ratio of TiO_2 in the TiO_2–SiO_2 mixture as follows:

$$n(TiO_2 + SiO_2) = n(SiO_2) + \left(n(TiO_2) - n(SiO_2)\right) \times \frac{\text{volume}(TiO_2)}{\text{volume}(TiO_2) + \text{volume}(SiO_2)}.$$

Figure 1 shows the refractive index of the dielectric films at a wavelength of 450 nm (left ordinate) and the deposition rate versus the power applied to the TiO_2 and SiO_2 targets (right ordinate). It also shows the volume ratio of TiO_2 in the TiO_2–SiO_2 mixture corresponding to the measured refractive index of the dielectric films.

Five layers of different volume ratios of TiO_2 and SiO_2 are deposited on sapphire to form graded-refractive-index layers. Table I shows the power applied to the TiO_2 and

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SiO_2 targets used during deposition for each layer in the stack of GRIN layers. The total thickness of the GRIN stack is around 1.4 μm. Photoresist (PR) is an efficient mask for dielectric and metal patterning. But dry etching has low etch selectivity of PR over the dielectric material. Also the degradation of the PR during the ICP-RIE process limits the etching depth and sidewall smoothness. Therefore, indium tin oxide (ITO) is being used in this work as a hard mask due to its strong resistance to ICP-RIE in fluorinated environments and its optical transparency to visible and near infrared light. The composition of ITO consists of In_2O_3 and SnO_2 at a ratio of 90:10. 150 nm thick ITO is sputter deposited. The power applied to the ITO target is 30 W. The pressure and reactive gas flow rates is similar to the prior deposition of the TiO_2 and SiO_2. Photo-lithography for the ITO hard mask patterning is performed with Shipley Company's S1813, a standard photoresist. ICP-RIE etching of the ITO hard mask is examined using H_2, CH_4, and Cl_2 environments.

III. ICP-RIE DRY ETCH OF THE ITO HARD MASK

Traditionally ITO dry etching is done under an Ar/CH_4 chemistry.[14] Ar contributes towards physical etching via bombardment of the sample by its heavy ions and CH_4 contributes towards the reactive chemical etching via CH_4^+ and CH_3^+ reactants.[15] In an etching process with pure methane or hydrocarbon-dominant environment; however, much of the reaction is hindered by carbon residue on the ITO surface. A small quantity of oxygen in the plasma environment helps remove the carbon residue. Figures 2(a) and 2(b) show scanning electron microscopy (SEM) images of an ITO pillar on a Si substrate etched under 600 W ICP power, 150 W RIE power with a 30 sccm flow of CH_4, 15 sccm of Ar, and 5 sccm of O_2 at a pressure of 10 mTorr and a chuck temperature of -10 °C. Figures 2(a) and 2(b) show that the PR has severely degraded during the ICP etch due to the physical bombardment of Ar ions and reaction with O_2. After the PR is further removed by sonicating the sample in acetone solution, the corners of the ITO pillar show corrugated features caused by heavy damage. The degradation of PR during the

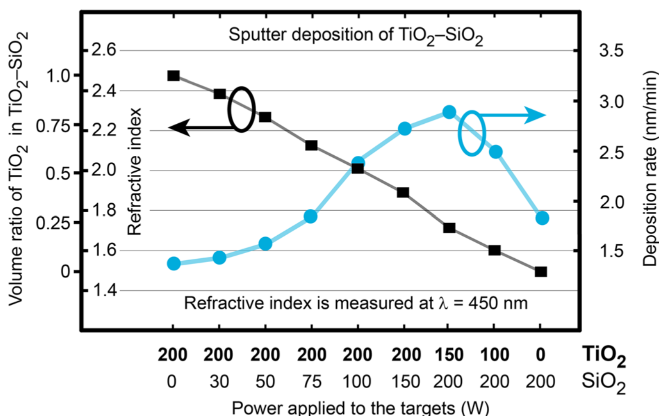

FIG. 1. (Color online) Refractive index measured at $\lambda = 450$ nm and deposition rate of the cosputtered TiO_2–SiO_2 layers vs the power applied the TiO_2 and SiO_2 targets. The refractive index of the layer is related to the volume ratio of TiO_2 in the TiO_2–SiO_2 mixture.

ICP etch exposes the corners of the pillar to physical bombardment of Ar ions thereby causing damage to the ITO.

The use of hydrogen in the etching ambient during dry etching of ITO offers several distinct advantages over Ar-based etches. The physical damage of the surface caused by hydrogen ions is lower than the physical damage of the surface caused by Ar ion bombardment.[16] Thus, the use of H_2 instead of Ar results in less PR and ITO damage. The presence of hydrogen in the environment eliminates the significant problem of carbon residue formation on the surface of the ITO-coated sample and the etch-chamber walls. The hydrogen ions dissociate oxygen from ITO and then remove the remaining In and Sn from the sample surface. Figures 3(a) and 3(b) show SEM images of an ITO pillar on Si substrate etched under 200 W ICP power, 150 W RIE power with 10 sccm of CH_4 and 50 sccm of H_2 at 10 mTorr and 50 °C. Prior to the ICP etch, PR was hardened and reflowed by heating it on a hot plate at 130 °C for 5 min. As seen in Fig. 3(a), the PR has withstood the ICP dry etch. Also the corners of the PR in the square pillar are rounded during reflow. Figure 3(b) shows the underlying ITO film after the PR is further removed by sonicating in acetone solution. The resulting ITO pillar is undamaged and the corners of the square pillar are rounded, reflecting the shape of the reflown PR. But there is polymer formation on the sidewalls of ITO from residual PR. Even though this can be removed by using an O_2 plasma in a plasma asher or by heating in a PR stripper, the sidewalls underneath the residue are not smooth. As ITO is being used as a hard mask for etching GRIN of TiO_2 and SiO_2, the sidewall profile of ITO is critical to the sidewall profile of the graded index layers.

As the PR was reflowed by heating it on a hot plate at 130 °C for 5 min, the PR has a dome shape instead of a vertical-pillar shape. When a small quantity of Cl_2 is added to the plasma environment, the PR is consumed faster during the etch process both in the vertical and the lateral direction. This leads to a reduction in both the height and the width of the PR dome as shown in the schematic of Fig. 4(a). Due to the consumption of the PR in the lateral direction, the sidewall of the ITO is etched as it is under the line of sight of the reactive ions. The resulting sidewall of the ITO pillar is no longer vertical and the width of the ITO pillar is reduced. Also there is no residual PR and a thinner passivation layer along the sidewall. Figure 4(b) shows a SEM image of an ITO pillar on sapphire substrate etched under 200 W ICP power, 150 W RIE power with 12 sccm of CH_4, 50 sccm of H_2, and 6 sccm of Cl_2 at 10 mTorr and 50 °C after removal of PR. The SEM image shows no polymer formation in the ITO sidewalls. The taper angle of ITO depends on the relative rates of vertical etching of ITO and etching of PR. The vertical etch rate of ITO can be controlled by the flow of CH_4 while the etch rate of PR can be controlled by the flow of Cl_2. Table II shows gas compositions used during the ICP-RIE etch of the ITO that result in different taper angles of the resulting ITO patterns. Figure 4(c) shows a SEM image of an ITO pillar on sapphire substrate etched under 200 W ICP power, 150 W RIE power with 10 sccm of CH_4, 90 sccm of H_2, and 10 sccm of Cl_2 at 10 mTorr and 50 °C

TABLE I. Each layer of the refractive index stack is deposited with different values of power applied to the TiO_2 and SiO_2 targets. Different sputter target powers result in dielectric layers with different refractive index values stacked one on top of another.

Layer No.	Power applied to TiO_2 target	Power applied to SiO_2 target	Measured refractive index
1	200 W	0 W	2.47
2	200 W	30 W	2.35
3	200 W	50 W	2.26
4	200 W	70 W	2.13
5	200 W	100 W	2.00

after removal of PR. The taper angle is 43° and 56° for Figs. 4(b) and 4(c), respectively. By adjusting the flow rates, a trade-off between vertical and smooth sidewall can be achieved. Figure 5 shows a SEM image of an ITO pillar on sapphire substrate etched under the optimized conditions of 200 W ICP power, 150 W RIE power with 15 sccm of CH_4, 70 sccm of H_2, and 7 sccm of Cl_2 at 10 mTorr and 50 °C, after removal of PR. The smooth and vertical sidewalls of the ITO micropillars along with minimizing residues during the ITO etching are found in the Fig. 5, which are needed for realizing GRIN vertical micropillars. The etch rate of ITO is around 1 nm/s.

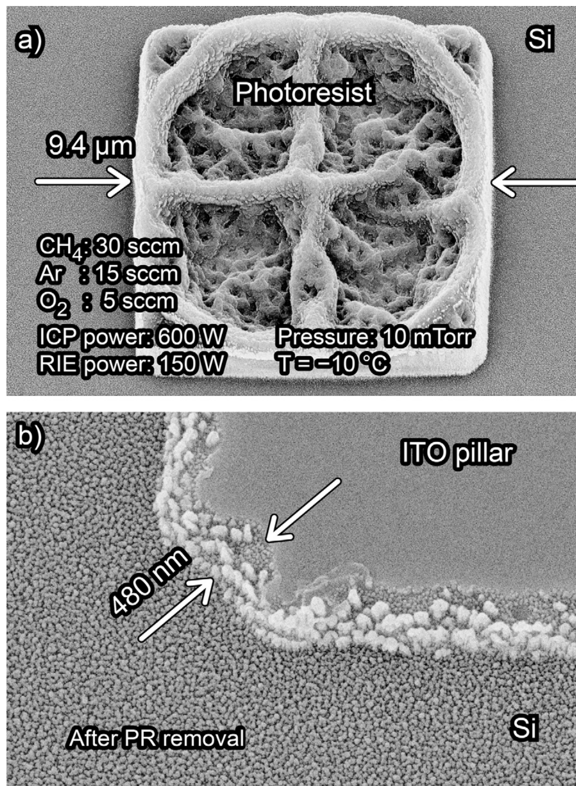

FIG. 2. SEM images of an ITO pillar on a Si substrate etched under 600 W ICP power, 150 W RIE power with 30/15/5 sccm of $CH_4/Ar/O_2$ at 10 mTorr and − 10 °C: (a) with the PR mask and (b) after removal of the PR mask. The PR is damaged and the sidewall of the ITO pillar has etch residues.

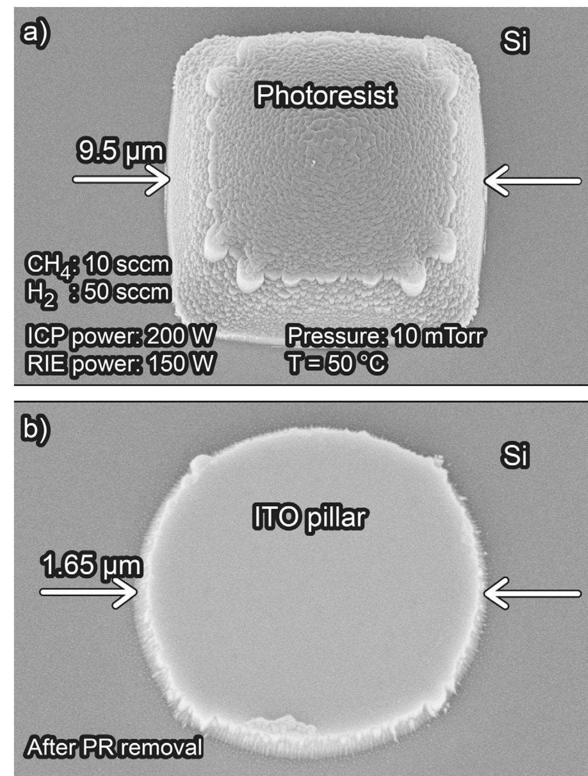

FIG. 3. SEM images of ITO pillars on Si substrate etched under 200 W ICP power, 150 W RIE power with 10/50 sccm of CH_4/H_2 at 10 mTorr at 50 °C after PR hard bake and overflow: (a) with the PR mask, (b) after removal of the PR mask. The PR mask has withstood the dry etch and the resulting ITO pillar is undamaged.

IV. ICP-RIE DRY ETCH OF GRIN LAYERS

To etch deep trenches of GRIN layers containing both TiO_2 and SiO_2, etching behavior under fluorinated environments is investigated. Traditionally TiO_2 ICP dry etch is done under Ar/SF_6 environment.[17] Argon contributes towards physical etching via bombardment of its heavy ions. The addition of SF_6 increases the etch rate drastically, indicating a chemical etching mechanism. Figure 6 shows a SEM image of a TiO_2 pillar etched under 600 W ICP power, 250 W RIE power with 30 sccm of SF_6, and 15 sccm of Ar at 25 mTorr and 0 °C followed by the removal of PR by sonicating in acetone solution and iso-propanol. Fluorine-based residues are seen in the corners of the TiO_2 pillars and are not easily soluble in acetone.

The use of pure CHF_3, instead of SF_6 and Ar, reduces the fluorine-based residues due to the presence of carbon and hydrogen forming volatile byproducts. Figure 7(a) shows a SEM image of a TiO_2 pillar on Si substrate etched under 600 W ICP power, 250 W RIE power with 60 sccm of CHF_3 at 25 mTorr and 0 °C, after the removal of PR by sonicating the sample in acetone solution. The sidewalls of TiO_2 are vertical, smooth and have no fluorine residues. SiO_2 was etched under the same conditions and the result was similar to TiO_2 etch except for less anisotropy in the etch process. Figure 7(b) shows a SEM image of a SiO_2 pillar on Si substrate etched under 600 W ICP power, 250 W RIE power with 60 sccm of CHF_3 at 25 mTorr and 0 °C.

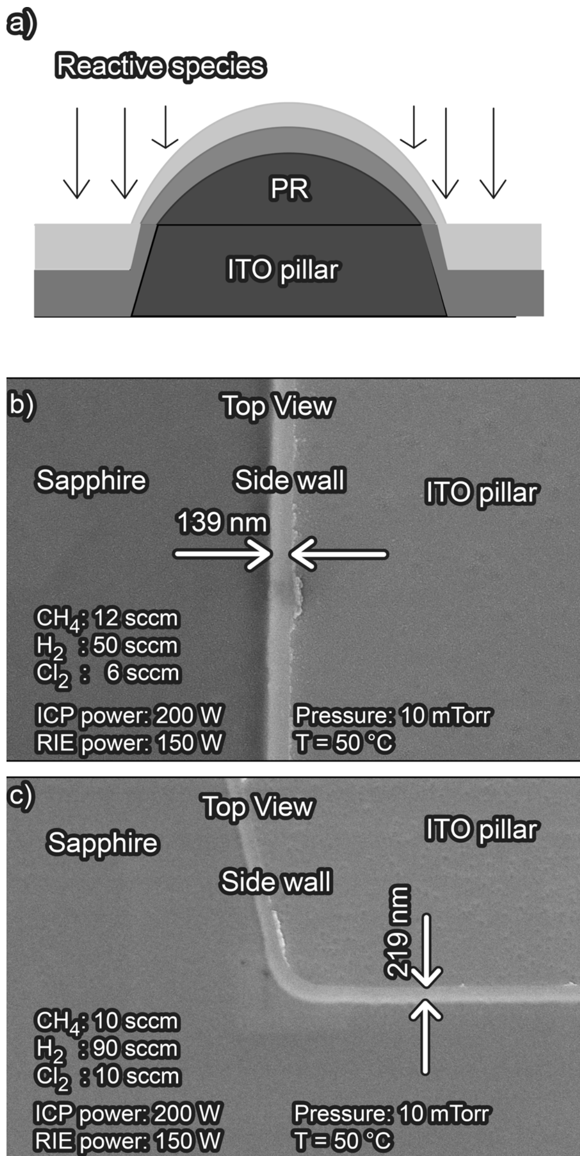

Fig. 4. SEM images of an ITO pillar on a sapphire substrate etched under 200 W ICP power, 150 W RIE power at 10 mTorr and 50 °C: (a) schematic of the ITO dry etch, (b) with 12/50/6 sccm of $CH_4/H_2/Cl_2$, and (c) with 10/90/10 sccm of $CH_4/H_2/Cl_2$. The taper angle of the sidewalls of the ITO pillar can be controlled by the relative flow rates of CH_4 and Cl_2.

Table II. Gas compositions used during the ICP-RIE etch of the ITO that result in different taper angles of the resulting ITO patterns. A 150 nm thickness of ITO was etched under 200W ICP power, 150 W RIE power at 10 mTorr and 50 °C.

CH_4 flow	H_2 flow	Cl_2 flow	Lateral etch	Taper angle
12 sccm	50 sccm	6 sccm	139 nm	43°
10 sccm	50 sccm	10 sccm	321 nm	65°
10 sccm	90 sccm	10 sccm	219 nm	56°
10 sccm	100 sccm	10 sccm	277 nm	62°
15 sccm	70 sccm	6 sccm	36 nm	13°
15 sccm	70 sccm	9 sccm	111 nm	37°

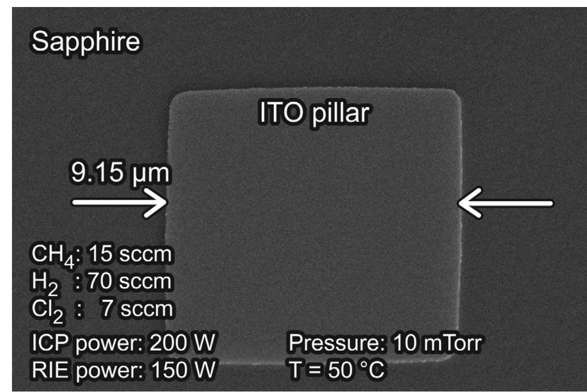

Fig. 5. SEM image of an ITO pillar on sapphire substrate etched under 200 W ICP power, 150 W RIE power with 15/70/7 sccm of $CH_4/H_2/Cl_2$ at 10 mTorr and 50 °C. The sidewalls of the ITO pillar are smooth and vertical.

The GRIN stack was etched under CHF_3 environment using ITO as a hard mask. The fluorine-based residue becomes less when the etching is done under higher ICP and RIE power, lower chamber pressure and at an elevated chuck temperature.[18] The selectivity of the dry etch of GRIN over ITO is compromised when the physical component of the dry etch becomes substantial with an increase in ICP and RIE powers. Figure 8(a) shows a SEM image of a pattern of GRIN layers with ITO hard mask on a sapphire substrate etched under 1000 W ICP power, 400 W RIE power with 60 sccm of CHF_3 at 10 mTorr and 50 °C. The sidewalls have an average taper angle of less than 5°. The GRIN sample was then dipped in PR stripper for 30 min at 80 °C and followed in a buffered oxide etchant (BOE) for 20 s. The SEM image of the GRIN pillar shown in Fig. 8(b) has an average taper angle of 7°, when the sample is etched under BOE solution for 20 s. As each layer in the GRIN stack has a different etch rate under BOE solution, there are steps formed on the sidewall of the GRIN pillar.

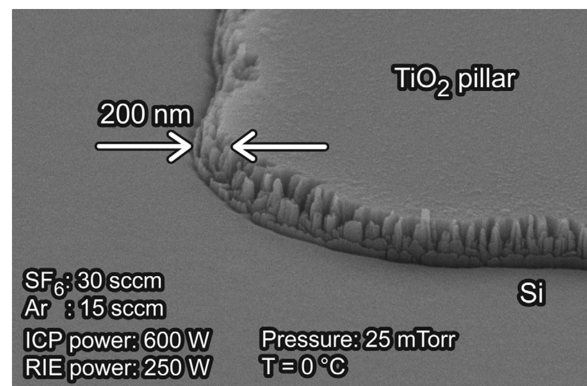

Fig. 6. SEM image of a TiO_2 pillar on Si substrate etched under 600 W ICP power, 250 W RIE power with 30/15 sccm of SF_6/Ar at 25 mTorr at 0 °C. The sidewall of the TiO_2 pillar has fluorine based residues.

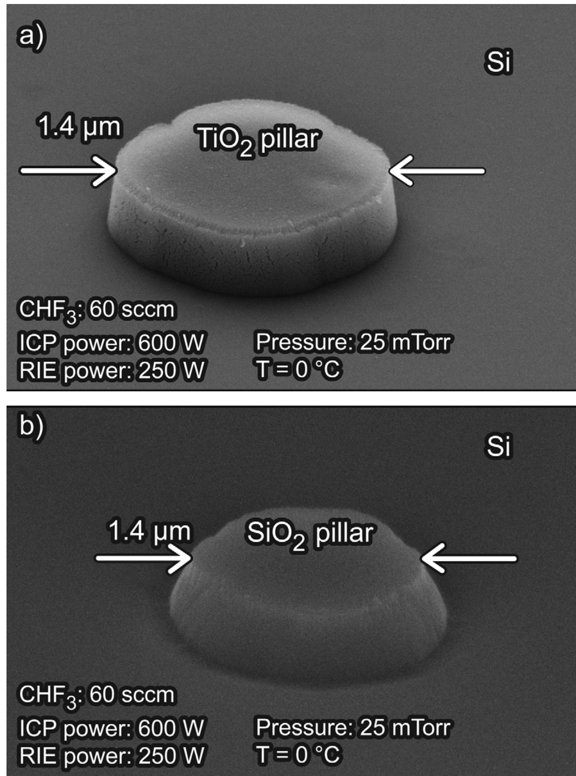

FIG. 7. SEM images of (a) TiO_2 pillar and (b) SiO_2 pillar on sapphire substrate etched under 600 W ICP power, 250 W RIE power with 60 sccm of CHF_3 at 25 mTorr and 0 °C. The sidewalls of the TiO_2 pillar and SiO_2 pillar are smooth and vertical.

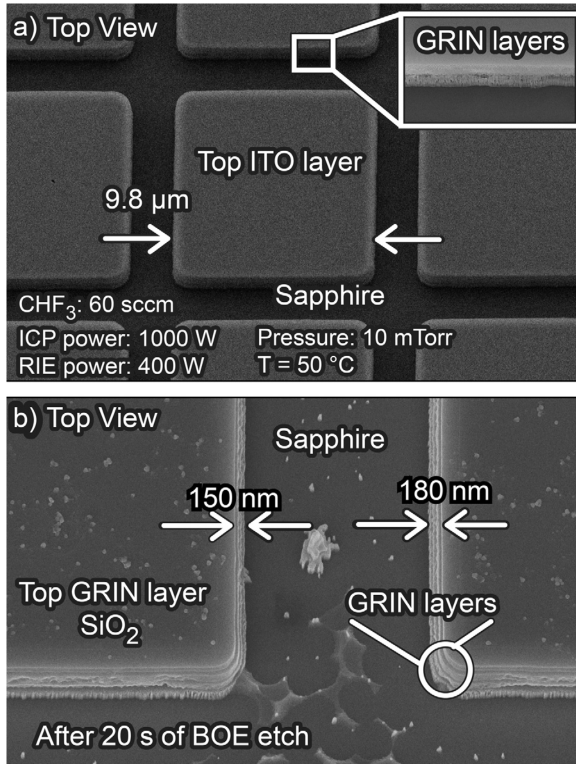

FIG. 8. (a) SEM image of an array of GRIN pillars on sapphire substrate etched under 1000 W ICP power, 400 W RIE power with 60 sccm of CHF_3 at 10 mTorr and 50 °C. (b) SEM image GRIN pillars on sapphire substrate after being dipped in PR stripper for 30 min at 80 °C followed by a 20 s buffered oxide etch (BOE).

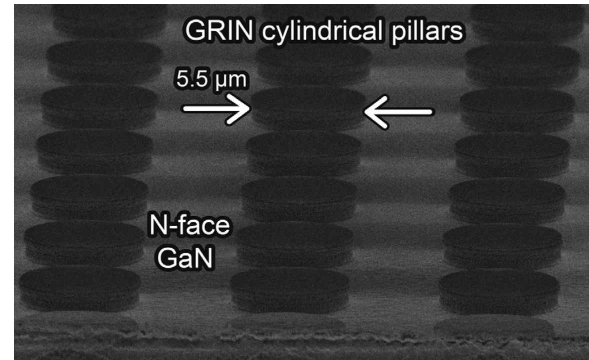

FIG. 9. SEM image of an array of 5.5 μm pillars of five-layer GRIN layers on the nitrogen-face of a GaN vertical LED. The sidewall is near vertical with a taper angle of less than 5°. The residue formation on the pillar's sidewall and top is minimal.

V. DISCUSSION

To demonstrate the viability of forming GRIN micropatterns on LEDs, arrays of cylindrical pillars of 1.4 μm thick GRIN layers with diameter 5.5 μm and spacing 5 μm were formed on 1×1 mm^2 GaInN/GaN LEDs. 150 nm thick ITO hard mask was etched under 200 W ICP power, 150 W RIE power with 15 sccm of CH_4, 70 sccm of H_2, and 7 sccm of Cl_2 at 10 mTorr and 50 °C. The GRIN layers were subsequently etched under 1000 W ICP power, 400 W RIE power with 60 sccm of CHF_3 at 10 mTorr and 50 °C. The etch rate of TiO_2, SiO_2, and ITO under fluorinated environments is 3.8, 6.6, and 0.8 nm/s, respectively. Figure 9 shows a SEM image of an array of GRIN cylindrical pillars on the nitrogen-face GaN vertical LEDs. The sidewall is near vertical with a taper angle of less than 5° and the residue formation is minimal.

VI. SUMMARY

In summary, the fabrication of GRIN micro-patterns has been developed. GRIN layers are made by sputter deposition of multiple dielectric layers of TiO_2 and SiO_2. ICP etching of the ITO hard mask is examined under H_2, CH_4, and Cl_2 chemistry. GRIN layers are patterned to form cylindrical pillars by ICP etching under CHF_3 chemistry using an ITO hard mask. Fluorine containing residues are identified on the TiO_2 and SiO_2 surfaces. Various etch chemistries are investigated to obtain smooth, vertical, and residue-free pillar sidewalls. GRIN micropatterns expand the scope of applications of GRIN materials in electronic and optical devices.

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