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Mesa-Free III-V Nitride Light-Emitting Diodes with Flat Surface

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A mesa-free pn-junction GaInN light-emitting diode (LED) structure is proposed and demonstrated. Some of the p-type top surface area of the LED epitaxial wafer is converted from p-type to n-type by means of Si-ion implantation. The resulting pn-junction LED wafer has cathode and anode contact points at the same surface height so that no dry-etching process is needed to access the n-type region. The measured specific contact resistance on the type-converted n-type layer and the light-output power of the mesa-free pn-junction LED are very comparable to those obtained by a reference LED.

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Light-emitting diode (LED) devices are the driving force behind solid-state lighting with its explosive growth in illumination applications.[1,2] III-V nitride semiconductors such as GaN, InN, AlN, and their ternary and quaternary alloy compounds are core materials for ultraviolet, blue, green, and white LED devices. Many technical breakthroughs have already improved the quality of GaN-based LEDs, but there are still further goals (e.g., higher efficiency, higher optical power intensity per device surface area, and lower cost) to be achieved to further the widespread use of LEDs in solid-state lighting applications.[3–5] A most important 'figure of merit' of LEDs is the power efficiency which has led the GaN-based LED development from a simple top-emitting configuration to an advanced thin-film configuration such as the thin-film flip chip configuration[6] and the thin-film chip configuration that uses via holes for the n-type contact.[7,8]

One of the characteristics of standard III-V nitride LEDs grown on a sapphire substrate is that the anode and cathode contact electrode are located on the same surface, i.e. the top surface. This is because the sapphire substrate is electrically inert (i.e., electrically insulating). Therefore, in order to make a cathode contact (n-electrode), it is mandatory to etch out part of the p-type semiconductor to form a mesa and expose the n-type semiconductor underneath. Inductively-coupled plasma (ICP) reactive-ion etching (RIE) is widely used for this process step. The mesa etching is typically 500 nm deep and done by ICP-RIE under chlorine-based gas chemistry at a few millitorr of pressure. As the result, the LED wafer has an undulated surface topography, which can deteriorate the quality of device during a series of follow-up fabrication steps: For example, the device wafer bonding process is a core process step in the LED fabrication procedure. A difference in surface height for the two contact electrodes makes the wafer bonding process more difficult and non-uniform in terms of its electrical and mechanical characteristics, resulting in a lower yield and thus an increase in fabrication cost. Therefore, it would be very advantageous if the wafer surface would be flat: the LED chip productivity would be improved, which will expedite the adoption of LED technology in high power illumination applications.

In this report, a mesa-free flat-surface pn-junction GaInN LED is demonstrated by employment of ion-implantation technology and without employment of a dry etching mesa-formation process. In the areas to be covered by the cathode contact, the LED epitaxial wafer's p-type surface layer is converted from p-type to n-type conductivity by implantation of a high concentration of Si donors. We investigate the metal ohmic contact properties of the type-converted n-type GaN and fabricate mesa-free LEDs that have cathode and anode contacts at the same surface height.

Figure 1 shows a cross sectional schematic of a mesa-free pn-junction LED where the 'ion implanted n-type region' was converted from its initial p-type to n-type conductivity by Si ion implantation. Thus the cathode can be formed on the type-converted n-type surface without the mesa etching process; consequently the final LED has a flat surface (i.e., the same height of the anode and cathode contact). Figure 1 also shows an 'ion-implanted isolation region'; this region is created by a second ion-implantation step, using N ions, in order to electrically isolate the converted n-type region from the p-type region so that the undesired current path between the p-layer to the converted n-type layer is suppressed.

It has been demonstrated that p-type GaN can be converted to n-type GaN by using Si ion-implantation which is followed by a high temperature anneal to reduce the damage caused by implantation.[9,10] In our experiments, a p-type GaN ($p \sim 6 \times 10^{16}$ cm^{-3}) wafer was implanted with Si doses ranging from 5×10^{14} to 5×10^{15} cm^{-2} and implantation energies of 40, 100, and 200 keV. Figure 2 shows the results of the p-to-n-type conversion when Si-ions are implanted into the as-grown p-type GaN followed by two different annealing conditions: After annealing at 1000°C for 30 minutes, the sample becomes n-type conductive with an electron concentration of up to 4×10^{19} cm^{-3} as determined by Hall-effect measurements. Annealing at a lower temperature of 900°C for 30 minutes also resulted in p-to-n-type conversion; however the resulting electron concentrations are lower than 1×10^{19} cm^{-3}. The mobilities of the p-to-n-type converted layers are between 10 to 20 cm^2/V · s which is a bit lower than those of typical Si-doped n-type GaN layers. The p-to-n conversion efficiency is a function of both implantation dose and temperature, but it shouldn't have to be a linear relationship between two variables. We find that while the dose has high effect on conversion efficiency at low doses (between 5×10^{14} to 1×10^{15} cm^{-2}), the annealing temperature shows its effect at high doses (over 1×10^{15} cm^{-2}).

Next, we investigate if Ti/Al metallization can result in low resistivity ohmic contacts on the 'p-to-n-type converted GaN' layer. A metal stack consisting of Ti and Al (30/250 nm) was deposited on

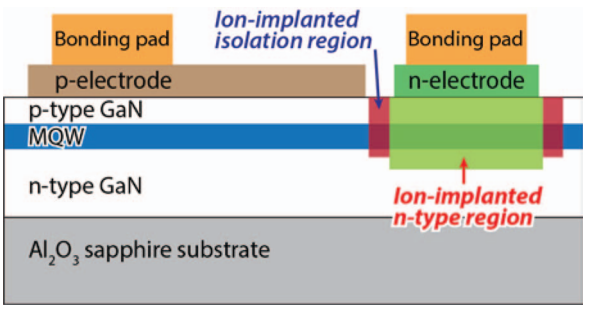

Figure 1. Cross-sectional view of the mesa-free flat pn-junction GaN-based LED.

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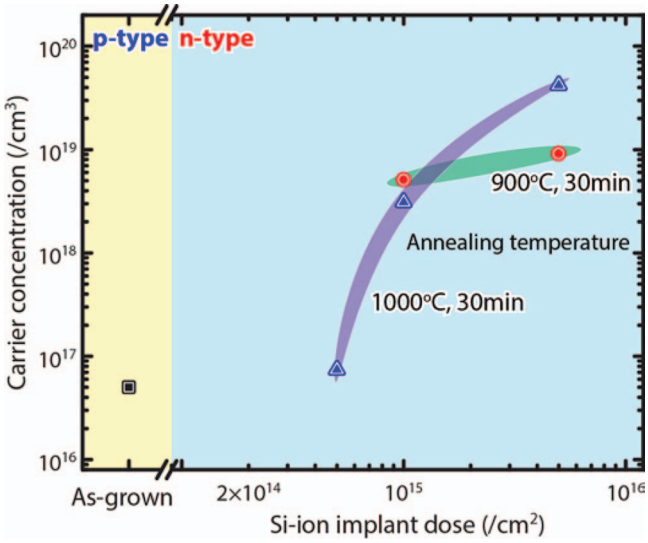

Figure 2. P-to-n conductivity type conversion of MOCVD-grown p-type GaN by using Si ion-implantation.

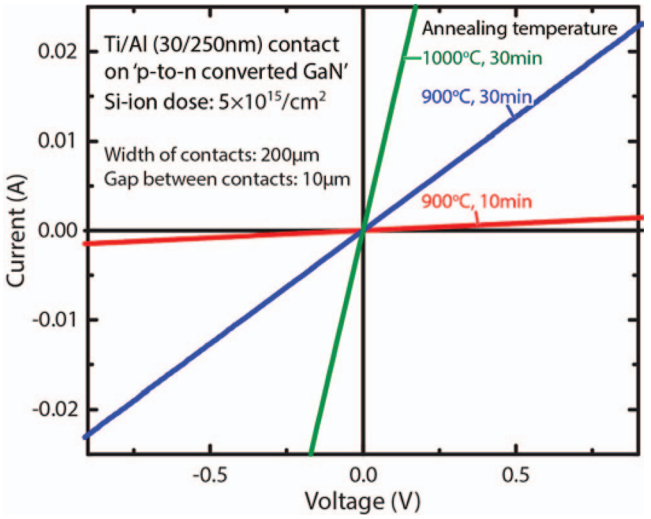

Figure 3. Current–voltage curves of two n-to-n contact electrodes of a TLM pattern on a 'p-to-n-type converted GaN' layer.

Si-ion implanted GaN by using an electron-beam evaporator and subsequent contact anneal at 650°C for 1 minute under an N_2 ambient. The contact resistance and sheet resistance were measured using C-TLM (circular transfer-length method) patterns. Figure 3 shows very linear ohmic characteristics for the metal contacts on 'p-to-n-type converted GaN' layer for the different contact annealing conditions. The measured specific contact resistivity is below 10^{-4} Ω cm^2 which is comparable to typical as-grown n-type GaN.

The commercial III-V nitride LED epitaxial wafer, which has a multiple quantum well (MQW) active region of five GaInN/GaN pairs, is used in this study. First, after areas were photolithographically defined for the n-contact electrodes, Si-ions were implanted using multiple steps with implantation energies of 300, 150, 40, 10 keV and doses of 1×10^{16}, 1×10^{16}, 3×10^{15}, 2×10^{15} cm^{-2}, respectively, to get uniform Si ion distribution up to a 500 nm depth. This process forms the p-to-n-type converted layer from the as-grown p-type GaN. Secondly, in order to create electrically inert layers between as-grown p-type GaN and p-to-n converted GaN, N is implanted into the p-type GaN.[11,12] When N ions are implanted into either conductive p-type or n-type GaN layers using an N dose of 2×10^{13} cm^{-2} and energies of 20, 100, and 175 keV, current flow is not measurable. In addition, we find that these isolation regions are tolerant to high temperature treatment up to 750°C. Finally, we deposited an Ag-based metal and a Ti/Al metal stack for the p-type and n-type electrode, respectively. The chip size and emission peak wavelength of the LED are 300 × 300 μm^2 and about 460 nm at room temperature, respectively. The above-described processes are used to fabricate mesa-free 'flat pn-junction LEDs'. 'Reference LEDs' follow the standard LED fabrication procedure (including mesa etching for exposure of the n-type GaN) and are fabricated alongside the 'flat pn-junction LEDs' on the same wafer, for comparison purposes.

Figure 4 shows the cross-sectional transmission electron microscopy (TEM) images taken from the fabricated LED. The TEM specimen was prepared by using a focused ion beam (FIB) and analyzed under a bright-field (BF) imaging mode to identify the ion-implanted region. As shown in Fig. 4a, the epitaxial layers of the LED structure are in good condition, as designed. On the contrary, the Si-implanted region ("p-to-n-type converted region") are relatively dark compared to the unimplanted region (see Fig. 4b and 4c). Moreover, the MQW cannot be clearly resolved in the implanted region due to intermixing of layers occurring during and after ion implantation. The projected depth of the Si implantation is measured to be about 576 nm which is well matched to the estimation by the TRIM/SRIM software.

Figure 5 shows the measured light-output power (LOP) as a function of current. Note that the LOP of a *typical* flat pn-junction LED is almost identical to the reference LED. Although the conductivity-type-converted region is a little absorptive at the emission wavelength, the portion of the type-converted region is limited so that the effect of light absorption is minimal. We also confirm that the flat pn-junction LED shows a very similar reverse leakage current compared to the reference LED (not shown here). However, as shown in the inset of Fig. 5, the operating voltage of the flat pn-junction LED is higher than that of the reference LED. The inset of Fig. 5 shows that whereas

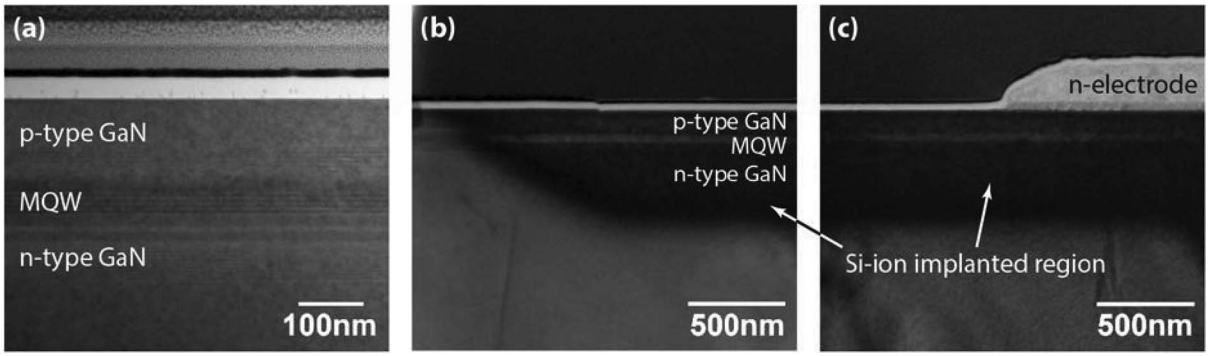

Figure 4. Cross-sectional transmission electron microscope images of the (a) untouched epitaxial layers used in this study, (b) boundary between the p-to-n-type converted layer and the as-grown layer, and (c) the p-to-n-type converted layer under n-type electrode.

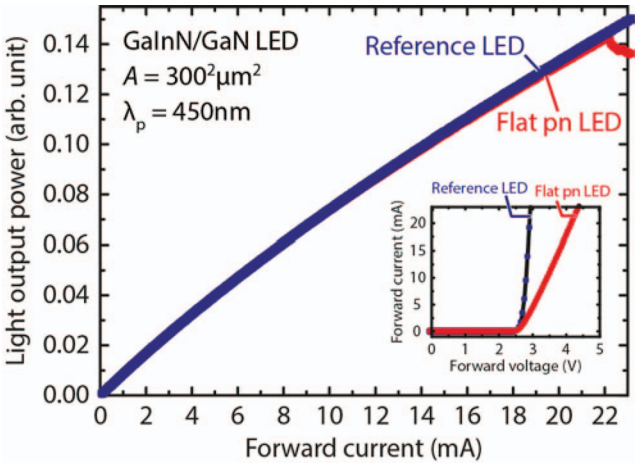

Figure 5. Light-output power–current–voltage (L–I–V) characteristics of the mesa-free flat pn-junction GaInN LED and the reference LED.

the turn-on voltages are almost the same, the series resistances are different. We believe that the higher operating voltage is caused by the increased bulk resistance of the type-converted n-type layer, considering the lowered electron mobility of the type-converted n-type layer. Although we get decent ohmic-contact properties on the type-converted region, the layer suffers from a higher resistance after ion-implantation thereby requiring further optimization of not only the ion-implantation processes but also of the post-implantation annealing conditions.

It is worthwhile to note benefits of the mesa-free flat pn-junction GaInN LED:

(1) This device structure eliminates the need for ICP-RIE from the LED chip fabrication procedure. The ICP-RIE process not only requires high vacuum and a toxic gas chemistry, but also suffers from low throughput, long process time, and irregularity of etching depth. Furthermore, exposed mesa sidewalls can be a cause of a surface leakage current which decreases the LED efficiency.[13]

(2) Unlike the conventional LED structure, which requires certain gap between (i) the mesa sidewall and (ii) the p-electrode as well as the n-electrode, the flat pn-junction structure can reduce the gap between the p-electrode and n-electrode thereby allowing for more chips to be fabricated on the same size wafer.

(3) A thin-film flip chip GaInN LED process combined with substrate removal by laser-lift off (LLO) is one of state-of-the-art technology of highly efficient LEDs. In the thin-film flip chip LED process, the wafer bonding process (used to bond the LED wafer to a carrier substrate) is a core process step. The flat surface of the mesa-free LED structure will contribute to a better bonding uniformity. In other words, no additional planarization step is required.

In summary, we present that Si-ion implantation can be used to convert an LED's p-type GaN to n-type GaN. The measured values of contact resistivity of the conductivity-type-converted layer are comparable to those obtained by conventional epitaxially grown n-type GaN. Consequently, this opens a way to make a mesa-free flat pn-junction LED which does not require the mesa dry etching process. The demonstrated flat pn-junction LED and the reference LED show comparable LOP performance showing that the LED fabrication process is highly promising.

Acknowledgments

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