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The beneficial effects of a p-type GaInN spacer layer on the efficiency of GaInN/GaN light-emitting diodes

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ABSTRACT

Light-emitting diodes (LEDs) with a Mg-doped p-type $Ga_{1-x}In_xN$ ($0 \leq x \leq 0.07$) spacer layer located between an undoped GaN spacer layer and the electron blocking layer are investigated. The LEDs are found to have comparable peak efficiency but less efficiency droop when the crystal quality of the p-type $Ga_{1-x}In_xN$ spacer layer is well-controlled by lowering the growth temperature and by using a suitable In composition and Mg doping concentration. All LED samples with the p-type spacer layer show a smaller efficiency droop compared to a reference LED having an undoped GaN spacer. Among the sample sets investigated, an optical power enhancement of 12% at 111 A/cm^2 is obtained when inserting a 5 nm-thick p-type $Ga_{0.97}In_{0.03}N$ spacer layer. The results support that carrier transport is the key factor in the efficiency droop observed in GaN-based LEDs.

1. Introduction

The efficiency droop, which is the decrease in efficiency occurring at high operating currents, is a major challenge that must be overcome for a variety of applications that utilize nitride-based light-emitting diodes (LEDs) [1–3]. Several studies have shown that low carrier-injection efficiency into the active region, induced by the strongly asymmetrical carrier transport, is a major contributor to this problem [4–6]. Better carrier injection, especially hole injection, increases the carrier concentration in the active region and reduces electron leakage out of the active region; thus, the efficiency becomes higher at high currents (i.e. a smaller efficiency droop). With this in mind, several approaches, including the design of novel electron-blocking layers (EBLs) and hole-injection layers [7–9] and attempts to improve the conductivity of p-type layers [10,11], have been proposed to reduce or alleviate the asymmetry in electron and hole transport.

In conventional nitride-based LEDs, the first-grown p-doped layer is the p-type AlGaN EBL. However, (i) the Mg solubility in AlGaN is not as good as it is in Ga(In)N and (ii) the Mg acceptor ionization energy in AlGaN is higher than in Ga(In)N (here, we will refer to $Ga_{1-x}In_xN$ with $0 \leq x \leq 0.07$ as Ga(In)N). These two points unavoidably lead to low hole concentrations and low p-type conductivity in AlGaN materials. Furthermore, the optimal growth temperature for p-type AlGaN for achieving a suitable hole concentration is usually higher than that for p-type Ga(In)N [12]. Note that the EBL is close to the active region (i.e. the last-grown quantum well), typically located only ~10 nm away. To spatially separate the multiple-quantum well (MQW) active region from the p-type AlGaN EBL, an undoped GaN spacer layer (usually 5–15 nm thick) is included. To avoid degrading the crystal quality of the MQW grown at low-temperatures (~800 °C for blue-emitting MQWs), the growth temperature of p-type AlGaN is chosen to be ~900 °C, well below its optimal value (~1100 °C). The lower-than-optimal growth temperature further deteriorates the conductivity of the p-type AlGaN EBL. This problem is even more severe for green LEDs which commonly exhibit a greater efficiency droop than blue LEDs [2].

In this work, in order to reduce the carrier asymmetry and so lessen the efficiency droop, we propose and demonstrate the inclusion of a p-type Ga(In)N spacer layer that partially replaces the

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conventional undoped GaN spacer. This structure that can be realized through a relatively simple process, provides a platform for the study of the effect of a higher hole concentration in the p-type layers on the efficiency droop without dramatic changes in the conventional LED structure. We show that the insertion of a p-type GaInN layer prior to the p-type AlGaN EBL can provide a way to maintain the LED efficiency at high currents by enhancing the hole injection efficiency (thereby also reducing electron overflow). However, optimizing the epitaxial-film properties in a metal-organic chemical vapor deposition (MOCVD) system for p-type Ga(In)N, its epitaxial growth requires the balancing of (i) better crystal quality achievable at higher growth temperature and (ii) efficient In incorporation achievable at lower growth temperature [11]. P-type Ga(In)N epitaxial layers with In compositions in the range of 0–7% (atomic percent) are grown for the present study. The LED structures include a systematic variation of the spacer layer's (i) growth temperature and (ii) Mg concentration, which is aimed at improving the hole injection efficiency of the LEDs. Atomic force microscopy (AFM), Hall effect measurements, light-output–current–voltage measurements by means of a parameter analyzer, and device modeling are conducted for optimizing the surface morphology, p-type conductivity, and device characteristics of the samples. As will be shown, this can further advance our understanding of the effects of the Ga(In)N spacer layer on device performance, when considered in comparison to LED structures having the conventional undoped GaN spacer layer.

2. Single layer analysis

As a preliminary study, we investigated the surface morphology of $Ga_xIn_{1-x}N$ single epitaxial layers (thickness 100 nm) with increasing In composition and Mg doping concentration. This was done to find general trends in the crystal quality and p-type conductivity of the layers. Two series AFM images revealing the epitaxial-film morphology of $Ga_xIn_{1-x}N$ single-layers having different In compositions and Mg doping concentrations are shown in Fig. 1. First, inspection of the images reveals that, at a fixed growth temperature, the hillock density increases with the In composition, as shown in Fig. 1(a)–(c). In general, the surface morphology of the GaN layer grown at 880 °C is better than that of the GaInN grown at 880 °C. A lower growth temperature allows the GaInN layer to have a higher In composition with a surface morphology that is comparable to that of GaN. The In incorporation in GaInN is only 2% at 880 °C but can be raised to 7% at a growth temperature of 830 °C. Therefore, the surface morphology of $Ga_{0.97}In_{0.03}N$ grown at 830 °C can be comparable to that of GaN grown at 880 °C. Second, at a fixed growth temperature (830 °C) and a fixed In composition (2%), the pinhole defect density increases with the Mg doping concentration, as shown in Fig. 1(d)–(f). This observation agrees well with the publication of Liliental-Weber et al. [13], which reported the influence of Mg dopants on defect formation in GaN. These pinhole defects, also known as V-defects, usually have {1011} sidewalls and are formed on the top of hillocks. Additionally, Mg dopants in Ga(In)N were reported to form several deep levels in GaN-based LEDs [14–16]. The deep levels, introduced by Mg-doping of the Ga(In)N spacer layer, can lead to a lower peak efficiency due to stronger Shockley-Read-Hall (SRH) recombination [17–19]. The same tendency is found in our samples; this will be discussed in further detail below in this article. Other than the deep-level defects, the polarization-mismatch-induced potential trap (i.e. a positive polarization sheet charge) at the interface between the Ga(In)N spacer and the AlGaN EBL exacerbates the non-radiative SRH recombination especially in the low current regime. This can also reduce the peak efficiency of LEDs when a p-type Ga(In)N spacer layer is used to increase the hole injection efficiency.

As for the p-type conductivity of the Ga(In)N layers, a Hall effect measurement system was used after a typical sample preparation process (i.e. surface cleaning by HCl:deionized (DI) water = 1:1 for 1 min, evaporation of Ni/Au (20/30 nm) for the contacts, and rapid thermal annealing at 550 °C in O_2 ambient for 1 min for ohmic contact formation). Fig. 2 shows the Hall carrier concentration and the resistivity as a function of the In mole fraction in the p-type Ga(In)N layers for a Mg/Ga molar precursor flow ratio of 0.8%. The p-type GaInN layers with 2 or 3% In have a higher Hall carrier concentration and lower resistivity compared to the p-type GaN layer. A Hall mobility of around 20 cm^2/Vs was obtained for all samples. It is noteworthy that the Hall carrier concentration is

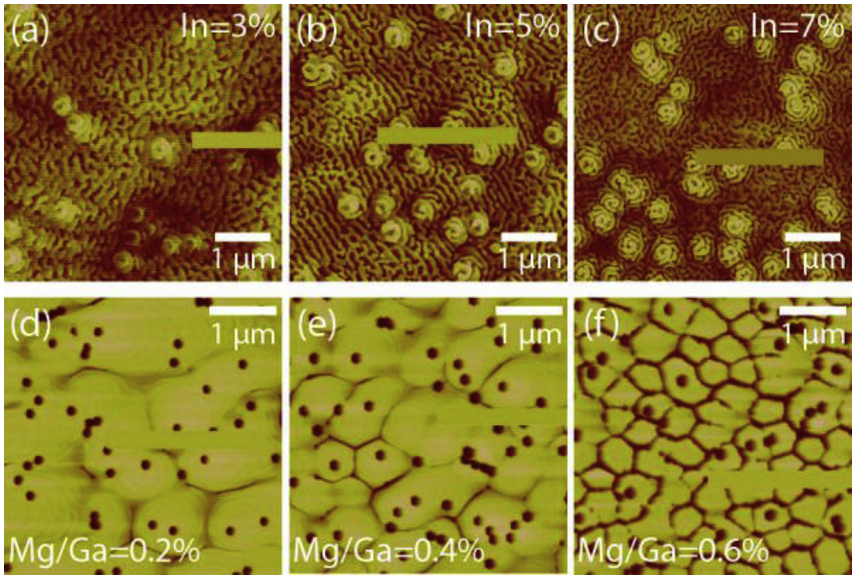

Fig. 1. (a–c) AFM images of GaInN surfaces showing the relation of hillock density and indium fraction at a fixed growth temperature. (d–f) AFM images of $Ga_{0.98}In_{0.02}N$ surfaces showing the relation of V-defect density and Mg/Ga molar precursor flow ratio at a fixed growth temperature.

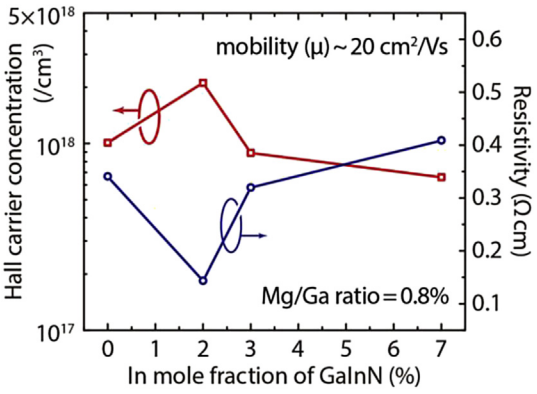

Fig. 2. Hall carrier concentration (i.e. hole concentration) and resistivity as a function of the In mole fraction in the Ga(In)N layers.

doubled in the $Ga_{0.98}In_{0.02}N$ layer ($p \sim 2.1 \times 10^{18}$ cm^{-3}) compared to the pure GaN layer ($p \sim 1.0 \times 10^{18}$ cm^{-3}), implying that the $Ga_{0.98}In_{0.02}N$ layer is suitable for use as the insertion layer between the MQW and EBL to increase the hole injection efficiency.

3. LED fabrication

The LEDs used in this study were grown by a multi-wafer MOCVD system on a c-plane sapphire substrate. First a low temperature GaN buffer layer was deposited, followed by a 2 μm thick unintentionally doped GaN layer. Next a 3 μm thick Si-doped n-type GaN layer was grown followed by an active region. After this, a p-type AlGaN electron blocking layer was grown followed by a p-type GaN capping layer. Mesas were fabricated under a standard LED fabrication process, followed by the depositions of n-type and p-type metal contacts. As for the active and EBL region, they include different Ga(In)N spacers with varying In compositions and Mg-doping levels. The active region of the LEDs consists of six pairs of 2.7 nm thick $Ga_{0.86}In_{0.14}N$ quantum wells and 13 nm thick GaN quantum barriers. To minimize the influence on the active region while growing the spacer layer, an undoped 8 nm thick GaN layer (as a low temperature spacer, LTS) was first grown on top of the last-grown quantum well at a growth temperature of 760 °C. The thickness of LTS was reduced from the conventional value of 13 nm to 8 nm to accommodate an additional 5 nm thick Ga(In)N high temperature spacer (HTS) that was epitaxially-deposited on the LTS; the HTS had different Mg doping concentrations and In compositions. Together, the undoped GaN LTS and the p-doped GaInN HTS form the Ga(In)N spacer layer. The schematic epitaxial structure and growth conditions of the designed HTS layer are shown in Fig. 3 and summarized in Table 1. Finally, as a reference sample, Sample A, with a single 13 nm thick undoped GaN spacer layer, was also prepared.

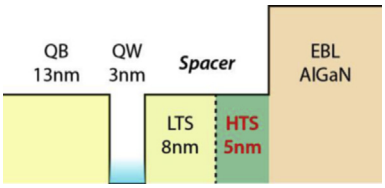

Fig. 3. The epitaxial structure of LEDs near the p-type Ga(In)N insertion spacer layer. The growth conditions of the LTS and HTS layers are summarized in Table 1.

Table 1
Summary of the growth conditions of the HTS spacer layer that is grown on top of the undoped GaN LTS spacer layer.

Sample ID	HTS material	Growth temp. (°C)	Mg/Ga ratio (%)
A	undoped GaN	880	0
B	p-type GaN	880	0.6
C	p-$Ga_{0.98}In_{0.02}N$	880	0.6
D	p-$Ga_{0.97}In_{0.03}N$	830	0.6

*LTS material: undoped GaN at 760 °C.

4. Results and discussion

Light-output–current–voltage (L–I–V) measurements were performed with a semiconductor parameter analyzer (Agilent 4155C) on the four LED sample sets (chip size: 300 × 300 μm^2): sample A, B, C, and D as shown in Table 1. At least five LED chips in each sample set were measured to confirm the uniformity of the LED wafer and to obtain representative efficiency-versus-current curves for each sample set. Besides the above-mentioned sample sets, we fabricated LEDs with a $Ga_{0.93}In_{0.07}N$ HTS to investigate the effect of a high In mole fraction (7%) in the spacer; however, none of the LEDs measured in this set did emit light, but showed diode characteristics with small turn-on voltages of ~1.5 V. The uniquely high indium composition (7%) is likely the cause of these problems. Strong lattice mismatch and thermal expansion mismatch between the $Ga_{0.93}In_{0.07}N$ spacer and the $Al_{0.15}Ga_{0.85}N$ EBL may degrade the interface quality. Moreover, the introduction of Mg (as a dopant) in the spacer can create additional dislocations; therefore, we suggest that a pre-mature turn-on, due to electrical punch-through via dislocations, was observed.

The measured efficiency-versus-current curves of the four different sample sets are plotted in Fig. 4. The reference (Sample A) has the highest peak efficiency. The peak efficiency ratios of samples A, B, C, and D, compared to the peak efficiency of Sample A, are 1, 0.84, 0.67, and 0.99, respectively. However, Sample A shows a 38.5% efficiency droop at 100 mA (current density of 111 A/cm^2). All the other sample sets, which possess the p-type Ga(In)N insertion spacer, have a smaller efficiency droop at the same current density. In particular, at a high current density, samples B and D have better efficiency performance than the reference Sample A. At 111 A/cm^2, the efficiency enhancement of samples B and D (compared to reference Sample A) are 3% and 12%, respectively. The efficiency

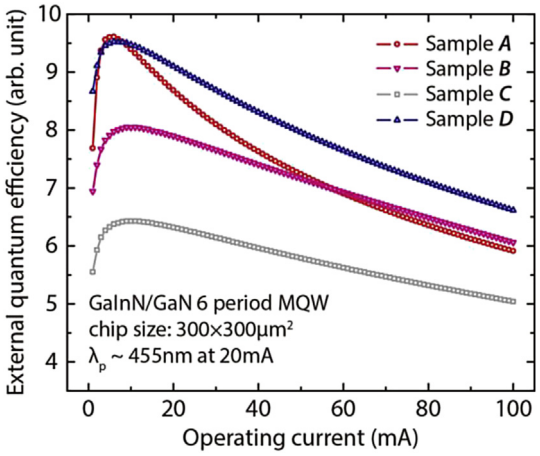

Fig. 4. Efficiency-versus-current curves for the LED samples with a p-type Ga(In)N spacer layer. A detailed description of the samples is given in Table 1.

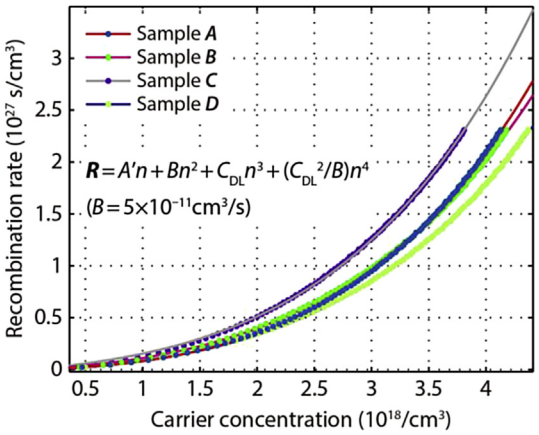

Fig. 5. Electron drift-leakage model fitting for the LEDs with a p-type Ga(In)N spacer.

enhancement at a higher current density (>111 A/cm^2) is without doubt expected to be even higher.

We use the electron drift-leakage model to further investigate the efficiency-loss mechanisms of each sample set [4,6]. By applying the analytic model in Ref. 6 to the experimentally-measured external quantum efficiency and current density, the recombination rate and carrier concentration can be calculated. The relation between the recombination rate and carrier concentration is fully explained by considering both the electron diffusion and drift leakage (note that for every hole not injected into the active region, an electron leaks out of the active region). The fitting results are organized in Fig. 5 and Table 2. From the fitting results, we find that the first-order non-radiative recombination of all p-type-doped spacer samples becomes larger presumably because of the introduction of Mg doping and In into the spacer layer. At the optimized growth temperature for undoped GaN (i.e. 880 °C), the SRH *A* coefficient of the reference set is 2.10 × 10^7 s^{-1} (Sample A). The *A* coefficient increases to 5.26 × 10^7 s^{-1} after the introduction of Mg (Sample B), and further increases to 9.18 × 10^7 s^{-1} when the In composition is raised (Sample C). This agrees with the above-discussed degradation of the AFM surface morphology of the p-type Ga(In)N surfaces (AFM was done on a separate set of single-layer samples in order to have access to the GaInN surface). By reducing the growth temperature to 830 °C, the crystal quality of p-type $Ga_{0.97}In_{0.03}N$ can be improved and the *A* coefficient is determined to be 5.21 × 10^7 s^{-1}, which indicates a crystal quality comparable to the p-type GaN grown at 880 °C (Sample D).

When compared to the reference set (Sample A), the third-order drift leakage coefficient C_{DL} is reduced in the samples with a p-type insertion spacer (Sample B and D), as expected, due to the higher hole concentration in the active region and a better carrier symmetry. However, the C_{DL} in Sample C is not smaller than that of the reference Sample A. The large first-order non-radiative recombination in Sample C could lead to large carrier leakage through some other leakage mechanisms (e.g. defect-assisted tunneling). Recall that the sample set with the highest In content of 7% showed the lowest crystal quality, resulting in a pre-mature turn-on voltage of 1.5 V (for blue LEDs, this value should be at least 2.7 V). This unusually low turn-on voltage could be due to the defect-assisted tunneling of carriers, without overcoming the p–n junction built-in potential [20,21].

Table 2
Fitting parameters extracted through the drift-leakage model of the LED samples with a p-type Ga(In)N spacer.

ID	IQE_P	*A* (1/s)	C_{DL} (cm^6/s)	GOF[a], R^2
A	60.0%	2.10 × 10^7	8.19 × 10^{-30}	0.9999
B	50.3%	5.26 × 10^7	7.33 × 10^{-30}	0.9997
C	40.1%	9.18 × 10^7	9.25 × 10^{-30}	0.9999
D	59.4%	5.21 × 10^7	6.72 × 10^{-30}	0.9998

[a] GOF: goodness of fit.

5. Conclusion

In summary, LEDs with a p-type Ga(In)N insertion spacer layer are shown to have comparable peak efficiency but a smaller efficiency droop if the crystal quality of the p-type GaInN insertion layer is well-controlled by lowering the growth temperature and by using a suitable In composition (3%) and Mg doping concentration. Every sample set with the p-type insertion spacer layer shows a smaller efficiency droop compared to a reference sample. Among the sample sets investigated, an optical-power enhancement of 12% at 111 A/cm^2 was obtained when inserting a 5 nm-thick p-type $Ga_{0.97}In_{0.03}N$ spacer layer. Some degradation of the crystal quality occurs when In is introduced into the spacer and when the spacer is doped with Mg; however, if the spacer is well-controlled by advanced epitaxy, a low efficiency droop is attained while maintaining a high peak efficiency.

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