Hybrid Integration of End-to-End Optical Interconnects on Printed Circuit Boards

Zhaoran Rena Huang, *Member, IEEE*, Daniel Guidotti, Lixi Wan, Yin-Jung Chang, *Student Member, IEEE*, Jianjun Yu, *Senior Member, IEEE*, Jin Liu, Hung-Fei Kuo, Gee-Kung Chang, *Fellow, IEEE*, Fuhan Liu, and Rao R. Tummala, *Fellow, IEEE*

***Abstract*—This paper discusses the integration of an end-to-end optical interconnect testbed on printed circuit boards using inexpensive off-the-shelf, bare die, optoelectronic components. We developed a process for efficient and simultaneous in-plane optical coupling between edge emitting laser and waveguides, and between photodetector and waveguide. We demonstrated an optically smooth buffer layer separating the printed circuit layer from the optical transport layer. The demonstrated radically new optical interconnect technology, which we refer to as interface optical coupling, is able to efficiently and simultaneously form optical interfaces between waveguides, lasers and photodetectors by photolithographic technique, thereby eliminating the need for micro-lenses and manual alignment. The measured laser to waveguide coupling efficiency is 45% and measured waveguide to photodetector coupling is 35%. The optical link is demonstrated to operate at 10 Gbps.**

***Index Terms*—Chip-to-chip, embedded devices, optical communication, optical integration, optical interconnect, polymer waveguide, printed circuit boards (PCBs), system-on-package (SOP).**

I. Introduction

As THE digital processor continues to scale down and the processing speed increases as predicted by Moore's law, the signal transport by electrical interconnection on printed circuit boards (PCBs) becomes a limiting factor for further improvement of a digital system due to its complexity in system layout, power consumption, electromagnetic interference, etc [1]. Optical interconnect is a promising solution in routing and distributing data at bit rate in multi-gigabits to above 10 Gpbs in distance less than ∼50 cm. In recent years, a number of chip-to-chip optical interconnect technologies have been demonstrated, including thin film device optoelectronics [2], embedded active and passive component integration [3], [4], hybrid packaging of electronic and optical component [5], [6], optical board technique [7], [8], etc.

Manuscript received October 16, 2006; revised April 28, 2007. This work was supported in part by the National Science Foundation Engineering Research Center, Georgia Institute of Technology under Grant EEC-9402723. This work was recommended for publication by Associate Editor F. Shi upon evaluation of the reviewers comments.

Z. R. Huang is with the Rensselaer Polytechnic Institute, Troy, NY 12180 USA (e-mail: zrhuang@ecse.rpi.edu).

D. Guidotti, Y.-J. Chang, J. Yu, J. Liu, and G.-K. Chang are with the Georgia Center for Advanced Telecommunications Technology, Georgia Institute of Technology, Atlanta, GA 30308-1019 USA.

L. Wan, H.-F. Kuo, F. Liu, and R. R. Tummala are with the Microsystems Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0560 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAPT.2007.901757

Fabrication of chip-to-chip optical interconnects by the industry at large, parallels the telecom industry practices of discrete component integration linking a waveguide to a photodetector or laser by means of micro-mirror and micro-lens relays that require substantial manual intervention in the optical alignment process. The active optical components, lasers, laser drivers, photodetectors and associated amplifiers are bonded to peripheral ball grid array (PBGA) packages. The PBGA package is then flip-chip bonded to the transceiver portion of the board [5]. Optical coupling to and from the passive lightwave network is accomplished by the use of mirrors and lenses. The results are high insertion loss, uncertain alignment stability and high production cost. The sketch in Fig. 1(a) represents the industry-wide approach, and articles representative of this integration strategy may be found in [5], [9], [10]–[12]. The board is depicted to contain an embedded, passive lightwave circuit which carries optical signals to and from PBGA packages that do not contain a processor. Because of the choice of vertical cavity surface emitting lasers (VCSELs) and vertically illuminated photodetectors (PDs), a 90°, out-of-plane beam turning element is required and is generally accomplished by using 45° micro mirrors and collimating lenses. One exception in this trend is the use of evanescently coupled thin metal-semiconductor-metal (MSM) photodetectors reported in [2], [11], [12]. A standard assembly process has been established in industry for utilizing mirrors and lenses to steer beam propagation direction. It usually has relaxed alignment tolerances due to the collimated beam between the lenses. However, the approach depicted in Fig. 1(a) has several drawbacks. It is difficult to fabricate 45° end mirrors by standard photolithography and these also suffer from sizeable insertion loss. Lenslet relays can be fabricated relatively easier but the relative alignment and insertion loss can be fairly large even neglecting board warping [9], [10], [13], [14]. Limited distance between lenses is another drawback in this approach. Alignment can be done actively and largely by hand with robotic assistance. However, solder wave reflow tends to negate precise alignment [13]. The use of peripheral ball grid array PBGA packages is another drawback for separately packaged optoelectronic (OE) chips and processors because it takes up substantial board space, which limits the number of inputs/ouputs (I/Os) and results in a separation of multiple centimeters away from the processors.

Viable economic realization of optical interconnect technology requires the development of radical packaging concepts that lead to affordable and reliable fabrication processes. A robust and affordable optical interconnect integration process will enable numerous architectural options at the board level and at the system level. In our group, we proposed an optical interconnect scheme that provides a much simpler fabrication

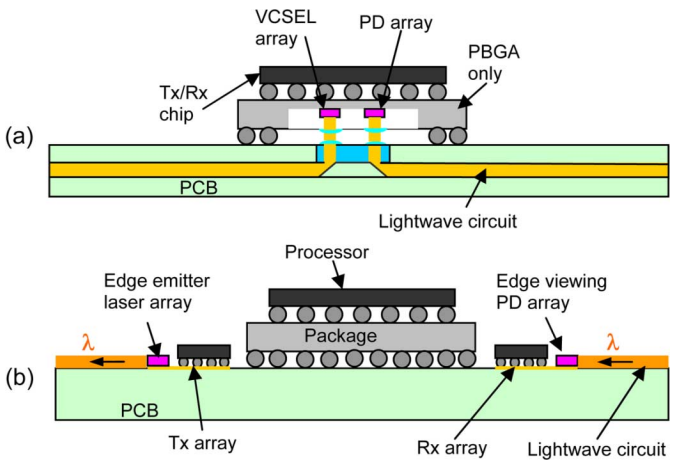


Fig. 1. (a) Conceptual sketch of the cross section of an electrical-optical circuit board being developed by a number of computer companies for the application of "fiber-to-the-processor." (b) Cross-sectional sketch of the results of IOC integration in which EELs and EVPDs are directly coupled to the lightwave circuit and in close proximity of the processor I/O pads.

process with greatly enhanced coupling, namely interface optical coupling (IOC), as shown in Fig. 1(b). The array of edge emitting lasers (EELs) and edge viewing PDs (EVPDs), launch and receive light in the plane of the passive lightwave circuit. The optical alignment is accomplished for one or multiple optical channels simultaneously in the step of photolithography during the waveguide core fabrication process, as described more fully below, without post-integration manual alignment. It ensures light is confined in the waveguide until it is detected.

As a first step toward the realization of viable high speed chip-to-chip optical interconnects, we have built a single channel testbed demonstrator: a fully integrated, 7 cm long optical link on an FR-4 board formed directly over printed circuit metallurgy. Both EEL and EVPD promote efficient butt-coupling to the lightwave circuit via a planar configuration with the optical waveguide. Suitable EVPDs do not exist at this time and are part of our current development activities, therefore, conventional PiN photodiodes are substituted in our demonstration, and a 45° end mirror is cut at the end of the waveguide over the PiN PD active area. It is important to note that the waveguide core is in direct contact and makes an interface with the PD active area. The optical link consists of a laser driver, an in-plane edge emitting laser diode, a polymer waveguide, a pin photodetector, an interface beam turning mirror at the end of the waveguide, a transimpedance amplifier (TIA), a limiting amplifier (L/A), an op-amp to control the laser driver bias current and modulation current and several passive surface mount components. A mesa area is defined by a smooth buffer layer on the FR4 board, on which waveguides are fabricated. The optical buffer layer effectively reduces scattering loss of the waveguide core. The testbed is sketched conceptually in Fig. 2.

II. Hybrid Integration of the Testbed

The single channel testbed demonstrator is designed to make use of off-the-shelf, bare die, 10 Gbps components to assess how well these perform when embedded into an optical data link on FR-4 and undergo board-type fabrication steps. The overall testbed consists of a laminated FR-4 substrate having

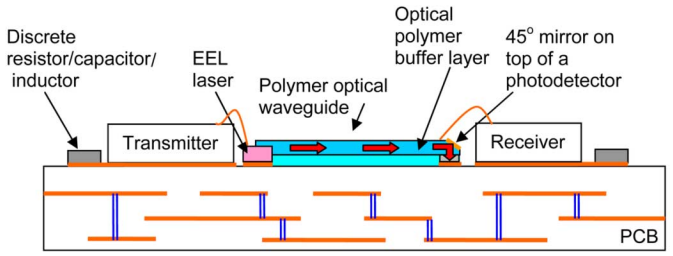


Fig. 2. Schematic of the testbed demonstrator by hybrid integration of optoelectronic devices and electronic chips on a PWB substrate.

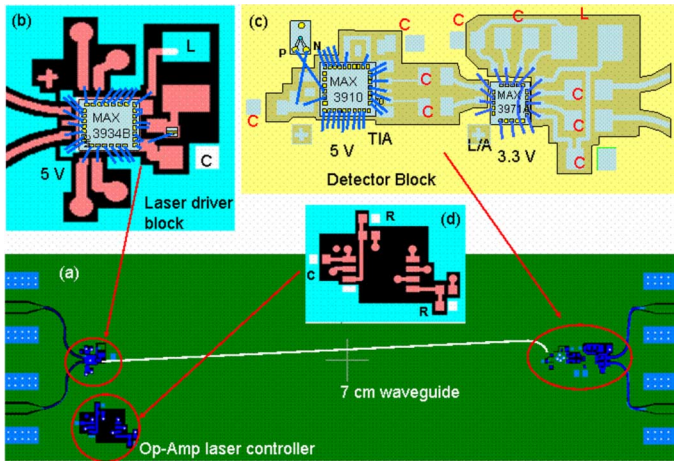


Fig. 3. Testbed layout. (a) Panoramic view of the test bed signal layer showing the coplanar microwave guides, SMA edge connector pads, the optical waveguide that optically connects the transmitter and receiver blocks. (b) Transmitter block. (c) Receiver block including a transimpedance amplifier and limiting amplifier. (d) Operational amplifier used to control laser bias and modulation current via two external voltage dividers.

four conducting copper layers. The layers are: signal (60 μm thick), ground (1 oz), power (1 oz) and ground (60 μm thick for board balance). The conducting layers are separated by three insulating FR-4 layer laminates without specific requirements, the first and last being 100 μm thick. Drill-through holes connect to the power planes to top wire bond pads, and the two ground planes are connected. High speed electrical I/Os to the board consist of SMA edge connectors rated for 17 Gbps and coplanar microwave guides connecting to the SMA connectors with the laser and detector blocks. An optical waveguide connects the laser with the detector, as shown in Fig. 3(a). The transmitter block, Fig. 3(b), consists of an edge emitting laser diode with emission at wavelength of $\lambda = 1310$ nm, and a laser driver and surface mounted capacitor and inductor. The detector block, Fig. 3(c), contains a PiN photodetector, a TIA, and a L/A. No filter or decision circuit is formed in the detection circuit. The laser dc bias and modulation amplitude are adjusted via a dual op-amp, Fig. 3(d), package and external variable voltage dividers. Surface mount capacitors and inductors are indicated as "C" and "L" in the figure. All active optoelectronic components are wire bondable and rated for 10.7 Gbps.

The fabrication sequence includes the following steps: 1) assembly of all surface mount electronic components including capacitors, inductors, all chips, laser diodes and photodetector, 2) wire bonding laser driver to laser and I/O pads, PD to TIA, TIA to L/A, and L/A to I/O pads, 3) form a thickness graded

polymer buffer layer, and 4) apply the lower cladding layer, the waveguide core layer, and the top cladding layer. The optical alignment from waveguide to laser diode and to PD is realized simultaneously by aligning the waveguide geometry on the photo-mask with the EEL emission region and with the PD active area. 5) After the waveguide core is developed and good alignment is confirmed, a 45° beam turning mirror is formed by cutting the core waveguide directly over the PD active area. 6) Finally, an Op-Amp used to control the ac and bias current to the laser via the laser driver is soldered into place, as are the I/O SMA edge connectors.

A. Integration of Laser Diode and Photodetector

Both the edge emitting laser diode (a laser from Emcore) and the photodetector (AXT, distributed by Lumei Optoelectronics), are rated as having a 3 dB cut-off frequency over 10 GHz. The laser emits at wavelength of 1310 nm and the PD has a marked responsivity of 0.9 A/W at this wavelength. The laser diode is fabricated on InP substrate with a die dimension of 254 μm $\times$ 250 μm $\times$ 100 μm. The die size of the PD is 250 μm $\times$ 460 μm $\times$ 150 μm. Manual pick-and-place was used to place the chips onto the designated metal bonding pads on board. The actual attachment was realized through high conductivity silver epoxy. The EEL has a bottom anode contact and a top cathode wire bonding pad. The photodetector is assembled in a similar fashion to the TIA input pads of the receiver circuit. The bonding pads for laser diodes and photodetectors are pre-defined on the assembly board through photolithography process. These bonding pads determine the position of the active devices in the optical link.

B. Formation of Optical Buffer Layer and Optical Waveguide

Optical alignment between the edge emitting laser and the top viewing photodetector requires vertical as well as in-plane alignment. The thickness of the edge emitting laser diode and PD dies are 100 μm and 150 μm, respectively. The difference in die thickness requires a slanted waveguide core layer to efficiently guide the optical wave from laser to the PD absorbing surface. In this work, we constructed a graded buffer layer to reduce the height inequality. Other approaches include polishing the photodetector back side, which is not electrically active, to a thickness of 90 μm, and placement of the PD in a 50 μm deep cavity in the FR-4 board.

Optical buffer layer is a technology we developed to address this issue. The fabrication of optical buffer layer is accomplished by using a solvent-free inorganic polymer glass (IPG) of proprietary composition, available from RPO Pty., Ltd., Acton, Australia. This material has a refractive index of $n = 1.52$ at wavelength of $\lambda = 632.8$ nm, which acts as negative tone in photolithography, and cross links only by the action of UV light. The waveguide fabrication sequence is as follows. The buffer layer is constructed after the assembly of laser diodes and photodetectors. IPG is applied to the designated open patch on the board at about 60 °C in order to obtain desired polymer viscosity. The board is tilted at an angle to allow the polymer viscosity to form the designed thickness gradient, at which the UV light (Mercury I-line) is turned on to cross link IPG thus freezing the buffer layer gradient into place in about 15 seconds at exposure of 9.8 mW/cm^2.

A lower cladding layer between 7 to 9 μm thick is next formed on top of the buffer layer by a conventional spin-coating process.

Fig. 4. Waveguide formation on (a) an edge emitting laser diode, (b) a pin photodetector, and (c) a pin photodetector with a 45° turning mirror.

The cladding polymer is an Epoxy Siloxane Oligomer (refractive index $n = 1.49$ at $\lambda = 632.8$ nm) from Polyset (Mechanicsville, NY). This polymer does contain a solvent and can be either thermally or optically cross-linked.

The waveguide core polymer has the same IPG material composition as the buffer layer and is formed to a typical thickness and width, each of 50 μm. The core waveguide is formed on a surface that typically lies 5 to 25 μm below the laser ridge waveguide, and within 5 μm of the PD surface. The heights are measured with a surface profiler (DEKTAK 3030). The waveguide core is cross linked by the use of a negative tone mask. The mask alignment for waveguide core definition was achieved by using two confocal microscopes: one is used to monitor the waveguide/laser diode interface and the other one is used to monitor the waveguide/photodetector interface. When the alignment appears satisfactory, the exposure chamber of the mask alignment is continuously flushed with Nitrogen and the UV is turned on. Thus, we formed the waveguide link between the laser diode and the PD. The unexposed waveguide materials are then washed away during the development cycle.

Finally, the top cladding layer (same as the bottom cladding polymer) is spun on, soft baked, and cross linked by UV light. Fig. 4(a) and (b) show the photos of waveguide integrated with a laser diode and a PD, respectively.

In addition to serving as a platform for thickness graded transitions, the buffer layer also provides an interface from FR-4 roughness to nano-scale smoothness optical waveguide substrate. It reduces the strain between FR4 board and the polymer optical waveguide.

C. Formation of 45° Turning Mirror

One end of the optical waveguide is defined along the cavity stripe of the edge emitting diode and the other end of the optical waveguide covers the active region of the PiN photodiode. The optical signal from the edge emitting laser diode is directly butt-coupled into the waveguide. Numerical simulation and measured laser to waveguide coupling efficiency will be discussed in next section. It is optional to remove the polymer stripe that covers the laser cavity to get a clean surface.

We defined a 45° beam steering mirror on top of the active PiN PD to couple light from the waveguide to the PD, as shown in Fig. 3(c). After the alignment of the waveguide core is confirmed with both the laser diode and the PD by microscope inspection, we perform a 45° cut on the PD active region (36 μm in diameter) using a scalpel blade. The blade is mounted on a linear stage with a 45° angle and manipulated into position by an XYZ stage.

D. Assembly of the Transmitter and Receiver

The single channel testbed is assembled on a 1×2 in FR4 board. The transmitter block consists of a DFB laser diode, and

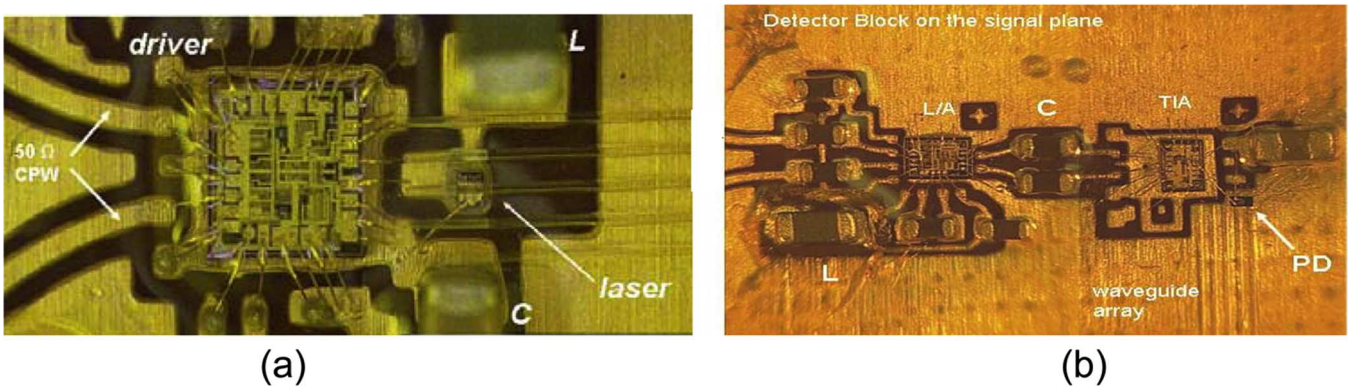


Fig. 5. Assembled (a) transmitter block and (b) a receiver block on FR4 board.

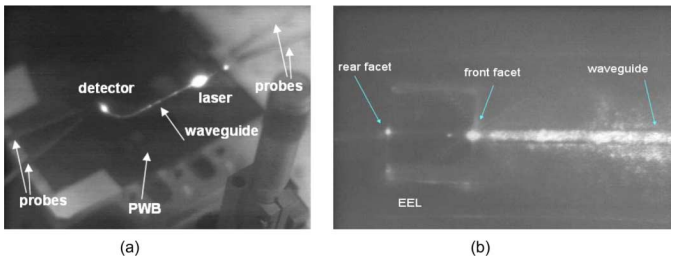


Fig. 6. (a) An infrared photo of a laser-waveguide-PD link on a FR4 board for dc coupling measurement. (b) Laser emission coupled to polymer waveguide.

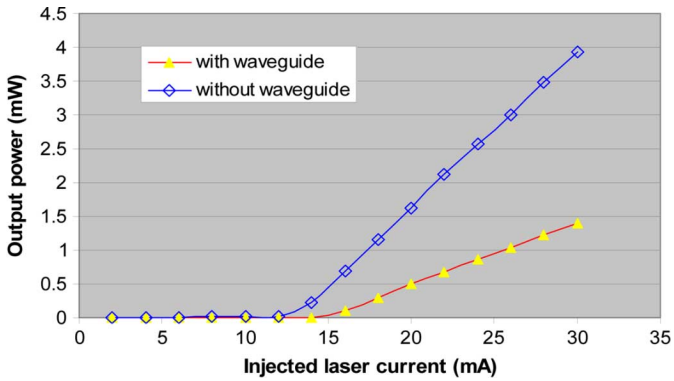


Fig. 7. Measured optical power with waveguide and without waveguide as a function of laser bias current.

a laser driver (MAX3934 with dimension of 1.6 mm × 1.6 mm) and a surface mounted capacitor and a ferrite bead inductor as filter and ballast. The laser dc bias and modulation is adjusted via a dual op-amp package (MAX4282). All chips are unpackaged bare dies, rated at 10.7 Gbps and fixed in place with conducting silver epoxy and are wire bonded to appropriate pads on the signal layer. The top view (8 mm × 3.5 mm) of the assembled transmitter block is shown in Fig. 5(a). The receiver block contains a PiN PD, a TIA (MAX3910 or MAX3970), and a L/A (MAX3971) for fixed output pulse amplitude. All chips are wire bonded, and the critical wire bond lengths are 0.6 to 0.7 mm long. The transmitter and receiver are connected via a 7 cm long polymer waveguide with a typical core dimension of 50 μm × 50 μm. The waveguide have 1 cm radius of curvature at the receiver side to prevent stray light from entering the PD.

III. Modeling and Measurement of Coupling Efficiencies

Power transmission efficiency is a big part of this research. The coupling efficiencies between laser and waveguide and between waveguide and PD via a 45° end mirror over the PD active area were measured under dc operation. In order to assess the coupling efficiencies, we assembled a reference testing board using components from the same batch as those in the complete end-to-end link. The reference board consists of an edge emitting laser diode, a curved waveguide and a pin photodetector. An infrared photo, shown in Fig. 6(a), is taken when the waveguide is light up by the laser diode with emission at $\lambda = 1.3$ μm. A close look of the edge emitting laser diode and the optical waveguide connection area is shown in Fig. 6(b).

A. Measurement of Laser to Waveguide Coupling

The coupling efficiencies between the edge emitting laser and polymer waveguide were measured under dc operation in two steps. 1) The total dc output power from an EEL is directly collected by a Ge PD with large aperture (0.5 mm × 0.5 mm) placed immediately in front of the laser. 2) We measure the output power from the waveguide that is end-coupled with the EEL laser diode. The detected optical power with and without coupling to waveguide as functions of laser bias current is plotted in Fig. 7. The polymer waveguide is 4.6 cm long and has a loss coefficient of 0.24 dB/cm which were determined previously. The power transmission, η (dB), between the edge emitting laser diode and waveguide, neglecting reflection losses, is given by

$$\eta = \frac{P_{\text{out}}}{P_{\text{laser}}} + \frac{\alpha L}{P_{\text{laser}}} \tag{1}$$

where P_{laser} is the bare die laser output power, P_{out} is the waveguide output power, and α is the total waveguide insertion loss in dB/cm that includes the intrinsic (absorption losses) and extrinsic (fabrication defects) losses. The measured waveguide output P_{out} is -4.6 dB and the total waveguide loss over the 4.6 cm long waveguide segment αL is 1.1 dB, giving the EEL laser to waveguide coupling efficiency of -3.5 dB or 45%.

B. Modeling of Laser to Waveguide Coupling Efficiency

The edge emitting laser is modeled as a 5 μm long, passive, single mode semiconductor waveguide with a thickness of 2.37 μm on InP substrate. The photon confinement layers,

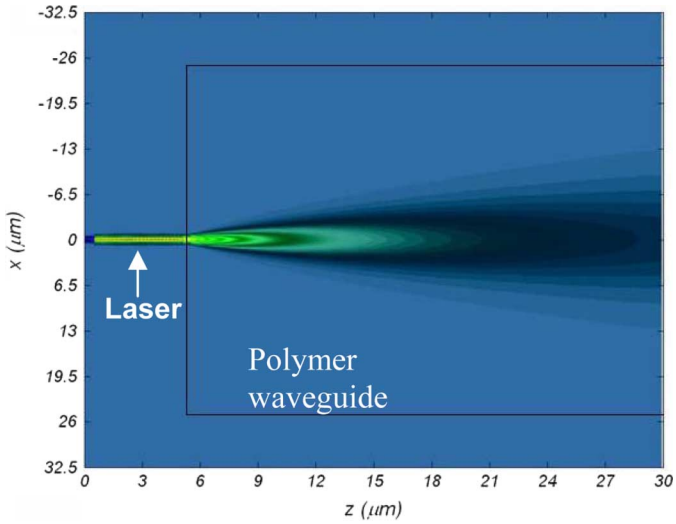


Fig. 8. Two-dimensional plot of S_z propagating across the interface between a single mode semiconductor laser waveguide cavity and a multimode polymer waveguide.

InP ($n = 3.22$) of 1 μm thick and InGaAsP ($n = 3.33$) of 0.15 μm thick, are symmetrically grown in both side of the multiple quantum well (MQW) layers. The MQW has a thickness of 0.07 μm with an average refractive index of 3.4025. The operational wavelength is taken to be 1310 nm and the fundamental waveguide mode was chosen as the field excitation.

The polymer waveguide core is modeled as having a thickness of 50 μm ($n = 1.52$) with a 10 μm-thick under cladding ($n = 1.49$) and no top cladding. The coupling efficiency between the two has been simulated for the case when both are immersed in a medium (i.e., air) with index of refraction of $n = 1.0$. The simulation was performed by finite difference time domain (FDTD) analysis and the mesh size is set at 0.03 μm in both of the x and z direction, which is around 1/44 of the operating wavelength. The coupling efficiency is obtained by determining the magnitude of the power density in the propagation direction that passes through a plane at $z = 30$ μm in the polymer waveguide as a fraction of the input power density set for the field excitation in the semiconductor laser waveguide cavity. A 2-D plot of Poynting vector S_z in z direction is shown in Fig. 8.

A coupling efficiency of 78% is obtained from the numerical simulation assuming no material loss of the waveguide. The optical power loss primarily arises from refractive index discontinuity at the interface and the mode mismatch between the laser cavity and the waveguide cavity. The optical wave reflected back from the waveguide facet may disturb stationary modes of the laser cavity. This is equivalent to lowering the reflectivity of the laser output facet. In our simulation, the EEL is modeled as a passive waveguide, which means we neglect the dynamics of the laser emission. This may cause overestimate the coupling efficiency. The oversimplified simulation presented here is meant to show consistency in the presence of numerous extraneous effects that are not easily characterized by the simulation and to predict the trend when parameters at the interface are adjusted. Simulation shows that the coupling efficiency can be improved by inserting a layer with intermediate refractive index ($n = 1.52$) between the laser facet and the optical waveguide.

C. Measurement of PD Coupling

The waveguide to PD coupling efficiency with turning mirrors is measured using an optical source with known emission characteristics. The responsivity of the PD is 0.9 A/W at $\lambda = 1310$ nm and the ratio of the photodetector active area to the ideal beam size steered by the mirror is 0.72. From the measured PD current, we deduce the coupling efficiency to be 35%, which excludes the insertion loss from the end mirror operating in total internal reflection without gold coating, scattering loss due to the rough surface of the end mirror, and waveguide bending loss and material scattering loss.

D. Modeling of PD Coupling With Turning Mirror

To estimate the coupling efficiency from the multimode polymer waveguide to the PD via a 45°, total internal reflection end mirror, we have simulated the waveguide-PD interface using FDTD method. The mirror is formed by the hypotenuse of an equilateral right triangle on a polymer waveguide having $n = 1.52$ and cross section of 50 μm $\times$ 50 μm. The boundary medium is assumed to be air. An ideal surface without metal coating is assumed. A PD having an active area of 36 μm in diameter is placed underneath the center of the mirror projection on the horizontal plane. The PD is represented by a medium with $n = 3.52$. We assumed no anti-reflection coating applied to the PD surface and the waveguide is taken as lossless. The modal index of the TE_0 mode is thus found to be $N_0 = 1.51582211$. The FDTD simulation indicates a coupling efficiency of 60.6% obtained by normalizing the power density across the PD detection area to the input power density of the TE_0 mode. The Poynting vector, in the x-direction (S_x) for the TE_0 mode reflected by a 45° mirror is simulated by a 2-D FDTD method and is shown in Fig. 9(a). The power loss for fundamental mode of the waveguide is primarily caused by surface reflection of the PD and limited PD responsivity.

Since the waveguide supports multimode propagation, it is important to exanimate beam turning via the 45° mirror for optical wave at higher order modes. Fig. 9(b) plots the simulated Poynting vector of a TE_{10} mode input ($N_{10} = 1.50644664$) in x direction. The observation line is placed at a distance of 2 μm away from the waveguide-PD interface. A large amount of power has penetrated through the mirror surface. The FDTD simulation gives a coupling efficiency of 28.3 %, which is close to our measured data of 35%. Nevertheless, the simulation reveals a 34.9 % of power has passed through the mirror, giving rise to another source of power loss via turning mirror coupling for optical wave at high orders in addition to reflection loss at the PD surface. Through simulation investigation, it is clear that we can improve the waveguide to PD coupling by reducing the dimension of the waveguide to achieve single mode (fundamental mode only) operation or coating the mirror with an Au layer to enhance optical wave confinement by the mirror or a combination of both approaches.

IV. AC Performance of the Testbed

We first measured the ac response of the transmitter block and receiver block individually, and then compared the eye diagrams with that of the end-to-end optical link. The characteristic optical output of the transmitter block is displayed in Fig. 10(a). The optical output of the laser is collected with a lensed, pigtail, single mode optical fiber. The optical eye opening diagram at

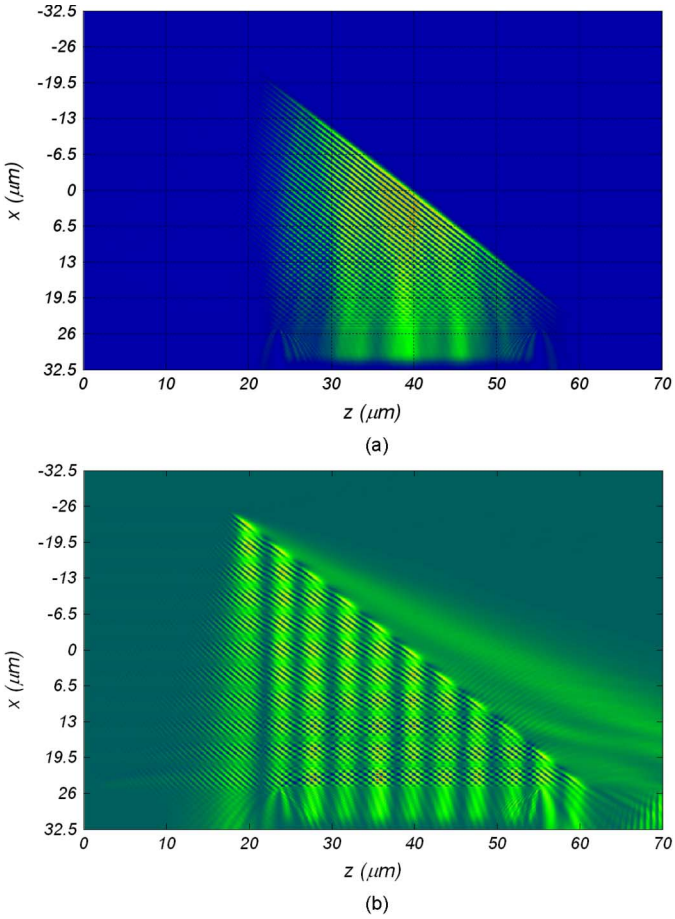


Fig. 9. Optical wave is turned via a 45° mirror. (a) x-directed Poynting vector (S_x) plot of TE_0 mode at the turning mirror, (b) x-directed S_x of Poynting vector of TE_{10} mode.

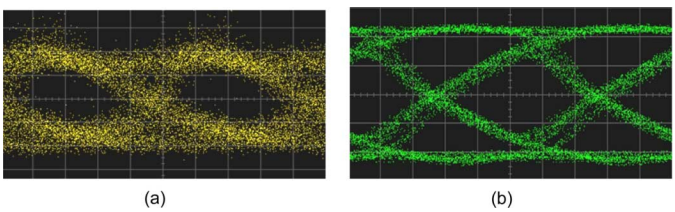


Fig. 10. (a) Single ended optical eye opening diagram at 10 Gbps of the transmitter block. (b) The single ended electrical eye opening diagram of the receiver block. The time scale is 20 ps/division.

10 Gbps is obtained with a digital analyzer (HP 83480A) for the case of a single ended electrical bit stream signal into the laser driver. The coupling from laser diode to fiber is low because of the difficulty of alignment as well as the reflection from the fiber back to laser diode. The characteristic electrical response of the receiver block, including the limiting amplifier, is displayed in Fig. 10(b). The optical signal originates from a precision fiber optic source (ILX Lightwave 7900B) and is impingent on the PD via a lensed, pigtail, single mode optical fiber. The single ended electrical output from the limiting amplifier is used to generate the eye diagram and is consistent with manufacturer specifications for the stand-alone TIA (MAX3970). The timing jitter is most likely due to the coplanar microwave guide design which was separately tested by an S-parameter analyzer and found to significantly diverge from 50 Ω above 7 GHz.

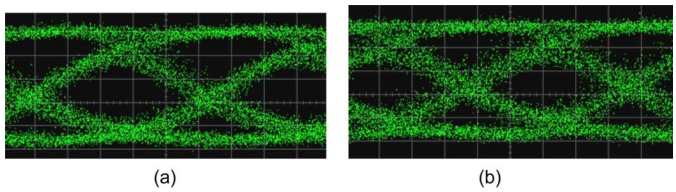


Fig. 11. Limiting amplifier output from the complete optical link tested at date rate of (a) 9 Gbps and (b) 10 Gbps. The time scale is 20 ps/division.

The combined the electrical responses of the end-to-end on board transmitter-waveguide-receiver link at 9 Gbps and 10 Gbps are shown in Fig. 11(a) and (b), respectively. Pseudo random electrical bits are introduced at one end of the board over an SMA edge connector to a single ended coplanar waveguide and to the laser driver block, transported optically across the board over an integrated optical waveguide to a PiN photodetector and recovered, without a decision circuit, as electrical bits at the other end of the board over a single ended CPW and output SMA connector. The data stream is analyzed by a digital communication analyzer. The measured eye diagram of the end-to-end optical link has lower noise and less jitter than that of transmitter block, attributing to free of alignment issues in the end-to-end optical link. The eye-diagram of the end-to-end optical link is worse than that of the receiver block due to power coupling losses at various stages.

V. Conclusion

We have demonstrated a novel, simple process that is free from manual alignment tuning to build a complete end-to-end optoelectronic signaling system at a data rate of 10 Gbps. The optical link, consisting of a transmitter block, optical waveguide, and receiver block, is integrated on a common FR-4 board packaged using bare die components. In our process, there is only one micro mirror and no lenses needed to steer or collimate the optical beams. The coupling efficiencies from edge emitting laser to waveguide and waveguide to PD via a 45° mirror are measured as 45% and 35%, respectively. Simulation of coupling efficiency by FDTD has indicated that the power loss at laser to waveguide interface is mainly due to reflection at the waveguide facet and mode mismatch between the laser cavity and the waveguide. It is shown by theoretical investigation that optical wave with high order mode can not be steered efficiently by the 45° turning mirror via total internal reflection. A metal coated waveguide facet is needed to improve waveguide to PD coupling.

Acknowledgment

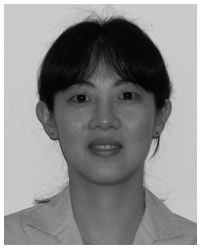
The authors would like to thank S. Halper, Georgia Tech Research Institute, and L. Rose, Georgia Tech Microelectronics Research Center, for their patient and expert wire bonding (without their persistence this work could not have been completed).

References

[1] D. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, no. 6, pp. 728–749, Jun. 2000.

[2] S.-Y. Cho, S.-W. Seo, N. M. Jokerst, and M. A. Brooke, "Board-level optical interconnection and signal distribution using embedded thin-film optoelectronic devices," *J. Lightw. Technol.*, vol. 22, pp. 2111–2118, 2004.

[3] C. Choi, L. Lin, Y. Liu, J. Choi, L. Wang, D. Haas, J. Magera, and R. T. Chen, "Flexible optical waveguide film fabrications and optoelectronic devices integration for fully embedded board-level optical interconnects," *J. Lightw. Technol.*, vol. 22, pp. 2168–2176, 2004.
[4] M. H. Cho, S. H. Hwang, H. S. Cho, and H.-H. Park, "High-coupling efficiency optical interconnection using a 90°—bend fiber array connector in optical printed circuit boards," *IEEE Photon. Technol. Lett.*, vol. 17, no. 3, pp. 69–692, Mar. 2005.
[5] D. Kuchta, Y. Kwark, C. Schuster, C. Baks, C. Haymes, J. Schaub, P. Pepeljugoski, L. Shan, R. John, D. Kucharski, D. Rogers, M. Ritter, J. Jewell, L. Graham, K. Schrödinger, A. Schild, and H. Rein, "120-Gb/s VCSEL-based parallel-optical interconnect and custom 120-Gb/s testing station," *J. Lightw. Technol.*, vol. 22, no. 9, pp. 2200–2212, 2004.
[6] M. Franke and F. P. Schiefelbein, "Optical interconnects on printed circuit board level-results based on German funded project OPTICON," in *Proc. Electron. Comp. Technol. Conf.*, 2004, pp. 1542–1546.
[7] B. S. Rho, S. Kang, H.-S. Cho, H.-H. Park, S.-W. Ha, and B.-H. (Tiger)Rhee, "PCB-compatible optical interconnection using 45 - ended connection rods and via-holed waveguides," *J. Lightw. Technol.*, vol. 22, pp. 2128–2134, 2004.
[8] K. B. Yoon, I.-K. Cho, S. H. Ahn, M. Y. Jeong, D. J. Lee, Y. U. Heo, B. S. Rho, H.-H. Park, and B.-H. (Tiger) Rhee, "Optical backplane system using waveguide-embedded PCBs and optical slots," *J. Lightw. Technol.*, vol. 22, pp. 2119–2127, 2004.
[9] D. Krabe, F. Ebling, N. Arndt-Staufenbiel, G. Lang, and W. Scheel, "New technology for electrical/optical systems on module and board level: The EOCB approach," in *Proc. 50th Electron. Comp. Technol. Conf.*, 2000, p. 970.
[10] Y. Ishii, S. Koike, Y. Arai, and Y. Ando, "SMT-compatible large-tolerance 'OptoBump' interface for interchip optical interconnections," *IEEE Tran. Adv. Packag.*, vol. 26, no. 1, p. 22, Feb. 2003.
[11] Z. Huang, Y. Ueno, K. Kaneko, N. M. Jokerst, and S. Tanahashi, "Embedded optical interconnections using thin film InGaAs metal-semiconductor-metal photodetector," *Electron. Lett.*, vol. 38, pp. 1708–1709, 2002.
[12] E. N. Glytsis, N. M. Jokerst, R. A. Villalaz, S.-Y. Cho, S.-D. Wu, Z. Huang, M. A. Brooke, and T. K. Gaylord, "Substrate-embedded and flip-chip-bonded photodetector polymer-based optical interconnects: Analysis, design, and performance," *J. Lightw. Technol.*, vol. 21, pp. 2382–2394, 2003.
[13] J. A. Kash, F. E. Doany, L. Schares, C. L. Schow, C. Schuster, D. M. Kuchta, P. K. Pepeljugoski, J. M. Trewhella, C. W. Baks, R. A. John, J. L. Shan, Y. H. Kwark, R. A. Budd, P. Chiniwalla, F. R. Libsch, J. Rosner, C. K. Tsang, C. S. Patel, J. D. Schaub, D. Kucharski, G. Guckenberger, D. S. Hegde, H. Nyikal, R. Dangel, F. Horst, B. J. Offrein, C. K. Lin, A. Tandon, G. R. Trott, M. Nystrom, D. Bour, M. R. T. Tan, and D. W. Dolfi, "Terabus: A chip-to-chip parallel optical interconnect," in *Proc. Opt. Fiber Commun. Conf. Nat. Fiber Opt. Eng. Conf.*, Anaheim, CA, 2006, p. 10.
[14] H.-S. Cho, K.-M. Chu, S.-Y. Kang, S.-H. Hwang, B.-S. Rho, W.-H. Kim, J.-S. Kim, J.-J. Kim, and H.-H. Park, "Compact packaging of optical and electronic components for on-board optical interconnects," *IEEE Trans. Adv. Packag.*, vol. 28, no. 1, p. 114, Feb. 2005.



Zhaoran Rena Huang (M'98) received the B.Sc. degree from the Beijing Institute of Technology, Beijing, China, in 1995, and the M.Sc. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, in 1999 and 2003, respectively.

She is now an Assistant Professor with Rensselaer Polytechnic Institute, Troy, NY. Her current research interests include RF/opto devices integration and packaging, and nano device characteristics.

Daniel Guidotti received the B.A. degree in physics and mathematics from the University of California at Berkeley in 1968 and the M.A. and Ph.D. degrees in physics from the University of Chicago, Chicago, IL, in 1970 and 1976, respectively. His thesis dealt with surface plasma wave dispersion in liquid Mercury in an effort to understand the intricate and still elusive electronic structure at that surface.

He is a Senior Research Scientist in the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta. Before joining Georgia Tech in 2002, he was with the IBM, T.J. Watson Research Center, Troy, NY, where he contributed to the development of numerous technologies. Prior to joining IBM in 1983, he made numerous discoveries as a Post-Doctoral Fellow: forbidden optical second harmonic generation from centro-symmetric semiconductors, coherent antistokes raman scattering from electronically excited states in benzene, raman scattering from strain confined electron-hole liquid in silicon, and electronically driven 1-D structural phase transitions in organic semiconductor polymers. He has authored over 50 archival articles in physics, chemistry and engineering, and has eight issued patents. His research focus is in optodigital system design and integration.

Dr. Guidotti received the IBM Outstanding Technical Achievement Award and the Industry Best R&D 100 Award.

Lixi Wan received the Ph.D. degree in electrical engineering from the Beijing University of Posts and Telecommunications, Beijing, China, in 1992.

He was a Postdoctoral Research Fellow at Tsinghua University, Beijing, from 1992 to 1994, and an Associate Professor at the Beijing University of Posts and Telecommunications, from 1994 to 1998. He joined the Electromagnetic Researching Center, University of Illinois at Champaign-Urbana, as a Visiting Associate Professor from 1998 to 2000. He is currently with the Microsystems Packaging Research Center, Georgia Tech, as a Senior Research Engineer. He has published over 70 archival articles in electromagnetic engineering, has two patents. His research interest areas are microwave technology, antenna, computation of electromagnetics, mixed signal system design, simulation, and testing.

Dr. Wan received eight awards for his technical papers.

Yin-Jung Chang (S'04) received the B.S. degree in electrical engineering from Tatung University, Taipei, Taiwan, R.O.C., in 1996, the the M.S. degree in communication engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1998, and is currently pursuing the Ph.D. degree in the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta.

His current research interests are guided-wave optical interconnects for optical/digital two-function integrations.

Jianjun Yu (M'03–SM'04) received the B.S. degree in optics from Xiangtan University, Xiangtan, China, in 1990 and the M.E. and Ph.D. degrees in optical communications from the Beijing University of Posts and Telecommunications, Beijing, China, in 1996 and 1999, respectively.

From June 1999 to January 2001, he worked at the Research Center COM, Technical University of Denmark, Lyngby, as an Assistant Research Professor. From February 2001 to December 2002, he worked for Lucent Technologies and Agere Systems, Hoboken, NJ, as a Member of Technical Staff. He joined the Georgia Institute of Technology (Georgia Tech), Atlanta, in January 2003, where he was a Research Engineer II and served as the Director of the Optical Network Laboratory. He is currently a Member of Technical Staff with NEC Laboratories, Princeton, NJ. He is also an Adjunct Professor with Georgia Tech and the Beijing University of Posts and Telecommunications. He is the holder of two U.S. patents with five others pending. He has authored more than 90 publications in prestigious journals and conferences. He is a Reviewer for the *Journal of Lightwave Technology*, *Optics Express*, *Optics Letters*, *Optical Engineering*, and *Optics Communications*. His current research interests include new modulation-format techniques, radio-over-fiber systems and networks, wavelength-division-multiplexing passive optical network, radio over fiber, and optical-label switching in optical networks.

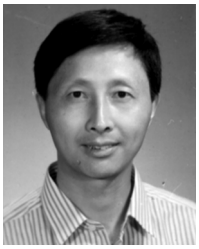
Dr. Yu is a Member of the IEEE Lasers and Electro-Optics Society (LEOS). He serves as a Technical Committee Member of the IEEE LEOS 2005–2007 Annual Meeting, as well as a Reviewer of the IEEE PHOTONICS TECHNOLOGY LETTERS. He is a Guest Editor for a special issue "Convergence of optical and wireless networks" for the IEEE/OSA *Journal of Lightwave Technology*.

Jin Liu, photograph and biography not available at the time of publication.

Hung-Fei Kuo, photograph and biography not available at the time of publication.

Gee-Kung Chang (M'80–SM'92–F'05) received the B.S. degree in physics from National Tsinghua University, Hsinchu, Taiwan, R.O.C., in 1969 and the Ph.D. degree in physics from the University of California, Riverside, in 1976.

He is the Byers Eminent Scholar Chair Professor and Georgia Research Alliance Eminent Scholar in Optical Networking in the School of Electrical and Computer Engineering, Georgia Institute of Technology (Georgia Tech), Atlanta. He spent two years carrying out postdoctoral research in high energy electron/photon physics at Rutgers University, Piscataway, NJ and Cornell University, Ithaca, NY. He spent the next 23 years within the Bell Systems in New Jersey-Bell Labs, Bellcore, and Telcordia Technologies where he served in various capacities including Director of the Optical Networking Systems and Testbed, Director of the Optical System Integration and Network Interoperability, and finally, Executive Director and Chief Scientist of the Optical Internet Research Group. Prior to joining Georgia Tech, he served as Vice President and Chief Technology Strategist of OpNext, Inc., in charge of technology planning and product strategy for advanced optical networking devices and components. He has been granted 35 patents in the area of optoelectronic devices, high speed integrated circuits, telecommunication switching components and systems, WDM optical networking elements and systems, multiwavelength optical networks, optical network security, and optical label switching routers. He has co-authored over 140 journal and conference papers.



Fuhan Liu received the Ph.D. degree from Fudan University, Shanghai, China, in 1965.

He is a Research Engineer at the NSF-Packaging Research Center, Georgia Institute of Technology, Atlanta. Prior to coming to the U.S., in 1997, he was an Associate Professor in the Department of Material Science and Deputy Director of High Density Electronic Packaging Laboratory, Fudan University. He had been a Visiting Scholar at Brandeis University (1987–1988), Wayne State University (1997–1998), and the International Microelectronics And Packaging Society (IMAPS, 1997). Currently, he focuses on the R & D of fabrication and integration of high density wiring and optoelectronics for systems on package, material evaluation, processes development, and testing.

Dr. Liu received the Global Collaboration Award for his outstanding Contributions to the NSF Programs, numerous national outstanding awards from China, the Memorable Paper of the *American Journal of Physics* in 1993, and is listed in the AJP All-Star Team.

Rao R. Tummala (F'94) received the B.E. degree in metallurgical engineering from the Indian Institute of Science, Bangalore, and the M.S. degree in metallurgical engineering and the Ph.D. degree in materials science and engineering from the University of Illinois, Chicago, in 1969.

He is a Distinguished and Endowed Chair Professor, and Director of NSF ERC, Georgia Institute of Technology (Georgia Tech) Atlanta, pioneering system-on-package (SOP) vision. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering such major technologies as the first flat panel display based on gas discharge , the first and next three generations of multichip packaging based on 35- layer alumina and 61-layer LTCC with copper and copper-polymer thin film, and materials for ink-jet printing and magnetic storage. He published 375 technical papers and holds 71 patents and inventions. He authored the first modern packaging reference book *Microelectronics Packaging Handbook* (New York: Van Nostrand, 1988) and the first textbook *Fundamentals of Microsystems Packaging* (New York: McGraw Hill, 2001).

Dr. Tummala received numerous awards including Industry Week's Award for Improving U.S. Competitiveness, IEEE 's David Sarnoff and Major Education awards, Dan Hughes Award from IMAPS, the Engineering Materials Achievement Award from DVM and ASM-International, the Total Excellence in Manufacturing Award from SME, the John Jeppson's Award from the American Ceramic Society as well as the Distinguished Alumni Awards from the University of Illinois, the Indian Institute of Science, and Georgia Tech. He is a Fellow of IMAPS and the American Ceramics Society, and a Member of the National Academy of Engineering. He was the President of the IEEE CPMT Society and the IMAPS Society.