Chip-to-Chip Optoelectronics SOP on Organic Boards or Packages

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***Abstract*—In this paper, we demonstrate compatibility of hybrid, large-scale integration of both active and passive devices and components onto standard printed wiring boards in order to address mixed signal system-on-package (SOP)-based systems and applications. Fabrication, integration and characterization of high density passive components are presented, which includes the first time fabrication on FR-4 boards of a polymer buffer layer with nano scale local smoothness, blazed polymer surface relief gratings recorded by incoherent illumination, arrays of polymer micro lenses, and embedded bare die commercial p-i-n photodetectors. These embedded optical components are the essential building blocks toward a highly integrated SOP technology. The effort in this research demonstrates the potential for merging high-performance optical functions with traditional digital and radio frequency (RF) electronics onto large area and low-cost manufacturing methodologies for multifunction applications.**

***Index Terms*—optical interconnections, optical planar waveguides.**

I. INTRODUCTION

OPTOELECTRONICS research has been very extensive over the last three decades. It has moved from fiber-based long distance communications in the 1980s, to shorter distances, system-to-system communications in the 1990s and recently to the back plane inside the box. The next evolutionary step is to extend optical signaling between chips on a module, as shown in Fig. 1. At data rates up to 10 Gb/s, direct chip-to-chip and intra-chip interconnects are well within the realm of conductive data transmission over about 1 cm distances. Optical links within a chip or between chips have been demonstrated but have not progressed beyond laboratory research. See, for example, the work reported in [1]–[3]. As such, it is worth reviewing the question as to where the divide between conductive and optical digital data transmission lies.

A number of designers have addressed this question from the point of view of power dissipation [4], [5], wire latency and power dissipation [6], and interconnect density [7], [8]. The broad conclusions are that 1) the main impediment to the evolution of dense (very large scale integration—VLSI) optical interconnects on chip or on package, based on arrays of directly modulated sources, is directly traced to the low yield and long-term reliability of vertical-cavity surface-emitting laser (VCSEL) arrays in the areas of low threshold current, wavelength control and low power supply voltage, for example, [7], [9], 2) For on-chip application, the detector is a major source of electrical power dissipation since it is biased as a low signal amplifier and the bias current is always on, in contrast to CMOS logic circuits which generally draw power only during switching. This situation is ameliorated in favor of optics in those situations in which an array of lasers share a common bias circuit and an array of receiver TIAs and post amplifiers also have a common bias circuitry [10]. 3) In terms of propagation delay, it is generally agreed that optical links can have lower latency than electrical links even over a few millimeters propagation distance, depending on line cross section [11], [12]. (4) Optical interconnect density is competitive with off-chip interconnect density because waveguide cores can be of the order of the optical wavelength, high-contrast index waveguides can be close together because of low crosstalk, signal fan-out is achievable to some extent and the dimensions of directly modulated VCSEL, FP lasers and detector bare dies are of the order of 70–100 μm, with electrical pads, comparable in size to present solder interconnects [9], [10].

The general conclusion is that VLSI optical interconnects can simplify the high-end system architecture by replacing wide copper buses with one optical link, eliminating many decoupling capacitors and using inexpensive board materials with relatively high loss tangents [10]. Optical signaling will migrate on chip at some time, but not in the near future.

This paper addresses the need for miniaturized, high bandwidth, low cost systems by demonstrating building blocks toward high density optoelectronic integration in an SOP module. Optoelectronic passive and active components are embedded in low-cost large-area organic boards. This is made possible by the formation of a buffer layer having nano scale local roughness that reduces optical losses.

II. GLOBAL R & D DEVELOPMENTS IN OPTOELECTRONICS

The primary focus of optoelectronics research at Georgia Tech's Packaging Research center is on highly integrated chip-to-chip optoelectronics by means of embedded active and passive optoelectronic components. Prof. Jokerst, *et al.* report on the progress they made in this area on Silicon, ceramic and on high temperature printed wiring boards [13]. A number of researchers around the world have made great strides in designing and fabricating chip-to-chip optoelectronics for high-speed digital data transport over wide areas at the board integration level. The Fraunhofer Institute, IZM in Germany, for example, has developed a hybrid carrier that provides complete compatibility between electrical and optical surface mounted components [14]. The key element of the electrical-optical

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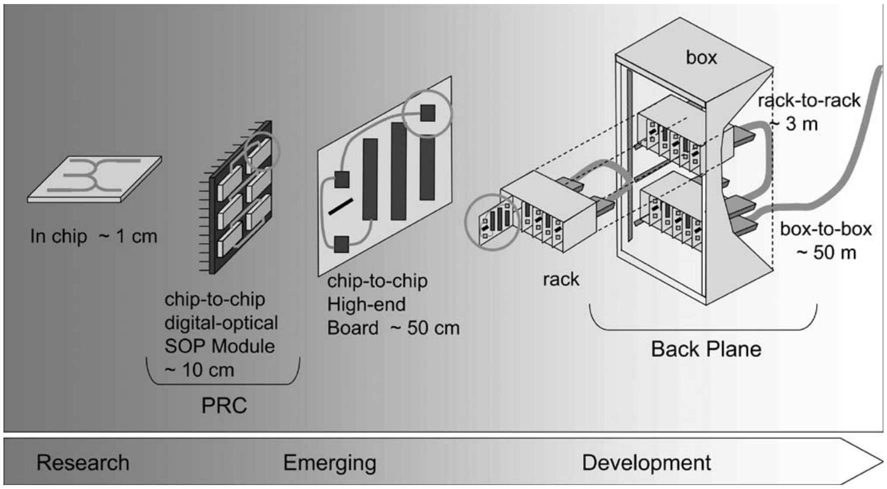


Fig. 1. Progression of optical data links toward the processor.

circuit board (EOCB) concept is the formation of an additional optical layer consisting of multimode waveguide structures. Waveguides are incorporated within the circuit board optical layer by a hot embossing processes and standard printed wiring board (PWB) fabrication technology. Multimode waveguides are used to meet assembly tolerances in order to interface to common surface mount packages and comply with pick and place surface mount technology (SMT) assembly tolerances. Optoelectronic devices have to fit within these process tolerances. The institute is also developing a hybrid polymer-silica vertical coupler switch in which silica waveguides are used for low loss transport and the polymer, having a much higher thermal-optic coefficient, is used to affect the coupling and thermal switching [15], [16]. Similarly, NTT has developed chip-to-chip optical communication using surface mount technology and waveguides embedded in a printed wiring board [17]. The University of Texas, in collaboration with Cray Research, GE Research, Radiant Research, Honeywell, and MMC developed an optical clock synchronization architecture for a Cray multilayer mother board. The optical signal distribution network consisted of VCSEL emitters, grating couplers, metal–semiconductor–metal (MSM) detectors and optical clock signal broadcast on polyimide waveguides [1].

Wafer level, heterogeneous integration of CMOS logic with a VLSI array of paired VCSELs and photodetectors was demonstrated at Bell Labs [7], and achieved an unprecedented optical integration density directly connected to the processor chip. Tohoku University has developed a multichip module in which chips are thinned and stacked and embedded horizontal waveguides distribute an optical signal vertically by integrated micromirrors [18]. In the spirit of the pioneering work at Bell Labs, Cornell University has demonstrated homogeneous integration of FET transistors, VCSELs, and photodetectors on a silicon-on-sapphire (SOS) substrate with gigahertz response and have stacked thinned chips to achieve high digital-optical density [19]. While we have given a flavor of the kind of optoelectronic integration work, recent or presently active, the list is by no means exhaustive.

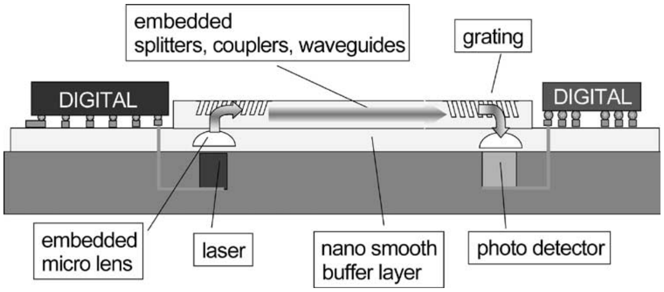
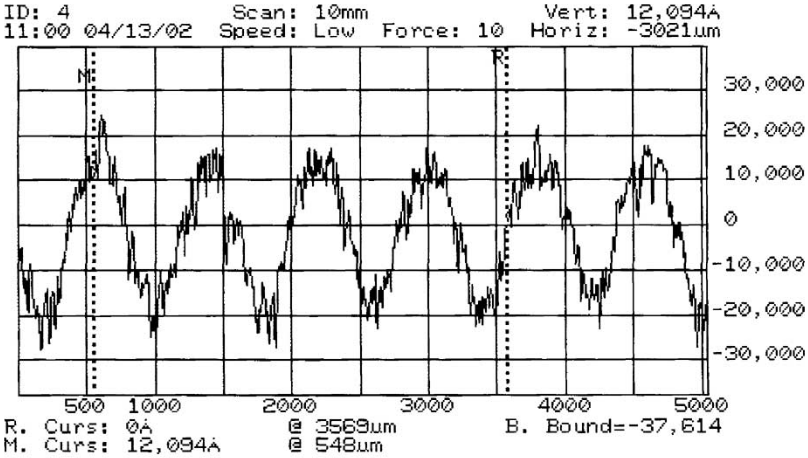


Fig. 2. An SOP concept for low-cost opto/digital integration on FR-4 board.

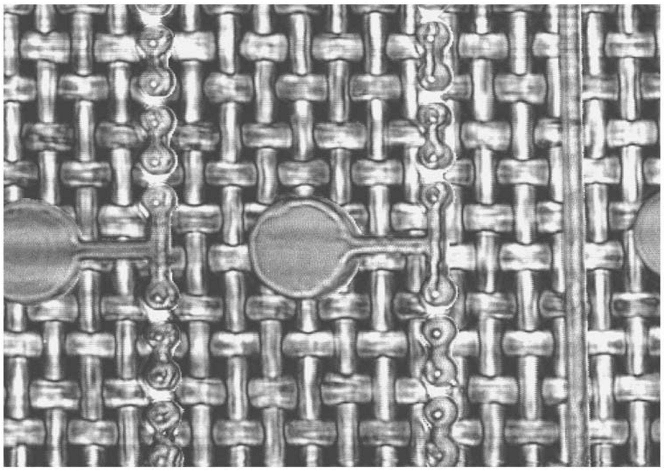
III. OPTOELECTRONICS SOP

System on Package (SOP) is about integration and miniaturization of two or more component technologies to achieve new system level functionalities and higher system performance at lower cost. One instance of an SOP concept for digital-optical integration at the wide area board level is shown in Fig. 2 where the emphasis is on high speed, integrated, chip-to-chip optical clock and data transmission. Wide area, high speed optical clock and data transport simplifies the digital architecture because fewer parallel transmission lines are needed for the same bandwidth and because optical links have low cross talk and are not susceptible to electromagnetic interference (EMI) noise, thus also reducing the need for decoupling capacitors. This is an example of how this particular SOP concept simplifies system design, enhances system performance and reduces overall cost.

In Fig. 2, are shown the basic technologies required for a fully integrated digital-optical microsystem. The text boxes indicate enabling integration technologies which have to be developed to achieve full digital-optical functionality. Each high-frequency output port from a processor modulates a specific laser in an array. The digitized optical signal is coupled through a microlens array, into the optical signal distribution network comprising waveguides, splitters, couplers, gratings, etc., where it is transported to its destination, is detected by a specific photodiode in an array of optical receivers, and converted to an electrical signal that is input into a specific port of the receiving pro-



(a)



(b)

Fig. 3. (a) Topography of a copper clad FR-4 surface, measured by Dektek 3030D. (b) C-SAM photography shows interior structure of a board with copper features, microvias, and woven glass fiber.

cessor. The signaling is bi-directional and nonblocking. Optical signals are coupled in and out of the optical transport network by a number of means that include gratings, lenses, waveguide end-mirrors, directional couplers and evanescent coupling. The entire opto/digital microsystem is built directly on the buffer layer which is fabricated on low cost FR-4 and APPE boards. Enabling building block technologies that are being developed at the Georgia Tech Packaging Research Center toward the realization of a fully integrated mixed signal SOP module are presented in the next section.

IV. ORGANIC BOARD COMPATIBLE EMBEDDED OPTOELECTRONICS

A. Fabrication and Characterization of Nanometer-Scale Smooth Buffer Layers on FR-4 Boards

Most FR-4-type bare boards have ±2 to ±4 μm waviness with period of 400 to 800 μm and local roughness of ±0.4 to ±0.5 μm, depending on vendor. The waviness arises from the woven fiberglass buried inside the board for reinforcement. The roughness on the top surface polymer is due to the board fabrication process. The flatness and roughness of a built-up layer PWB depends on the circuit structures and fabrication processes. A typical build-up PWB has 10 μm to 18 μm thick copper lines embedded in a dielectric film which has been intentionally roughened to a root-mean-square (rms) roughness of about 0.5 μm in order to increase metallurgical adhesion. In Fig. 3(a) is shown a profilometer (DekTak 3030) scan of the surface of a bare FR-4 board. The waviness is approximately 4 μm peak to peak with a period of 800 μm and the measured local roughness is $+/-0.5$ μm. In Fig. 3(b) is shown a three-dimensional (3-D) ultrasonic image of a high density built-up interconnect board obtained with a C-SAM Technology ultrasonic microscope. Copper lines, bonding pads, and microvias are clearly seen, as is the woven glass fibers.

This type of surface is completely unsuitable for the fabrication of an optical waveguide network. A local roughness that is greater than $+/-25$ nm [20] will contribute to optical scattering losses. To minimize scattering loss, waveguides must have smooth surfaces. To meet this requirement necessitates, in part, the development of materials and processes designed to planarize rough surfaces.

The enabling technology for implementing lightwave circuits on inexpensive printed wiring boards is the formation of a buffer

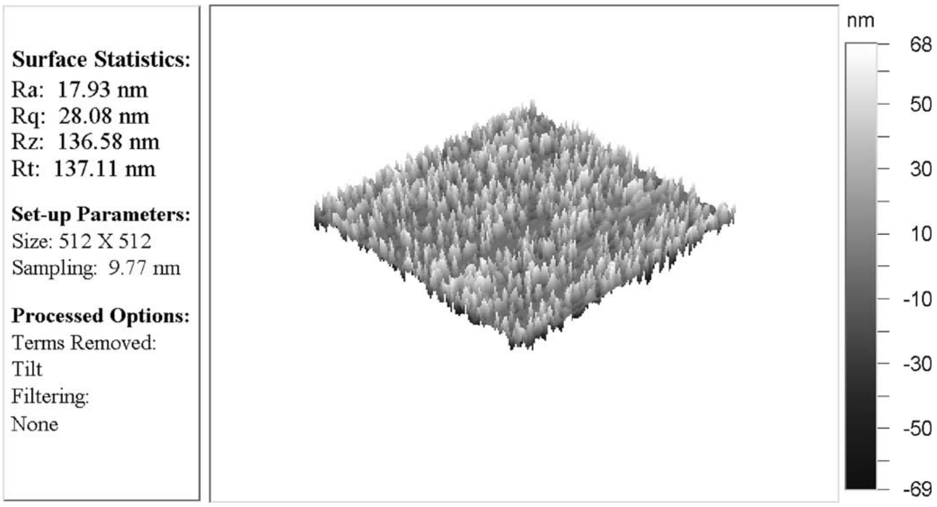


Fig. 4. AFM topograph of a $5\ \mu m \times 5\ \mu m$ area of the buffer layer stack showing a local roughness of 18 nm.

layer which serves two functions: 1) it provides a planar and smooth surface for waveguide fabrication and 2) it provides a transition layer for strain relaxation due to the CTE mismatch between the embedded metallurgy and the waveguide layer [21]. The former minimizes scattering losses in waveguides due to local roughness, while the latter enhances thermal reliability and minimizes strain on the aveguide and embedded structures. Greater detail of local surface roughness of our buffer layer is obtained by atomic force microscopy (AFM). In Fig. 4 is shown a tapping mode AFM topograph of our buffer layer over a $5\ \mu m \times 5\ \mu m$ area. The average surface roughness is less than 18 nm. The buffer layer is fabricated by an inexpensive, low temperature, polymer process. The buffer layer is formed by a multi layer meniscus and/or spin-coating process consisting of an epoxy-based polymer which is partially cured, followed by a layer of Siloxane polymer. The first polymeer does most of the planarization and the second does most of the local smoothing and adds to the planarization. After final curing, the total thickness of the resulting buffer layer is approximately 30 μm which depends on the starting structure beneath the buffer layer.

The importance of a buffer layer for lightwave circuits on FR-4 boards has also been reported in other publications. For example, Suzuki *et al.* [22] report only the long range waviness of their BCB buffer layer. A smooth buffer layer has also been developed for high-density electrical integration in order to permit photolithographic definition of fine pitch copper lines and has been reported by Liu, *et al.* [23].

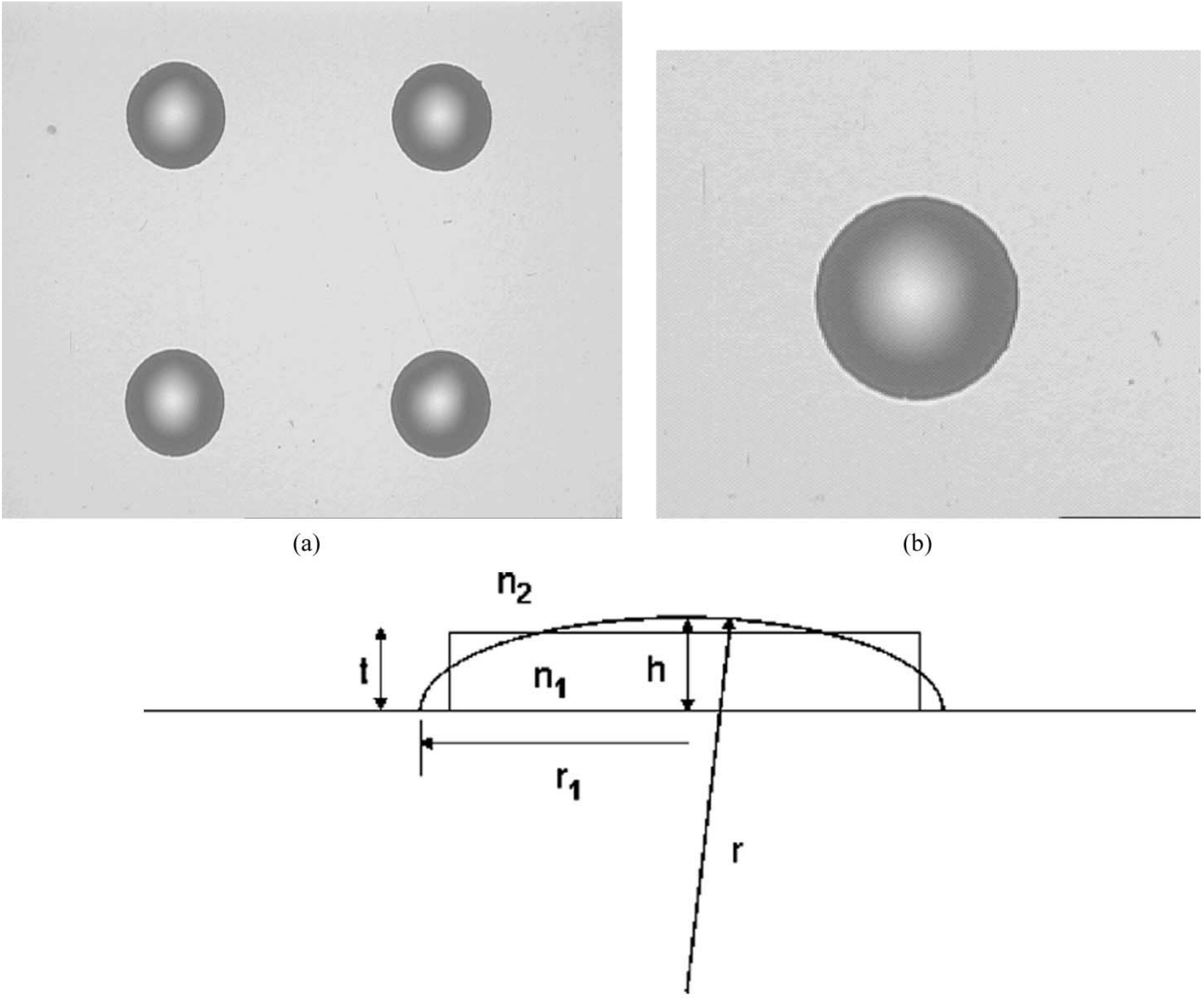
Material requirements for fabricating low loss optical waveguides on PWB's are: 1) a buffer layer to control micro roughness and minimize long range waviness and to provide strain relief from the underlying substrate metallurgy, 2) high transparency of the waveguide material at the working wavelength, 3) good interface adhesion, 4) minimal residual roughness from processing, 5) a coefficient of thermal expansion that is consistent with that of the substrate board and polymers, 6) low moisture content to minimize O-H absorption, 7) resistance to oxidation, solvents and metal plating chemicals, and 8) low bulk modulus for strain relief during solder reflow temperature excursions. A large number of potential polymers have been evaluated for this application over the past decade by numerous groups. Broad category of these are polycabonates, acrylates, polyimides, polymethylmethacrylates, polycyanurates, siloxanes, BCB, and fluorinated versions of these [24].

B. Integration of Microlenses for Optical I/Os

Micro lens arrays are necessary for maintaining coupling efficiency in free space optics. For example, it is used to collimate a free space beam incident on a grating structure or for focusing a beam onto a detector. As shown in Fig. 5(a) we have fabricated micro lenses and arrays of these by a simple and effective polymer reflow process described in [25]. The focal length of the lenslet is defined by the initial thickness (t) and the base diameter $(\mathrm{r}_{\mathbf{1}})$ of the initial polymer pillbox before reflow, see Fig. 5(c). The focal length (f) of the lenslet is given by $\mathrm{f} = \mathrm{n}_{\mathbf{2}}\mathrm{r}/(\mathrm{n}_{\mathbf{1}} - \mathrm{n}_{\mathbf{2}})$ and r is given by the measured lenslet parameters as $\mathrm{r} = (\mathrm{h}^{\mathbf{2}} + \mathrm{r}_{\mathbf{1}}^{\mathbf{2}})/2\mathrm{h}$. The indexes of refraction $\mathrm{n}_{\mathbf{1}}$ and $\mathrm{n}_{\mathbf{2}}$ refer to the lenslet material and surrounding medium, respectively. We can calculate the focal length of the lenslet represented in Fig. 5(b) from the measured values of the polymer pillbox prior to reflow: $\mathrm{r}_{\mathbf{1}} = 125\,\boldsymbol{\mu}\mathrm{m}, \mathrm{h} = 25\,\boldsymbol{\mu}\mathrm{m}, \mathrm{r}_{\mathbf{1}} = 250\,\mu\mathrm{m}$ and by using $\mathrm{n}_{\mathbf{1}} = 1.55$ and $\mathrm{n}_{\mathbf{2}} = 1.0$, we find $\mathrm{f} = 210\ \boldsymbol{\mu}\mathrm{m}$, consistent with previously reported work [25].

C. Fabrication of Blazed Polymer Gratings With Incoherent Illuminations

Blazed surface relief gratings are important wavelength sensitive components that are used for wavelength-selective coupling into and out of a waveguide. In Fig. 6 is shown an optical microscope cross section of a surface relief grating having 250 lines/mm and a blaze angle of 36° with respect to the surface normal. Surface relief, blazed gratings can be fabricated on a photo sensitive polymers, for example, a Siloxane polymer, by using a lithographic mask and exposing in the usual manner. The only difference is that instead of normal incident illumination, the blaze structure is formed by illumination at a large angle (e.g., 45°) with respect to the normal to the mask and polymer planes. This simple but



(a) (b)

(c)

Fig. 5. Optical image of (a) a microlens array containing $250\ \mu\mathrm{m}$ diameter microlenses, and (b) a single $250\ \mu\mathrm{m}$ diameter microlens. All are formed on a substrate by polymer reflow. The calculated focal length is $210\ \mu\mathrm{m}$.

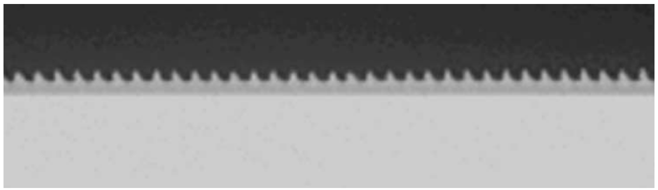


Fig. 6. Optical microscope image of the cross sectional of a blazed grating formed on polymer by using only incoherent optics. The groove height is $2\ \mu\mathrm{m}$.

effective procedure represents the first time that blazed gratings have been fabricated on photo sensitive polymers using only incoherent illumination. The ultraviolet exposure tool is a Tamarack Scientific Co., Inc. Model 152R with a Hg vapor bulb having principal emission at 365 nm. While Fig. 6 is meant to demonstrate the feasibility of our simple and novel blazed grating fabrication process on a planar buffer layer substrate, we are adapting the fabrication process for directly writing gratings on low multimode and single mode waveguides.

D. Multimode Polymer Waveguide Fabrication and Integration on FR-4 Boards

An example of an array of ridge polymer waveguides fabricated above the metallurgy built-up layer on FR4-type organic fiber boards is shown in Fig. 7. The buffer layer was formed on the metallized FR-4 board as described in Section IV-A. A lower cladding layer was deposited on the buffer layer. The core polymer was photo defined to form an array of ridge waveguides which were subsequently cladded on top. The waveguide

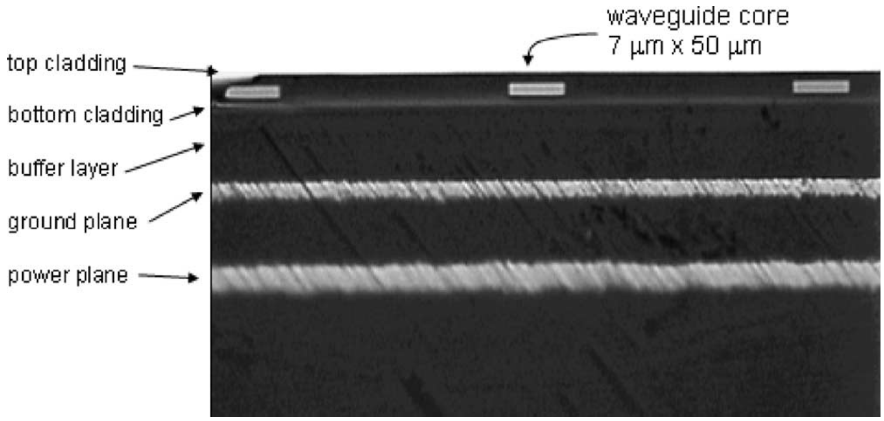


Fig. 7. Polished cross section of a PWB with an embedded array of waveguides. Only three of eight waveguide cores are shown for clarity.

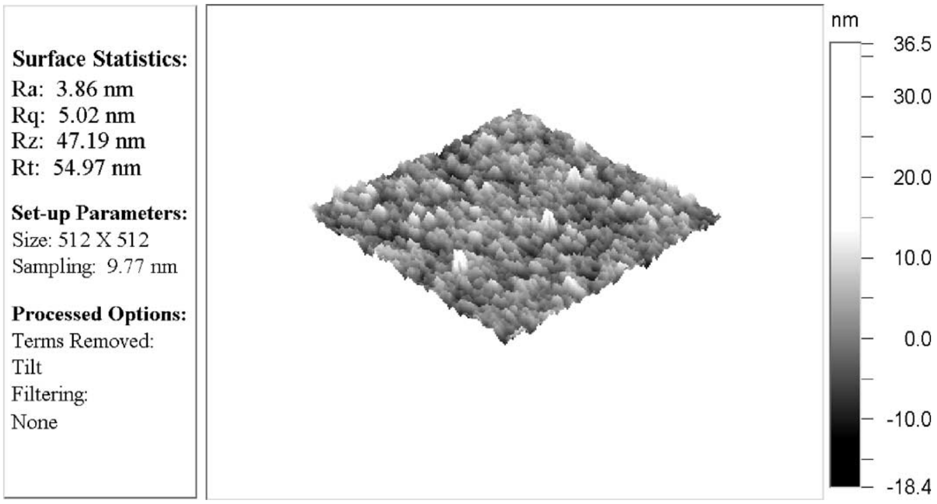


Fig. 8. AFM topograph of a $5\ \mu\text{m} \times 5\ \mu\text{m}$ area of an Inorganic Polymer Glass showing a local roughness of 4 nm.

polymer material used for both core and cladding was photo-definable epoxy-based Siloxane oligomer, which cross links at temperatures less than 160 °C. The core and cladding indices of refraction were measured and are 1.55 and 1.49, respectively. Once the waveguide structure is completed, the end of the FR-4 board and the waveguide array are finely polished to near optical quality and light is end-coupled in (and out of) the array by single mode (and multimode) optical fibers. Waveguide core dimensions are $50\ \mu\text{m} \times 7\ \mu\text{m}$ and are up to 14 cm in length. The cladding layer thickness is greater than $5\ \mu\text{m}$. In Fig. 7 is shown a polished cross section of three waveguides in an array of eight embedded waveguides in a PWB. The cores are accentuated by incandescent light illumination from the back side. A polymer which we are evaluating for its planarization and optical waveguide properties is an inorganic polymer glass (IPG) of proprietary composition and process, and will be referred to simply as "IPG". IPG is available from PRO Pty, Ltd. This polymer provides exceptional planarization. A tapping mode AFM area topograph of IPG on a PWB is shown in Fig. 8.

Waveguide losses were measured by the cut back method for waveguides having an IPG core of cross section $50\ \mu\text{m} \times 30\ \mu\text{m}$ and Siloxane cladding having thickness of $7\ \mu\text{m}$ for the bottom cladding and about $2\ \mu\text{m}$ for the top cladding. An array of eight waveguides, each 14 cm long and each having an "S-turn" at mid section, were used for these measurements. Each section of the "S" turn has a radius of curvature of 1 cm. Light was end-coupled into each waveguide using a single mode optical fiber with $8\ \mu\text{m}$ core diameter, and the throughput was collected by a multimode optical fiber having a core diameter of 62.5 mm and guided to a calibrated detector. The troughput of each of the eight waveguides in the array was measured before and after each section cut. For this core/cladding combination, the measured propagation losses, averaged over eight waveguides in the array, were found to be: $0.24 + /- 0.08$ dB/cm at 1322 nm and $0.52 +/- 0.11$ dB/cm at 1548 nm. A graphical plot of the cutback data is shown in Fig. 9. Measurement consistency and waveguide-to-waveguide variation is summarized in Table I for the eight waveguides prior to cut back. It is seen that the variation in waveguide-to-waveguide insertion loss is ±0.08 dB at $1.32\ \mu\text{m}$ and ±0.11 dB at $1.55\ \mu\text{m}$. In Table I, the left column is the waveguide number and the middle and right columns are the insertion loss in dB at the indicated wavelengths. A table similar to Table I is compiled after each of the six section cuts during the cutback measurement process.

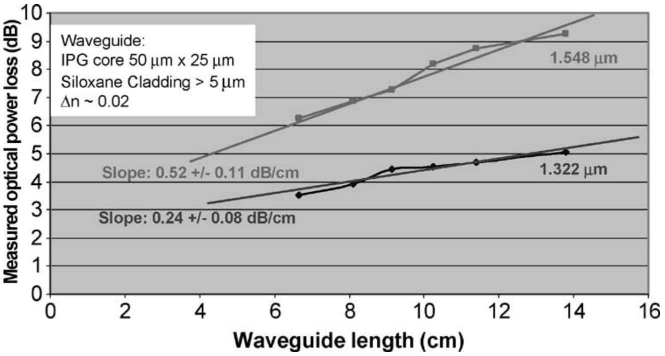


Fig. 9. Waveguide loss measured by the cut back method and averaged over eight waveguides.

TABLE I
LOSS MEASUREMENT FOR EACH OF 8 "S" TURN WAVEGUIDES, EACH 13.8 cm LONG

Waveguide length is 13.8 cm		
Channel	**Loss, dB** (λ=1.55 um)	**Loss, dB** (λ=1.32 um)
1	9.02	5.05
2	9.42	5.11
3	9.27	5.05
4	9.19	4.93
5	9.22	5.16
6	9.29	5.13
7	9.16	5.10
8	9.18	4.98
Av	9.22	5.06
S.Div.	± 0.11	± 0.08
% Div.	1.2%	1.6%

E. Embedded InGaAs PIN Photodetector in Polymer Waveguide on SOP

We have developed a method for embedding commercially available photodiodes on FR-4 boards. The embedding process has a high yield (eight of eight detectors have been successfully embedded to date) and applies equally well to edge emitting lasers, VCSELs, laser amplifiers and arrays thereof. A bare die PiN photodetector, purchased from Lumei, and embedded on an FR-4 board is shown in Fig. 10(a). The active area of the detector is 36 μm in diameter and is evanescently coupled to a polymer waveguide having IPG core with dimensions $50\ \mu\mathrm{m} \times 22\ \mu\mathrm{m}$ and a Siloxane cladding, as described above. The waveguide extends to the edge of the board where it has a polished cross section as described in Section IV-D. A cross section schematic drawing of the embedding process is shown in Fig. 10(b). "Polymer" refers to the buffer layer discussed in Section IV-A. An optical signal is end-coupled into the waveguide at the edge of the board, and the photocurrent of the PiN is measured at wavelengths of 1320 nm and 1540 nm.

The PiN dark current and current under 1320 nm illumination from the coupled waveguide is shown in Fig. 10(c). The photodetector has a responsivity of 0.8 A/W at wavelength of $1.3\ \mu\mathrm{m}$ as specified by the manufacturer, AXT.

The coupling efficiency between detector and waveguide for another embedded PiN photodiode from the same vendor was calculated from the measured photocurrent as described below. The coupling efficiency was found to be 3.2% at 1320 nm, consistent with the reported value of 2.9% for evanescently coupled thin film MSM detectors on ceramic substrates [26].

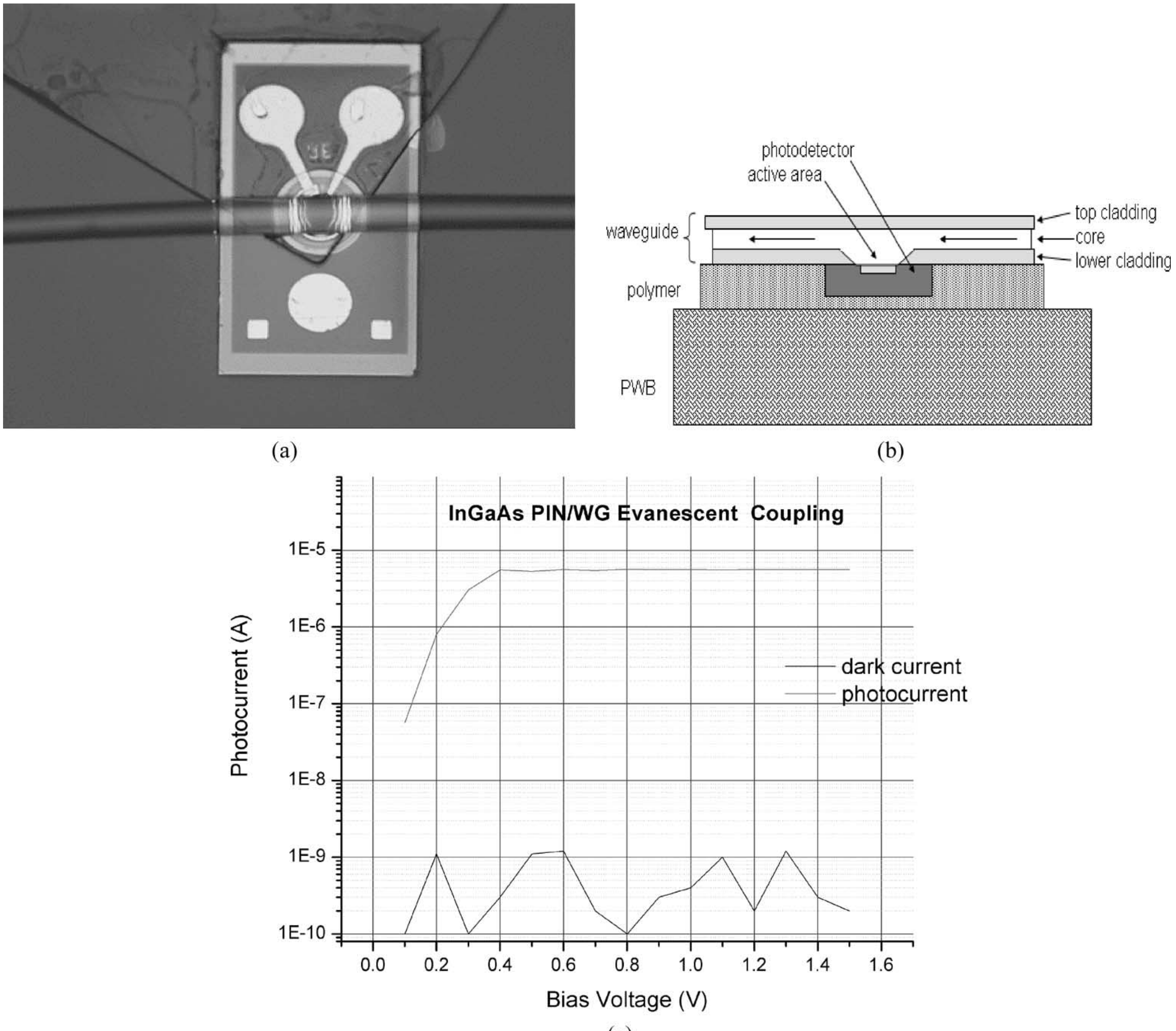
The coupling efficiency, ζ, is defined as the ratio of the power available at the detector and the detected power: $\zeta = \mathrm{Pd}/\mathrm{Pa}$ where Pd is the detected optical power and Pa is the area normalized, available optical power at the detector. We have used a configuration in which light is end-coupled from an external SM optical fiber into the waveguide as described above. The waveguide extends to the edge of the PWB and is polished to near optical quality. The estimated OF-WG coupling loss is 2 dB based on throughput measurements and simulations in conjunction with Fig. 11. Then, $\mathrm{Pa} = [1 - (\text{coupling loss} + \text{propagation loss}] \times \mathrm{Rdw} \times \mathrm{Pi}$, where Rdw is the ratio of detector active area to the available waveguide area at the detector diameter, and Pi is the power incident on the waveguide end facet. The detector for which the coupling efficiency was measured is a PiN photodiode manufactured by AXT, having an active area diameter of 36 μm, a responsivity of 0.8 A/W at 1320 nm and was operated at -1.5 V. Optical dc power was launched into the waveguide from a single mode fiber pigtail with measured output of 1 mW $+/-0.1$ mW at 1320 nm. The waveguide core material is IPG and the core dimensions are $50\ \mu\mathrm{m}\ \text{wide} \times 22\ \mu\mathrm{m}\ \text{thick}$. The waveguide cladding material is Epoxy Siloxane Oligomer. The measured waveguide loss gradient for this structure is shown in Fig. 9. The distance between the detector active region and the waveguide input facet is 2.5 cm. We estimated the (coupling loss + propagation loss) to be 2.75 dB at 1320 nm. The measured dc current at the detector was 7.5 μA. The deduced optical power at the detector (Pd) is, therefore, 9.4 μW. The ratio of detector active area to the active area of the waveguide at the detector diameter is 0.56. We find for the available power at the detector (Pa) 297 μW. Then the estimated coupling efficiency (ζ) is found to be 3.2%.

This represents the first time that a commercially available, thick, bare die photo detector has been embedded on an FR-4 board. A total of 8 out of 8 similar detectors from two vendors have so far been successfully embedded, of which 4 were tested, two were damaged during testing and two were damaged during waveguide re-work. The embedding process described above applies equally well to commercially available photo detectors, lasers, laser amplifiers and arrays of these, and will be the subject of a future publications. The advantage of embedding commercial bare die detectors is availability from various sources and thermal management by soldering lasers and detectors to a common ground plane that can be cooled.

V. WAVEGUIDE INSERTION LOSS MEASUREMENTS AND RELIABILITY ISSUES

A. Insertion Loss Measurements

We measure insertion losses using an array of ridge waveguides. The waveguide array consists of five cladded waveguides,



(a) (b)

(c)

Fig. 10. (a) Optical microscope view of an embedded PiN detector with dimensions 250 μm × 350 μm × 150 μm thick and having a 36 μm diameter active area. (b) A schematic cross section of the embedding process. (c) Dark current and evanescently coupled photocurrent as a function of reverse bias voltage. Light output (1 mW at 1320 nm) from a single mode, pigtail fiber is end-coupled to the waveguide through a polished waveguide facet as discussed above. The dark current is very low, hence the apparent "noise".

spaced by 250 μm, in the form of a semi circle having a radius of curvature of 1 cm and tangential elongations of approximately 1 cm at each end, resulting in a total length of 5 cm. Each waveguide has a cross section of 7 μm by 50 μm, The ridge waveguide array is constructed on a buffer layer on an FR-4 type board as described above. Waveguides are composed of Epoxy Silixane Oligomer core and cladding with ($n_{\mathrm{core}} = 1.55$; $n_{\mathrm{clad}} = 1.49$). The experimental setup for the insertion loss measurement is shown in Fig. 11. The continuous-wave (CW) power at wavelength 1.55 μm or 1.32 μm is launched into the polished end facet of the input waveguide from a cleaved SMF pigtail. At the waveguide output facet, also polished, the transmitted power is coupled into a cleaved MMF pigtail and measured by a calibrated optical power detector. The core diameter of the SMF is 8.06 μm; its refractive indexes are 1.46 for the core and 1.44 for the cladding layer. The MMF has a diameter of 62.5 μm and the core refractive index is 1.52 whereas that of cladding is 1.50. The reasons for using cleaved SMF and MMF

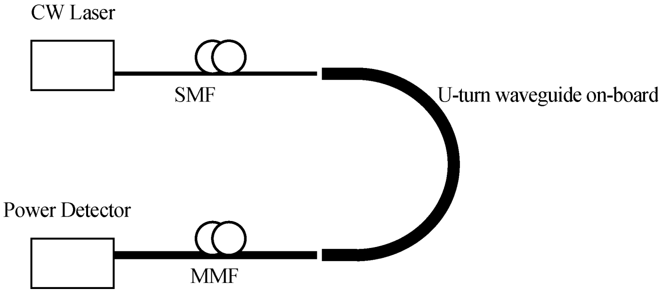


Fig. 11. The experiment setup for the total insertion loss easurement.

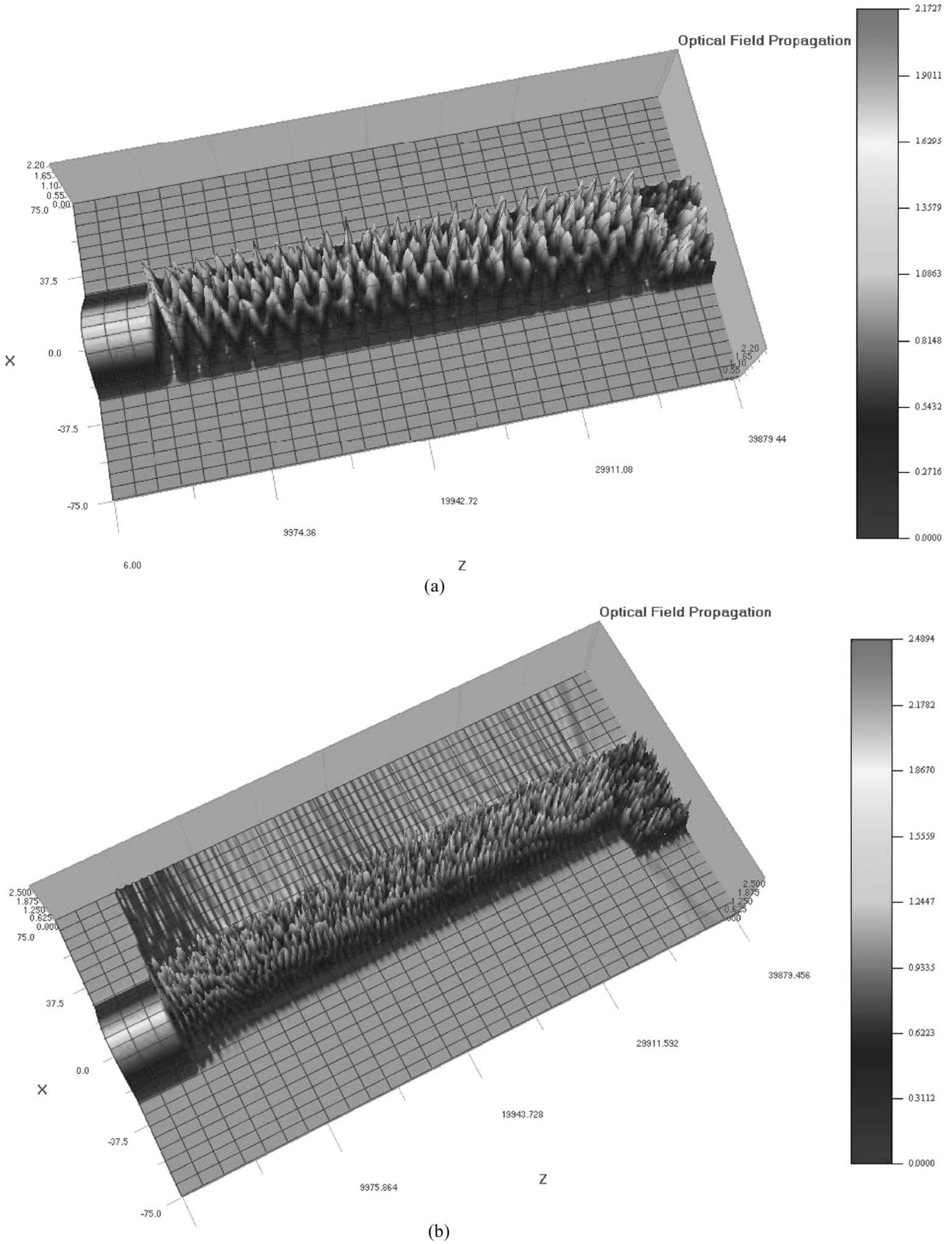


Fig. 12. (a) Total TE and (b) total TM field amplitude propagating through the curved waveguide.

pigtails at the waveguide input and output end facets, respectively, is to optimize the input and output coupling.

The butt-coupling scheme is used to couple light in and out of the waveguide as an expedient while integrated optical I/O couplings are under development. The two pigtail fibers are individually held and positioned by bare fiber holders and 5-axes (normal x-, y-and z-axis plus elevation and azimuthal direction) manual stages having 3 $\mu\mathrm{m}$with a minimum reading of 5 $\mu\mathrm{m}$. Care must be taken to precisely adjust the alignment between fibers and the waveguide in order to obtain the maximum coupling efficiency. Using this coupling scheme and experimental setup, the minimum total insertion loss of cladded Siloxane waveguides was found to be -18.99 dB at 1550 nm and -11.17 dB at 1310 nm.

B. Bending Loss Characterization

From the ray-tracing equation of geometrical optics, there are no bound rays on bent waveguides. Electromagnetic energy leaks through the mechanism of tunneling, or refraction or both. The tunneling mechanism, in this instance, is a form of frustrated total internal reflection caused by the curved core-cladding interface and the bound nature of the wave front, and is related to the Goos-Hanchen effect for bounded waves. To calculate the radiation loss from the on-board waveguide due to its bending radius, the BPM-based computational electromagnetic simulation incorporated with the conformal mapping technique is applied. The curved waveguide section is transformed to a straight one with modified refractive index at every mesh grid along the straight waveguide.

Fig. 12(a) shows the TE field amplitudes propagating through the waveguide. The radius of curvature is $10\,250$ $\mu\mathrm{m}$ with a bent length of $32\,201$ $\mu\mathrm{m}$. The straight input and output sections of the waveguide are set to 400 $\mu\mathrm{m}$ for the sake of saving computational resources without loss of computational accuracy. As one can observe in Fig. 12(a), optical fields are strongly confined along the bending region since no leaky fields are observed. In contrast, the wave propagation for TM modes is somewhat leaky, as shown in Fig. 12(b). In this case, according to the numerical simulation, the output power is -0.8359 dB less than the input power. Experimentally, the measured difference in throughput between TE and TM input polarizations is 1.12 dB, therefore, the bending loss for the two polarizations is experimentally estimated to be 0.326 dB/cm when coupling losses for both polarizations are taken into account.

C. Reliability Issues

Reliability of optoelectronic components is of great concern particularly if they are made of organic polymer materials. The reasons are: 1) All organics absorb water, and 2) most organics are not as dimensionally stable as silicon and other inorganic materials. Accelerated thermal aging and optical aging are critical tests for choosing a viable optical waveguide polymer and polymer fabrication processes. While optical aging tests are under way, we report on thermal shock cycling results for an array of siloxane, ridge polymer waveguides. The core/cladding indices of refraction are 1.55/1.49 respectively. Siloxane is reported by the vendor to have about 1% moisture content, to be stable up to 350 °C and to be highly resistant to oxidation. An array of five parallel Siloxane waveguides (7 $\mu\mathrm{m} \times 50$ $\mu\mathrm{m}$ with 7 $\mu\mathrm{m}$ thick cladding) was fabricated on a buffer layer on an FR-4 board, as described above, and subsequently subjected to thermal shock cycles between -55 °C and 125 °C. After 300 cycles, the insertion loss increased by 35 dB. The optical absorbance spectrum of a 2.9-mm-thick Siloxane sample showed no substantial difference at wavelengths of 1550 nm and 1310 nm, after being cycled in the same way 300 times, as shown in Fig. 13. No evidence of cracking is visible after 300 cycles under dark field illumination and further investigations continue.

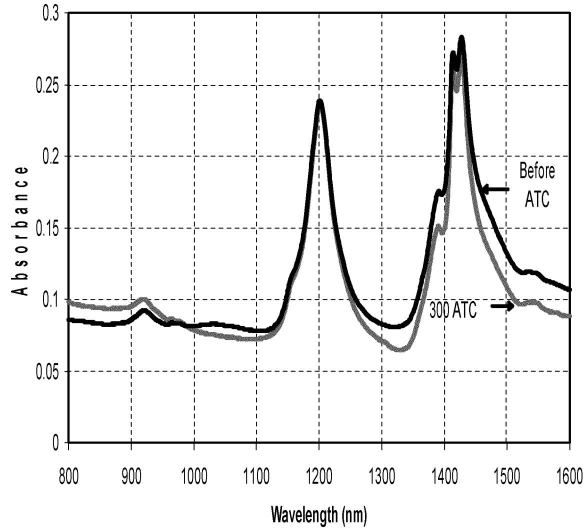


Fig. 13. Absorbance spectra (absolute units) of a 2.9-mm-thick siloxane sample before thermal shock cycling and after 300 cycles measured in a dual beam spectrometer.

VI. CONCLUSION

We have developed a low-temperature polymer process for fabricating and integrating optical passives as well as for embedding active optoelectronic components on printed wiring boards for mixed signal SOP applications. We have demonstrated, for the first time, three new key enabling technologies for optoelectronic integration on low cost boards. These are 1) first time fabrication of a low temperature polymer buffer layer having a measured nanometer scale local roughness, which enables large-scale integration of active and passive optoelectronic devices and components. 2) First time demonstration of embedded commercially available, bare die optoelectronic components with optical coupling to polymer waveguides. 3) First time fabrication of fine pitch, blazed, polymer gratings by using only incoherent illumination.

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Gee-Kung Chang (M'82–SM'92) received the Bachelor degree in physics from National Tsinghua University in Taiwan in 1969 and the doctoral degree in physics from the University of California, Riverside, in 1976.

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Dr. Liu received the Global Collaboration Award for his outstanding contributions to the NSF Programs and numerous national outstanding awards from China. His paper on "Nitrogen Temperature Super-Conducting Ring Experiment" was voted as the "Memorable Paper of the *American Journal of Physics* (AJP) since 1933" and his name was listed in the "AJP All-Star" team.

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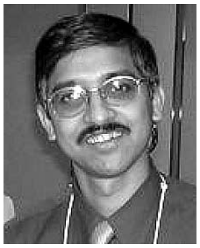

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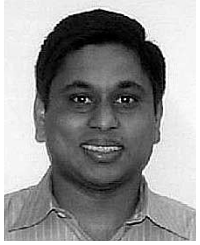
Mr. Sundaram is a member of the High Density Substrate Technical Committee (TC-6) of the IEEE-CPMT society, PRC program manager for the SOP Technology Transfer Partnership with Endicott Interconnect, New York, and the High-Density Substrate Task Leader for the multimillion dollar Nano-Wafer Level Packaging Program.



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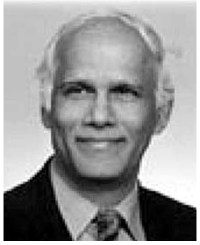

Rao R. Tummala (M'81–SM'84–F'92) received the B.E. degree in metallurgical engineering from the Indian Institute of Science, Bangalore, and the Ph.D. degree in materials science and engineering (MSE) from the University of Illinois, in 1969.

He is an Endowed Chair Professor in electrical and computer engineering and MSE with the Georgia Institute of Technology (Georgia Tech), Atlanta. He is also the Founding Director of the Microsystems Packaging Research Center (PRC). The PRC is currently the largest and most comprehensive microsystems packaging center involving 250 students, 30 faculty, and 50 global companies, and was funded by the National Science Foundation (NSF) as one of its Engineering Research Centers in the United States, the Georgia Research Alliance, and the electronics industry, where he is pioneering the system-on-a-package (SOP) vision for mixed-signal systems of the next decade. He is also a Temasek Professor, NUS, Singapore. Prior to joining Georgia Tech, he was an IBM Fellow where he invented a number of major technologies for IBM's products for packaging, displaying, printing, and magnetic storage that include LTCC and scale-up of multilayer alumina ceramic. He was also part of the pioneering team that developed the industry's first flat panel display based on gas discharge display. He was the Director of the Advanced Packaging Technology Laboratory for all of IBM in 14 labs across the United States, Europe, and Japan. He edited the first undergraduate textbook *Fundamentals of Microsystems Packaging* (New York: McGraw-Hill, 2001) currently used by 43 universities around the world. He edited the first modern book in packaging *Microelectronic Packaging Handbook* (1988) which began to catalyze the academic research and educational programs. During this time, he began to lecture and advise universities in this area throughout the United States. Three notable examples are: Chairman of Advisory Board at the Massachusetts Institute of Technology, Cambridge, from 1988 to 1993, at the University of California at Berkeley from 1984 to 1987, and at the University of Illinois, Urbana, from 1983 to 1986. He left IBM in October 1993 and, two weeks later, he wrote the winning NSF proposal for an NSF-Engineering Research Center on SOP. He has published 350 papers and holds 71 U.S. patents.

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