Monolithic Low-Power 6-Gb/s Optical Transmitter for a Silicon HBT-Based Carrier Injection Electroabsorption Modulator

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***Abstract*—Photonic devices monolithically integrated with nanoscale electronic signal processing circuitry in silicon are emerging as a disruptive technology to reduce cost and improve optical system integration and performance. Silicon heterojunction bipolar transistor (HBT)-based carrier injection electroabsorption modulators (EAMs) implemented in a commercial silicon process have several merits, including high speed, low power, low driving voltage, small footprint, and high modulation efficiency. A low-power high-speed optical transmitter driver module has been realized in a 130-nm SiGe BiCMOS process for an HBT-based carrier-injection-type modulator. The transmitter consists of a monolithic $2^7 - 1$ pseudorandom bit sequence generator and a driver circuit with digitally tuned preemphasis strength. With 1.5-V power supply, the transmitter circuit consumes 44.5 mW at an operating speed of 6 Gb/s.**

***Index Terms*—Carrier injection electroabsorption modulator (EAM), low power, monolithic, optical transmitter, preemphasis, pseudorandom bit sequence (PRBS), SiGe BiCMOS, silicon photonics.**

I. Introduction

EVER increasing data rate demands for high-performance computers and data centers have accelerated the need for interchip input–output (I/O) supporting speeds beyond 100 GB/s. Optical interconnect, which has much less dominant frequency-related loss, is favored over electrical interconnect for terascale computing applications [1]. Silicon photonics has rapidly developed over the past two decades, producing monolithically integrated photonic devices and electronic VLSI systems to realize cost-effective building blocks for optical interconnects.

Optical modulators are a key component of integrated silicon photonic chips for optical I/O. The microring modulator structure is widely used and has several merits, including CMOS compatibility and ultralow-power operation [2]. However, the narrow optical bandwidth and high sensitivity to temperature and process variation minimizes the robustness of the microring structure. The implementation of tuning circuitry to improve the performance of this structure contributes considerable overhead power and increases system cost [3]. The commonly used silicon optical modulators are mostly based on PN junctions operating in depletion mode, which requires a high driving voltage swing ($V_{\rm pp} > 4$ V). The high-driving-voltage requirement prevents the full integration of a silicon optical modulator with its drivers in a single chip due to the tradeoff between breakdown voltage and operating speed of CMOS devices. This transmitter design is based on a heterojunction bipolar transistor (HBT) optical modulator that operates in injection mode, which only requires a subvolt driving voltage to turn on and off the device. With its fabrication through the commercial silicon BiCMOS process, the HBT-based modulator offers a promising solution for next-generation inter- or intrachip optical links with the speed of tens of gigabits per second. This brief presents an integrated transmitter driver module to provide drive signals for the silicon HBT-based modulator, exhibiting wide optical bandwidth, high speed, low power, low drive voltage, small footprint, and high modulation efficiency. The driver module incorporates an integrated $2^7 - 1$ pseudorandom bit sequence (PRBS) generator for reliable high-speed testing and a driver circuit featuring digitally tuned preemphasis signal strength. The driver can be applied to a wide range of carrier injection modulators with drive voltage requirements below 1.5 V [4]. In Section II, the operation principle of the HBT-based carrier injection electroabsorption modulator (EAM) is discussed. Section III presents the transmitter design, including the system-level and transistor-level circuit topology. Section IV describes the fabrication and experimental results of the transmitter driver. Conclusions are summarized in Section V.

II. HBT-Based Carrier Injection EAM

Traditional optical modulators employ an electrooptic (EO) effect to realize the modulation, such as the Pockels effect and the Kerr effect. However, the EO effect is very weak in silicon material. Most silicon modulators utilize the free-carrier plasma effect to manipulate the refractive index. As illustrated by Drude [5], the real part of the refractive index, i.e., Δn, and the imaginary part of the refractive index, i.e., $\Delta\alpha$, can be manipulated by the electron and hole density change, i.e., ΔN_e *and* ΔN_h. Soref and Bennett derived an empirical equation for the free-carrier plasma effect in silicon, which is still widely used today [6].

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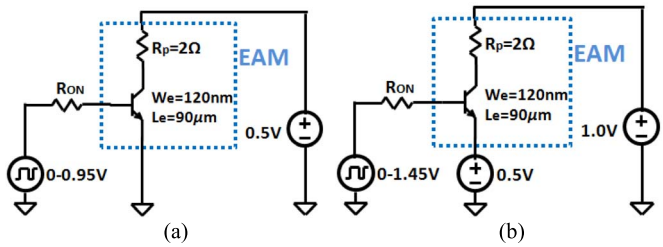

Fig. 1. Electrical model and driving interface of HBT EAM (a) regular and (b) all terminal biases raised by 0.5 V.

A. HBT-Based EAM

By using the HBT transistors in an advanced commercial BiCMOS process that has ultrahigh transition frequency f_T, the HBT-based modulator can work up to hundreds of gigabits per second [7]. In this brief, the HBT modulator is based on the HBT device in a commercial 130-nm SiGe BiCMOS process, and details on the device design are discussed in [7]. It should be noted that several postprocessing steps are required to efficiently couple light into the HBT device. For example, the subcollector is polished down to 0.1 μm, and a cladding layer is grown on the backside of the device.

The optical simulation results in [7] show that the optical field region spans mostly in the base region and the collector directly underneath the base, which means that to realize good modulation efficiency, the free carriers in the base should drastically change. Thus, the HBT device is biased to operate between the saturation region (both PN junctions are deeply forward biased) and the cutoff region (both PN junctions are reverse biased). To get a 5-dB extinction ratio, the HBT only needs a length of around 90 μm with a driving voltage of around 0.95 V, which means that it has outstanding modulation efficiency.

B. Electrical Model

Postprocessing steps introduce several modifications to the standard electrical model of the HBT device provided by the foundry. To account for a thinner subcollector region, an extra parasitic resistor is added with its value calculated as follows. Before polishing, the sheet resistance of a subcollector is 8.8 Ω/sq. After the subcollector is polished from 2 μm down to 0.1 μm, the sheet resistance is increased to 167.2 Ω/sq. With the device length of 90 μm and width of 1 μm, the parasitic resistance is divided by 90 down to 1.86 Ω. A 2-Ω resistor is added at the collector for pessimistic estimation. The electrical model of the HBT EAM and its driving requirement is shown in Fig. 1(a). To achieve a 5-dB extinction ratio, the forward-bias voltage across the base–emitter junction ($V_{\rm be}$) representing logic "1" should be around 0.95 V, given the HBT length of 90 μm [7], [8]. Fig. 1(b) shows a new driving interface in which the voltages of the three terminals of HBT are all raised by 0.5 V. The modification generates a negative $V_{\rm be}$ during the discharge period, resulting in a significant increase in speed.

III. Transmitter

A transmitter is specifically designed for this modulator based on the electrical model, as shown in Fig. 1. To increase the modulator speed, a CMOS driver is designed with a preemphasis feature. The CMOS design helps to considerably reduce the power consumption compared with [8], which is realized by a current mode logic (CML) driver circuit. A 2^7-1 PRBS generator is designed and monolithically integrated into this transmitter, providing a cost-effective means for reliable testing and verification of the modulator and the optical link.

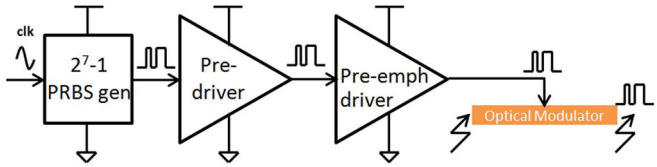

Fig. 2. HBT-based EAM transmitter circuit block diagram.

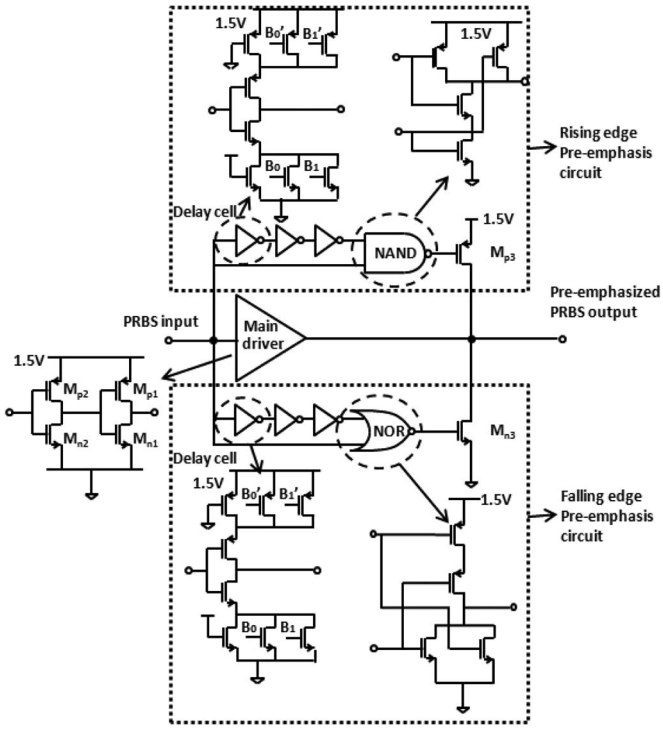

Fig. 3. Preemphasis driver circuit schematic.

A. Block Diagram

The transmitter consists of a 2^7-1 full-rate PRBS generator, a predriver circuit, and a preemphasis driver circuit, as shown in Fig. 2. The PRBS generator adopts CML to guarantee the speed performance. A CML/CMOS hybrid logic predriver stage is inserted between the CML PRBS generator and the CMOS logic preemphasis driver to provide logic transition. With the new driving interface as shown in Fig. 1(b), the preemphasis driver can provide a 1.45-V voltage swing to the base-to-emitter junction of the HBT-based modulator, resulting in a forward bias of 0.95 V and a reverse bias of -0.5 V.

B. Preemphasis Driver

As shown in Fig. 3, the preemphasis driver is comprised of a main driver in parallel with a rising-edge preemphasis circuit and a falling-edge preemphasis circuit. The load of the driver is the HBT modulator with 90-μm emitter length and 120-nm emitter width. To reduce the output resistance $R_{\rm on}$ of the driver, which is very critical for the driving injection modulator, the transistors M_{p1} and M_{n1} in the main driver are designed with a large gate width of 50 and 18 μm, respectively.

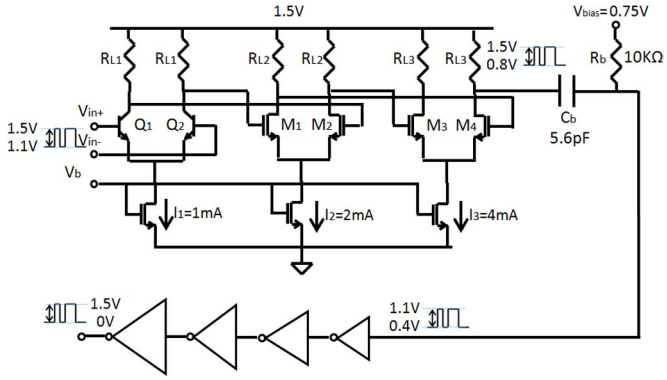

Fig. 4. Predriver circuit schematic.

TABLE I
COMPONENT VALUES OF PREDRIVER

Q_1/Q_2	M_1/M_2	M_3/M_4	R_{L1}/R_{L2}	R_{L3}	R_b	C_b
W=120nm	W=18μm	W=36μm	0.4KΩ	175Ω	10KΩ	5.6pF
L=1.6μm	L=120nm	L=120nm				

The preemphasis circuit further reduces the rising and falling transition times. Transistors M_{p3} and M_{n3} control the rising-edge peaking and the falling-edge peaking, respectively, with the peaking duration set by the total delay of the three identical cascaded delay cells.

The delay of each delay cell can be set by control bits B_1 and B_0. By turning on a combination of parallel transistors, the equivalent "ON" resistance is reduced, resulting in a reduction in cell delay. The control bits yield three different delay setting values: 27, 30, and 38 ps. The original and delayed data signals drive a NAND/NOR gate, which generates the preemphasis pulse at the gate of M_{p3}/M_{n3}.

C. Predriver

The predriver stage is applied between the PRBS generator and the preemphasis driver to provide CML to CMOS logic transition. As shown in Fig. 4, the predriver consists of three CML differential amplifiers with its output ac coupled into a cascade of CMOS inverters. The component values and transistor dimensions are summarized in Table I.

The first differential amplifier utilizes bipolar transistors Q_1 and Q_2, which provide higher transconductance than field-effect transistors (FETs), resulting in a relatively smaller load capacitance to the PRBS generator circuit for a given tail current. The first differential stage works similar to a buffer with unity voltage gain while possessing higher driving capability to the next stage. The second and third stages utilize FET input transistors to prevent the transistors from being driven into the linear region with the amplified signal swing. After the third stage of the differential amplifier, output swing is increased to 700 mV.

A cascade of CMOS inverters with increasing size is used to amplify the voltage swing from 700 mV to rail-to-rail swing. The threshold of the CMOS inverter chain is designed as half of the power supply voltage. The output signal from the CML differential amplifiers is ac coupled by a high-Q metal–insulator–metal capacitor, C_b, and level shifted by biasing a parallel resistor R_b. The values of C_b and R_b are selected to be 5.6 pF and 10 KΩ, respectively, with $f_{-3\,\mathrm{dB}}$ as low as 2.8 MHz to accommodate the wideband PRBS signal.

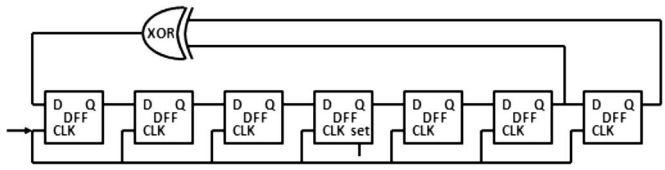

Fig. 5. 2^7-1 PRBS generator circuit.

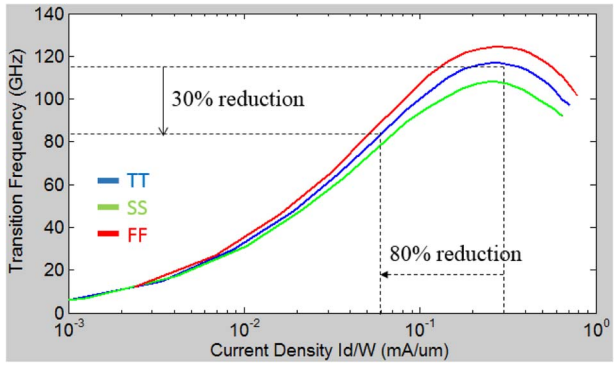

Fig. 6. Tradeoff between current density and f_T of a MOSFET ($W = 3.2\ \mu$m, $L = 120$ nm) in the 130-nm BiCMOS process.

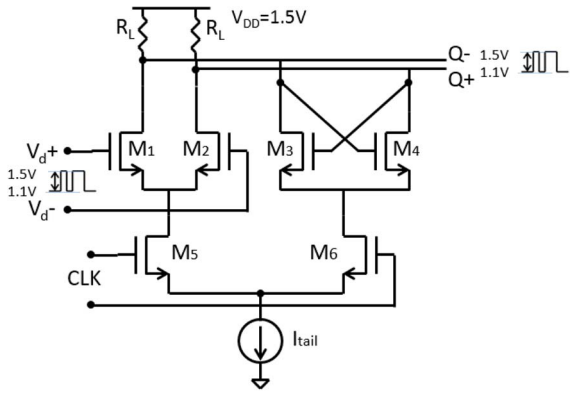

Fig. 7. Low-power CML D-latch circuit schematic.

D. 2^7-1 PRBS Generator

To provide a cost-effective means for reliable testing and verification of the modulator and the optical link, a 2^7-1 full-rate PRBS generator is designed and monolithically integrated. The block diagram of the PRBS generator circuit is shown in Fig. 5. One of the seven D-flip-flops (DFF) is designed with the "set" function to avoid the all-zero state. Traditional CML circuits are designed to achieve the current density at peak f_T to realize the best speed performance. As Fig. 6 shows, the current density at peak f_T for a MOSFET is approximately 0.3 mA/μm in the 130-nm BiCMOS process. It also shows that a reduction in current density by 80% to 0.06 mA/μm only reduces f_T by 30% at different process corners, resulting in substantial power savings. The deeply forward-biased HBT device that forms the backbone structure of the modulator device limits the overall transmitter bandwidth, and therefore, the sacrifice of DFF speed has a minimal effect on the overall transmitter circuit performance.

The CML D-latch topology is shown in Fig. 7. This latch employs MOSFET input transistors, which reduces the voltage drop by 0.2 V compared with bipolar transistors in the 130-nm BiCMOS process. For the same tail current, this voltage drop reduction yields considerable power savings as the power supply voltage V_{DD} is reduced accordingly.

TABLE II
COMPONENT VALUES OF CML LATCH

M_1/M_2[a]	M_3/M_4[a]	M_5/M_6[a]	R_L	I_{TAIL}
3.2 μm	3.2μm	3.2μm	1KΩ	400μA

[a]gate length are all 120nm

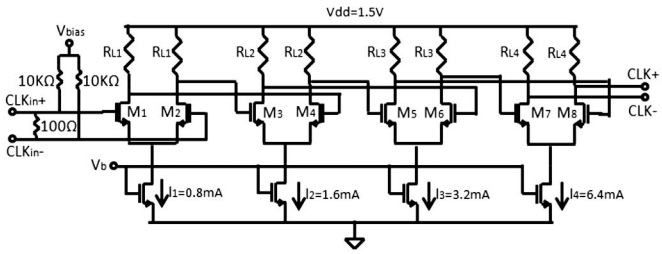

Fig. 8. Clock buffer circuit schematic.

TABLE III
COMPONENT VALUES OF CLOCK BUFFER

M_1/M_2[a]	M_3/M_4[a]	M_5/M_6[a]	M_7/M_8[a]	R_{L1}	R_{L2}	R_{L3}	R_{L4}
6.4 μm	12.8μm	25.3μm	50 μm	750Ω	378Ω	188Ω	100Ω

[a]gate length are all 120nm

With a 400-μA D-latch tail current and a 400-μA XOR gate, the total current of the $2^7 - 1$ PRBS generator is 6 mA. The load resistor R_L is selected to enable the output voltage swing of the master latch to fully switch the 400-μA tail current of the slave latch. A value of $R_L = 1$ KΩ is selected, which corresponds to an output voltage swing of 400 mV. Transistors M_1, M_2, M_5, M_6 are designed with the smallest gate width to minimize the parasitic capacitance while enabling full switching of the tail current with a 400-mV voltage swing at the gates. The cross-coupled regenerative pair M_3 and M_4 is designed to minimize its parasitic capacitance while setting $g_{m3,4}R_L$ larger than unity to guarantee the operation of the regenerative pair. All seven DFFs in this PRBS generator, which include a master and a slave D-latch, are designed with this feature. The CML XOR gate is similarly designed with the same tail current. The component values are summarized in Table II.

E. Clock Buffer

The clock buffer is used to amplify the input clock signal and drive all clock-triggered devices with the consideration of parasitic capacitance along clock distribution routing. As shown in Fig. 8, it is comprised of four stages of differential amplifiers. Each stage doubled the tail current and the differential pair size and halved the load resistance compared with its preceding stage. A 100-Ω resistance is connected between the differential inputs to provide 50-Ω impedance matching. The component values are summarized in Table III.

IV. CHIP FABRICATION AND EXPERIMENTAL RESULTS

The transmitter driver chip is fabricated in a commercial 130-nm SiGe BiCMOS process. Fig. 9 illustrates the microphotograph and the measurement setup of the chip. The total die area is 1920 μm $\times$ 1650 μm. Clock signal is supplied by the signal generator (Agilent E8247C) and converted into a differential signal by a wideband balun (Hyperlabs HL9402). The differential clock signal is supplied to the chip by a radio frequency (RF) probe (Cascade 40-GHz GSGSG) on the left side. Output signals from the PRBS generator and the preemphasis driver are measured by using RF probes (GGB 40-GHz GS) through the SGS pads at the bottom and GSG pads on the right side of the chip, respectively. The DC pads are wire bonded to an open-cavity QFN-52 package and mounted on an FR4 printed circuit board.

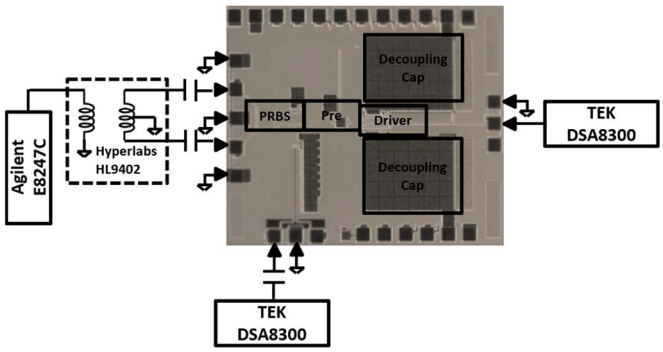

Fig. 9. Experimental test setup for RF probe measurements.

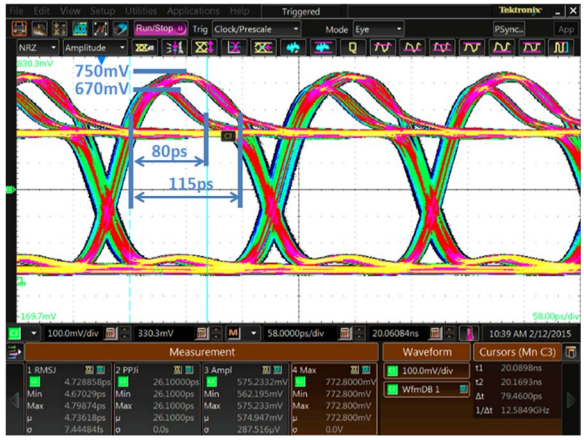

Fig. 10. 6-Gb/s eye diagram of the preemphasis driver output signal with 50-Ω load (weak and strong preemphasis overlap).

The eye diagram of the driver output with 50-Ω load and with weak preemphasis $(B_1B_0 = 00)$ and strong emphasis $(B_1B_0 = 11)$ are overlapped and shown in Fig. 10, highlighting the preemphasis peaking signal. With preemphasis, the amplitude is increased from 575 mV (nominal) to 670 mV (weak peaking) and to 750 mV (strong peaking). The peaking duration is 80 and 115 ps, respectively. The spectrum of the 6-Gb/s preemphasized PRBS signal is measured by a spectrum analyzer (Agilent E4408B). The 47-MHz tone spacing shown in Fig. 11 is equal to the data rate (6 Gb/s) divided by the pattern length (127), indicating that the 127-bit PRBS signal pattern is correctly achieved.

To demonstrate the expected performance of the driver circuit with the HBT-based modulator, the circuit is simulated using the electrical load model presented in Fig. 1. The simulated eye diagram at 6 Gb/s is shown in Fig. 12. As shown, the 0.95-V forward bias satisfies the design specification, which will guarantee a modulator extinction ratio of 5 dB. The -0.5-V reverse voltage for the base-to-emitter junction increases the discharge speed.

The total power consumption of this optical transmitter at the data rate of 6 Gb/s is 44.5 mW, including the PRBS generator (27 mW), the predriver (10.5 mW), and the preemphasis driver (7 mW). Table IV summarizes the performance comparison of

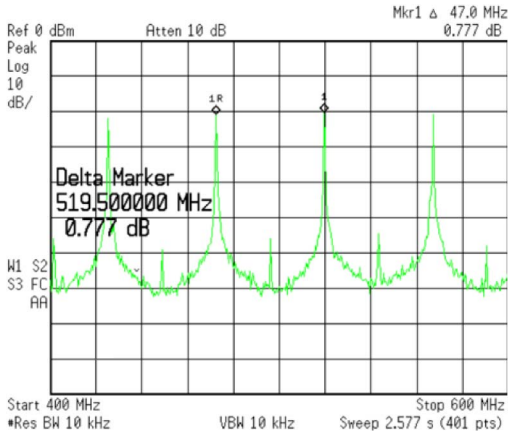

Fig. 11. 6-Gb/s preemphasis driver output signal zoomed-in spectrum at 50-Ω load.

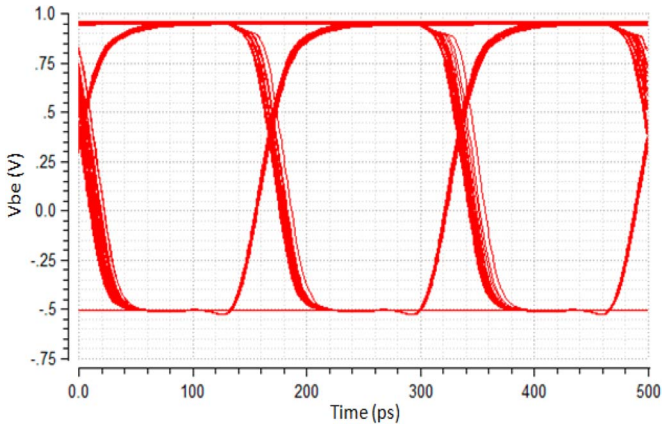

Fig. 12. Simulated 6-Gb/s eye diagram of the transmitter module driving an electrical load model of the HBT-based modulator.

TABLE IV
TRANSMITTER PERFORMANCE COMPARISON

Specification	[9]	[10]	[11]	This work
Modulator type	Ring	MZI	MZI	EAM
Optical BW	~0.2nm	NA	7.3nm	Not limited[a]
Data rate (Gbps)	2.5	20	10	6
Power (mW)	3.125[b]	90[c]	51[c]	44.5[d]
Extinction Ratio (dB)	3	NA	6-10	5
Modulator footprint (μm)	Radius: 15	L:480 W:375	L:200 W: 10	L:90 W: 2
Driving voltage (V)	1.5	1	1.8	0.95
Process	45nm SOI	40nm CMOS	Custom	130nm BiCMOS

a. The optical BW is not limited by modulator itself; b. accounts modulator and driver power consumption; c. only accounts modulator power consumption; d. accounts modulator, driver and PRBS generator

this work to recently published silicon optical transmitter designs. With implementation in a more cost-effective technology compared with the work in [9] and [10], this design renders good speed and power performance with excellent modulator footprint and low driving voltage, which are critical merits for the monolithic integration of an optical transmitter system as discussed in Section I. It is expected that with a better silicon process and higher power budget for the driver circuit, the speed of this transmitter system could be as high as tens of gigabits per second as claimed in [7]. By comparison, a ring modulator has excellent operating power because the resonant structure significantly enhances the free-carrier plasma effect. However, this is at the expense of narrow optical bandwidth, as discussed in Section I. In summary, with the merits of wide optical bandwidth, low power, outstanding small footprint, low driving voltage, and potential operating speed of tens of gigabits per second, the HBT-based carrier injection modulator provides a good solution for next-generation intra- or interchip optical interconnects.

V. CONCLUSION

The HBT optical modulator is a good candidate for monolithic integrated silicon optical interconnects due to its high speed and low driving voltage. This brief has presented a low-power high-speed optical transmitter module design for an HBT-based carrier injection EAM. The main features of the transmitter circuit are high speed, low power, and high efficiency. An ultralow-power $2^7 - 1$ PRBS generator is included on chip for high-speed testing. A configurable preemphasis feature improves speed performance. The chip is realized in a 130-nm SiGe BiCMOS process. Measurement results with a 50-Ω load demonstrate transmitter modulation up to 6 Gb/s with digitally tuned preemphasis strength.

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