Ultrashort SiGe Heterojunction Bipolar Transistor-Based High-Speed Optical Modulator

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***Abstract*—A graded base SiGe HBT optical modulator has high-speed, high optical modulation efficiency, small footprint. In this paper, we present our work in the design and modeling of an HBT optical modulator, its driver circuit and fabrication and integration. A high-efficient HBT electro-optical (EO) modulator with π phase-shift length of 22.6 μm is investigated. The speed of this modulator is calculated to be 30 Gb/s. To verify the functionality of HBT structure as an EO modulator, an 80 Gb/s serializer and driver with an HBT modulator is fabricated by the IBM 8HP BiCMOS process, which has much higher speed but lower modulation efficiency.**

***Index Terms*—Electro-optic (EO) modulators, heterojunction bipolar transistors (HBTs), intensity modulation, optical interconnections.**

I. Introduction

SILICON photonics has been a fast growing area of research in response to the demand of alterative interconnect technology in complex complementary metal-oxide semiconductor (CMOS) circuitry [1]. Optical interconnect emerged two decades ago as a possible candidate to replace copper-based electric interconnect. Up to date, the question is no longer whether to adopt optical interconnects but how to incorporate optical interconnects for intra- and interchip communication. A Si-based optical modulator with high-speed, small footprint, broadband and low power consumption is one of the key elements to enable optical interconnect for data center applications.

Si CMOS compatible electro-optic (EO) modulators have been extensively explored in the past few years. Since crystalline Si does not possess a linear EO effect, most Si EO modulators working at telecom wavelength utilize the free carrier plasma effect to manipulate the change the real and imaginary part of the refractive index. They are often termed electrorefractive and electroabsorption effects [2]. Mach–Zehnder interferometer (MZI) configuration is widely used to provide intensity modulation in which one arm acts as the phase shifter [3], [4]. Other than MZI, ring or disk resonator-based EO modulators have also been studied widely and gained much attention due to its small footprint [5], [6].

The electrical structures of current Si EO modulators are typically based on the MOS capacitor, PiN or PN structure. The PN type of modulator operates in reverse-bias mode in which the major carrier depletion gives rise to refractive index modulation. This type of device is fast, but requires long waveguide length to achieve π phase shift in an MZI configuration [3]. The PiN type of an EO modulator is based on injection and dissipation of minority carriers that are governed by the physics of minority carrier diffusion. The PiN-based optical modulator is typically slow due to finite minority carrier lifetime and built-in capacitance [4].

In this paper, we present a bipolar type of an EO modulator that has a highly doped emitter, narrow base, and a wide collector region. In an NPN type of heterojunction bipolar transistor (HBT), the free carriers, i.e., electrons inject into the base region and extend into the collector. The narrow base enables fast electron transit time, on the order of picosecond across the base. The electrons once they enter the collector region become majority carriers, and diffuse rapidly toward the subcollector. It is shown that the HBT is capable to operate at a data rate of hundreds of gigabyte per second [7].

In one of our earlier publications, we discussed the HBT EO modulators with an emphasis on switching speed [8]. In this paper, we present a modified design of the HBT with much higher optical modulation efficiency. Tradeoffs among the speed, device length, and extinction ratio are also discussed here. In the presented HBT design, as the emitter is doped to 10^{21} cm^{-3}, the injected electron density reaches a peak of 10^{20} cm^{-3} in the base region with a base–emitter (BE) voltage $V_{\rm be}$ of 1.1 V. The revised collector region increases the overlap between the carrier plasma and the optical mode, leading to an ultrashort optical modulator without using any resonant structure.

To verify the functionality of SiGe HBT structure as an EO modulator, an 80 Gb/s serializer, driver, and HBT modulator is fabricated using the IBM 8 HP process. The design of a serializer and an optical modulator driver circuit is also discussed in this paper. The modeling of the HBT EO modulator using IBM 8HP was discussed in our early work [8]. The serializer utilizes high-speed retiming MUXs (HRO-MUXs) and high-speed

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latching operation flip–flops (HLO F/Fs) technique to produce on-chip signal stream at 80 Gb/s for input data retiming. Three-stage buffered fan-out architecture is used to drive the optical modulator using a differential emitter-coupled logic (ECL) circuit. Postprocessing is carried on to thin down the backside of the HBT for optical mode confinement.

II. Modulation Efficiency by the Free Carrier Plasma Effect

A. Effectiveness of the Free Carrier Plasma Effect for Optical Modulation

The free carrier plasma effect in semiconductor materials is originated from the change of dielectric constant as a result of electric field perturbation in polarized solids. The real and imaginary parts of the dielectric constant (or refractive index) are related by Kramers–Kronig relation. The change in effective index Δn_{eff} of a waveguide is obtained by taking a weighted average of the optical irradiance $I(x,y)$ over the plane perpendicular to optical propagation

$$\Delta \text{n}_{\text{eff}} = \frac{\iint_{+\infty}^{-\infty} \Delta n(x,y) \times I(x,y) dxdy}{\iint_{+\infty}^{-\infty} I(x,y) dxdy} \tag{1}$$

where Δn is the change of refractive index of the material.

A Drude–Lorentz model or Soref's empirical equations [2] are commonly used in calculating the carrier density change-induced electrorefraction and electroabsorption effects in Si modulators. Soref and Bennett's paper [2] estimated L_π and optical loss tradeoff for a bulk crystalline Si under various carrier density modulation conditions. In this paper, we calculated the index modulation effect in a hypothetical nanowire waveguide that has a dimension of 300 × 300 nm. The choice of the waveguide dimension is such that it is compatible with the dimension of typical modulator devices. The π phase-shift length L_π is given by $L_\pi = \lambda_0/2\Delta n_{\text{eff}}$. We assume the index modulation is caused by the change of either electron or hole carrier concentration. The total number of majority carriers in plasma (M) that interact with the optical field in an L_π distance is $M = \Delta N_i \times \text{A} \times \text{L}_\pi$, where ΔN_i is the carrier density change either by electrons or holes, and A is the cross-sectional area of the waveguide, i.e., 300 × 300 nm. According to Soref's empirical equation [9], for light at $\lambda = 1.55$ μm, M is given by

$$M_e = \frac{\lambda_0 \times A}{2 \times 8.8 \times 10^{-22}} = 7.9 \times 10^7 \tag{2}$$

$$M_h = \frac{\lambda_0 \times A \times \Delta N_h^{0.2}}{2 \times 8.5 \times 10^{-18}} = 8.2 \times 10^3 \times \Delta N_h^{0.2} \tag{3}$$

where ΔN_h is the magnitude of hole concentration in the unit of cm^{-3}.

The nanowire waveguide has a negligible background doping, and has a cladding layer of SiO_2. We assume the carrier injection or depletion causes an electron density change of ΔN_e = 10^{18} cm^{-3}, 10^{19} cm^{-3}, and 1×10^{20} cm^{-3}, respectively. The effective index of the waveguide is calculated using a beam propagation method (BPM) mode solver from Rsoft. The optical loss of the optical wave passing through the waveguide in an L_π length is given by loss = $10\alpha_{\text{eff}} \times L_\pi / ln(10)$ where α_{eff} is the effective absorption coefficient for optical mode. Tables I and II summarize the simulation results. It is observed that the total number of majority carriers M is nearly a constant for all three doping levels for modulators based on electron carrier density change. The change of the refractive index due to hole density change does not follow linear relation, resulting in a varying total number of holes to induce π phase shift. This is in good agreement with our previous theoretical derivation. L_π is about 10 μm for carrier density change level at 10^{20} cm^{-3} for both electron and hole-induced EO modulators. The optical loss of unit length increases with the carrier density change; however, the total optical loss for electron-induced modulator is near a constant for all three ΔN_e conditions. The loss for hole-dominant EO modulator does increase with ΔN_h because M_h increases with hole density change.

TABLE I
Electron Plasma Effect for EO Modulators

ΔN_e	10^{18} cm^{-3}	10^{19} cm^{-3}	10^{20} hcm^{-3}
Δn_{eff}	0.00086	0.00857	0.08373
α_{eff}	0.00083 μm^{-1}	0.00825 μm^{-1}	0.0786 μm^{-1}
L_π	903.26μm	90.45 μm	9.26μm
M_e	8.13×10^7	8.14×10^7	8.33×10^7
Total optical loss	3.16dB	3.24dB	3.25dB

TABLE II
Hole Plasma Effect for EO Modulators

ΔN_h	10^{18} cm^{-3}	10^{19} cm^{-3}	10^{20} cm^{-3}
Δn_{eff}	0.002083	0.0131	0.080936
α_{eff}	0.00058 μm^{-1}	0.0058 μm^{-1}	0.0556 μm^{-1}
L_π	372.06 μm	59.16 μm	9.57 μm
M_h	3.35×10^7	5.32×10^7	8.62×10^7
Total optical loss	0.943 dB	1.49 dB	2.31 dB

B. Broadband Optical Modulator

Resonator-based EO modulators offer significant device size reduction and are able to mitigate the speed limitation posed by minority carrier diffusion in PiNs [5], [10]. The resonant cavity quality factor Q of these devices is typically greater than 10 000 [10]. The microring or disk modulator operates as a narrow bandpass filter owning to the sharp resonant peak. A small number of carrier plasma is sufficient to produce adequate index change in a waveguide for intensity switching. Inherently, it can be viewed that the optical wave is trapped in the ring or disk resonator characterized by the photon lifetime [11]. However, the drawback of high-Q resonator-based optical modulator has a high demand in fabrication accuracy and suffers from instability to temperature fluctuation. The use of temperature compensation circuits causes extra power consumption.

As the argument presented in Section II-A, optical field needs to interact with more or less a fixed number of carrier plasma to give rise to π phase shift in an MZI EO modulator. Thus, we envision a slow light structure in combination with a device that has high density of carrier plasma that would give rise to a broadband optical modulator with sufficiently small footprint as well as sufficiently small power consumption. The slow light structure might take the form of distributed feedback (DFB) gratings

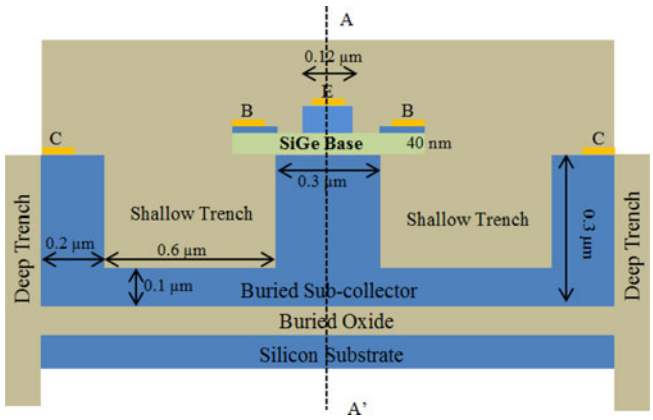

Fig. 1. Cross section of the proposed HBT structure.

or a photonic crystal waveguide to provide wave perturbation along the optical wave propagation direction. The PiN incorporated photonic crystal EO modulator demonstrates L_π of 80 μm, corresponding to length reduction of approximately one order of magnitude [12]. In our early publication, we reported a multisegment 1-D grating design that allows an L_π reduction of 2.4 times [13]. The DFB grating or the photonic crystal waveguide can be viewed as a series of localized resonators that allow the optical wave to interact with the free carrier plasma multiple times along its propagation. This is equivalent to recycle the use of the carrier plasma which results in light-wave interaction enhancement and modulator length reduction. It is worth noting that both grating and photonic crystal waveguides have finite spectrum bandwidth during which the slow light effect is present.

As the MZI length shrinks due to slow light effect, the total current reduces because the current density remains the same. For instance, if a size reduction of 10 times can be achieved, this will allow power consumption to reduce by a factor of 10. The HBT offers the ability to manipulate a large number of free carrier plasma at a very high speed. When it is used in combination with a slow light structure, a broadband, high speed, small footprint, and low power consumption optical modulator can be realized. With a more or less fixed quantity of charge, i.e., $\Delta Q = q \times M$ where q is the electron charge, and fixed switching voltage, i.e., ΔV = VBE = 1.1 V, the capacitance of the device, $C = \Delta Q / \Delta V$ does not decrease with the size reduction. Ultimately, the speed of the EO modulator is limited by the *RC* time constant of the device.

III. Ultrashort SiGe HBT Optical Modulator

A. Device Structure Design and Tradeoffs

The aim of the device design is to achieve an ultrashort optical modulator without using any resonant structure. The proposed HBT modulator structure is shown in Fig. 1. The emitter has a width of 0.12 μm with doping at 1×10^{21} cm^{-3} by arsenic. The thickness of graded SiGe base is 40 nm. The Ge mole fraction increases from 19% at the BE junction to 25% at the base–collector junction. The doping in base follows Gaussian profile with a peak doping level of 2×10^{19} cm^{-3} (Boron). The collector directly underneath the base region has a width of 0.3 μm and a height of 0.2 μm while the subcollector has a thickness of 0.1 μm. The collector region beneath the base is graded doped from 2×10^{18} cm^{-3} to 7×10^{18} cm^{-3} to avoid kirk effect. The buried subcollector is doped with arsenic of 5×10^{19} cm^{-3}, and the reach through region is doped with arsenic to 1×10^{20} cm^{-3}. The shallow trench and the buried oxide form the cladding layers of the waveguide. The width of shallow trench is 0.6 μm and is filled with SiO_2. The deep trenches are defined on each side of the device for electrical isolation.

The graded Ge composition in the base causes conduction band bending which gives rise to a built-in electric field on the order of 1 kV/cm. This electric field accelerates the carrier transit across the base [14]. Our simulation shows for the device designed earlier, the rise time for carrier plasma built up is reduced by 25% compared to Si BJT.

There are many tradeoffs that need to be considered in the HBT modulator design. We first consider the tradeoff between device doping and operation speed. Higher doping in the emitter, base, and collector region gives a smaller series resistance and thus higher operation speed. Also, high doping would lead to a high carrier injection level, which can be concluded from our previous reported work [8], [15]. However, higher doping, particularly in the collector region, leads to increasing optical propagation loss due to the free carrier plasma effect, which will affect the modulator's insertion loss.

Another design tradeoff happens in the geometry design. The width (0.3 μm) of the collector region underneath base and the thickness (0.1 μm) of the subcollector simultaneously affect both the speed and the optical modulation efficiency. In our early work, an 80 Gb/s HBT modulator was designed in which the thickness of the subcollector was chosen to be 0.4 μm [8]. The theoretical sheet resistance is estimated to be 668 Ω/sq and 166 Ω/sq for subcollector thickness of 0.1 and 0.4 μm, respectively. However, as we reduce the subcollector thickness, the center of the optical mode is push more toward the base and collector region where the free carrier plasma has the highest density. In addition, a thick subcollector may excite multiple modes in the rib waveguide which will result in a malfunction in an MZI EO modulator due to intermodal beat. Similar argument applies to the collector region directly underneath the base. A collector with reduced width increases the optical modulation efficiency but degrades the speed.

B. Device Modeling

The device is simulated by Sentaurus to get the carrier distribution during switching [16]. The hydrodynamic model is used, which considers the Poisson's equation, charge continuity equation and the temperature gradient simultaneously in the device. The Shockley–Read–Hall model and Auger recombination and surface recombination are considered to determine the carrier recombination behavior. The mobility models used in the simulation includes the Philips unified model (PHUMOB) and the velocity saturation model.

The HBT structure is switched between cutoff mode and saturation mode. This is realized by applying a dc bias of 0.5 V between BE junction and a square wave signal (0–1.1 V) to BE

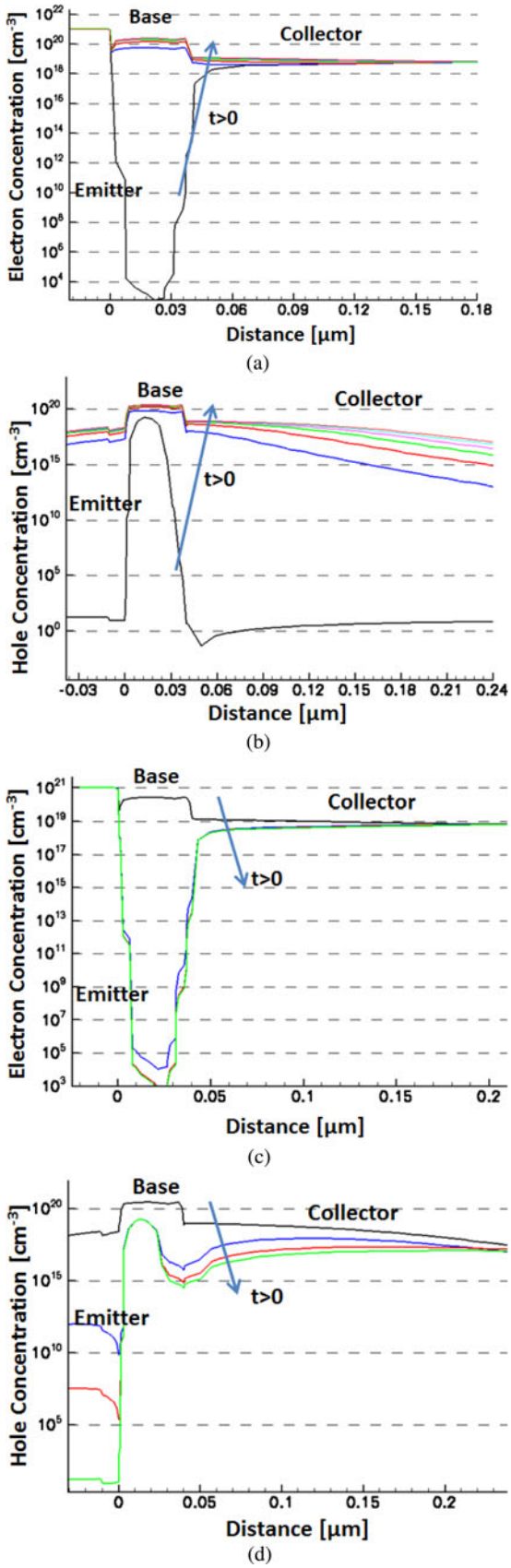

Fig. 2. (a) and (b) Time evolution of electron and hole distribution along centerlines during turn-ON period. (c) and (d) Time evolution of the electron and hole distribution along centerlines during turn-OFF period. The time step is 10 ps.

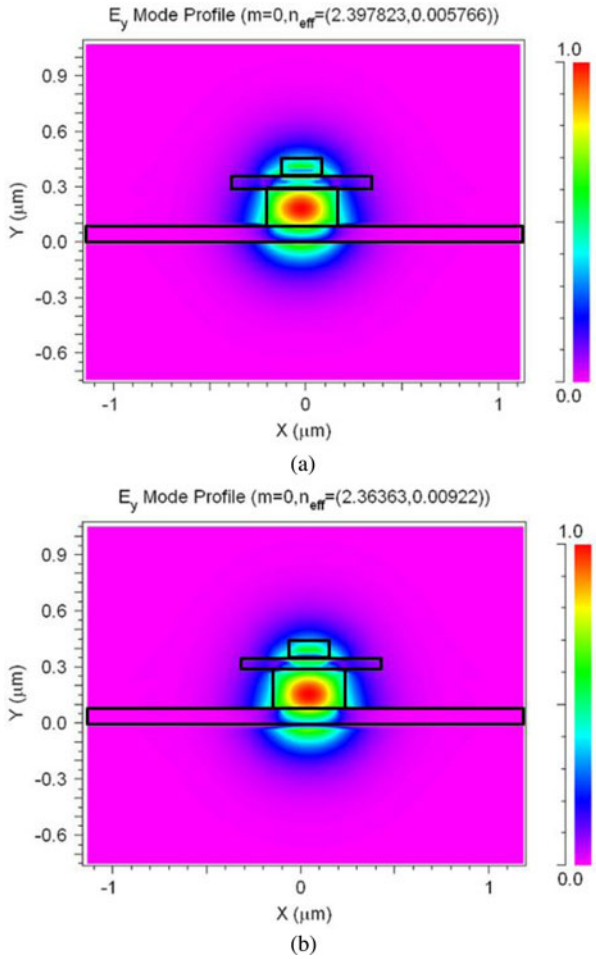

Fig. 3. (a) TM mode for OFF state. (b) TM mode for ON state.

junction. The rise time and fall time for this square signal is set to be 1 ps. The electron and hole distribution along the centerline (see AA′ in Fig. 1) are plotted in Fig. 2, which shows how carrier distribution changes during the switching process. These plots reveal that the electron injection in the base region reach its peak density at 2×10^{20} cm^{-3} and the hole injection to the collector region underneath the base and emitter region reaches 1×10^{19} cm^{-3}. It should be noted that the carrier injection level is higher than its doping level, i.e., high-level injection happens. Considering charge neutrality outside the depletion region, the injected electron density and the hole density should be on the same order of magnitude. This can be easily verified by comparing these plots in Fig. 2. The large carrier density change leads to excellent optical modulation efficiency.

C. Optical Simulation

The refractive index is calculated from carrier distribution according to Soref's equation [9]. The optical property is simulated by the BPM module in Rsoft. An optical wave at wavelength of 1.55 μm with Gaussian profile (beamwidth of 0.4 μm and height of 0.3 μm) is coupled to the HBT waveguide with an offset of 0.15 μm from the center. The optical field of TM polarization is shown in Fig. 3(a) when the device is in its "OFF" state. The

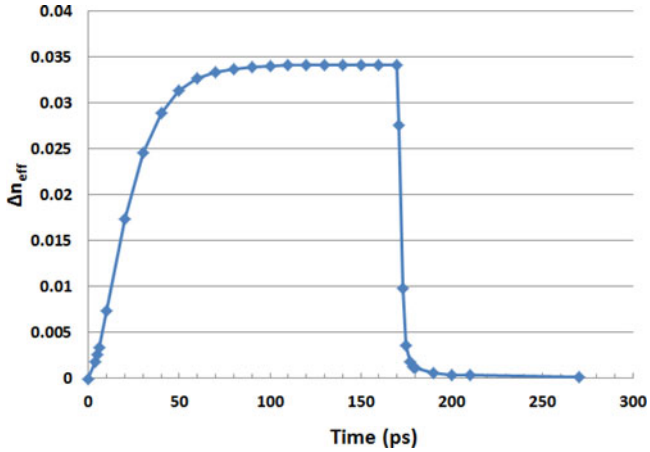

Fig. 4. Effective refractive index change as a function of time.

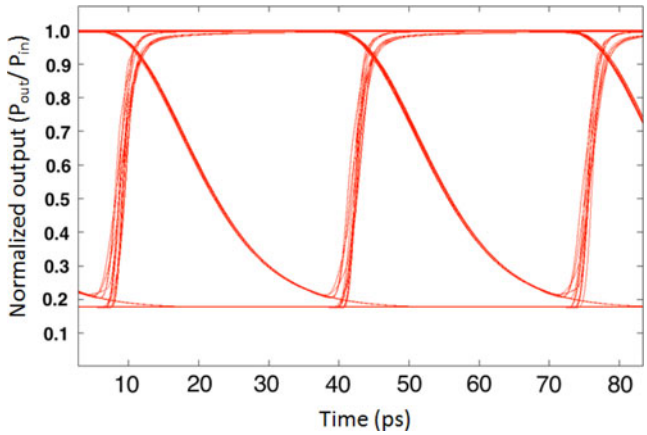

Fig. 5. Simulated eye diagram at 30 Gb/s of the output of the MZI HBT EO modulator.

figure shows that the high optical field region spans mostly in the base and the collector directly underneath the base, where a large carrier injection takes place during the switching. The large overlap between the carrier plasma region and the center of the optical field gives to excellent modulation efficiency. The optical field of the TM polarization of the device in its "ON" state is shown in Fig. 3(b). The effective refractive index for the "ON" and "OFF" state is calculated to be 2.36363+j0.00922 and 2.397823+j0.005766, respectively. From these data, L_π is extracted to be 22.6 μm as an EO modulator in MZI configuration. The insertion loss of device is defined as the optical wave propagation loss when there is no bias. The insertion loss of the aforementioned device is 4.6 dB. If we use PNP type of modulator, the insertion loss can be reduced.

The carrier distributions during switching process are recorded and converted to effective refractive index by BPM module in Rsoft. The effective refractive index change $\Delta n_{\rm eff}$ is plotted as a function of time in Fig. 4. It is observed from this plot that the rise time for this structure is much slower than fall time. An HBT structure of 22.6 μm long is incorporated in a symmetric MZI as a phase shifter. A 2^7-1 pseudorandom binary sequence (PRBS) signal, which switches between 0 and 1.1 V, is applied to the BE junction of the HBT. The simulated eye diagram of the normalized output $P_{\rm out}/P_{\rm in}$ of this MZI structure at 30 Gb/s is plotted Fig. 5. The eye diagram reveals that the rise time and fall time is different, which agrees with the results shown in Fig. 4. This problem could be solved by using a preemphasis technique in the driver circuits [4]. In [4], a speed increase by four times is observed with a preemphasis circuit technique. Significant improvement of speed is also expected for the HBT EO modulator that was discussed here if preemphasis technology is employed.

Using the approach in [15], the dynamic power consumption is calculated to be 5.3 pJ/bit for a 30 Gb/s signal. IBM reported a PiN-based EO modulator that has a power consumption of 5 pJ/bit [4], which is compatible to this HBT optical modulator as both are carrier injection type modulators. When this device is used as an electroabsorption modulator, the length needed to get 10 dB extinction ratio calculated to be 82 μm.

The power budget of Si modulators for data center applications is less than 100 fJ/bit. When a slow light structure, such as photonic crystal waveguide is incorporated in both arms of the MZI, an L_π reduction of 10 times was demonstrated [12]. Using IBM 9HP SiGe technology [7], a theoretical investigation of an EO modulator shows a data rate of 250 Gb/s. Let N be the L_π reduction ratio, and BW the data rate of the modulator. The total power consumption for a slow light incorporated EO modulator is P.C. $= P_t/(N\times{\rm BW})$, where P_t is the total power consumption of an HBT structure. For a 250 Gb/s HBT SiGe EO modulator with slow light structure incorporated, the power consumption is expected to meet the 100 fJ/bit requirement. The key to meet the power budget is the combination of the L_π length reduction and speed increase.

To verify the functionality of the HBT structure and the accuracy of our simulation, an HBT modulator and its driver circuit are fabricated using the IBM 8HP SiGe process. The next two sections of this paper will discuss the circuit design, device fabrication, and postprocessing of a fast HBT EO modulator.

IV. Driver Circuit Design

There are a few challenges concerning high data rate SiGe bipolar EO modulator drivers. First, it is the difficulty in creating 80 Gb/s data stream. Second, the optical modulator is an ultralong transistor compared to typical HBTs used for analog circuit applications. It requires large amount of current therefore wider interconnecting wires from the driver to the modulator. This ultimately increases the loading capacitance and decreases the performance bandwidth. The EO modulator also requires larger than normal (>300 mV) output voltage swing. This effectively requires a larger switching current through the emitter-coupled pair to achieve sufficient small rise and fall times. Larger currents also lead to higher power dissipation, heat density, and device junction temperature which results in reduced electron mobility, thus degrading the overall performance of the optical modulator and the circuit subsystem. To manage heat density, area of the circuitry would need to increase, thus increasing the interconnecting wires to the modulator.

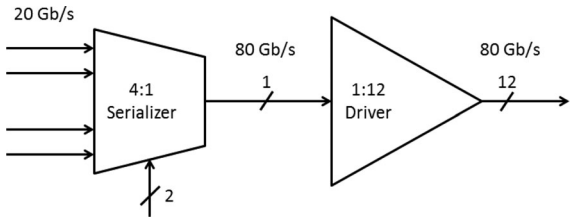

Fig. 6. Block diagram of the EO driver system.

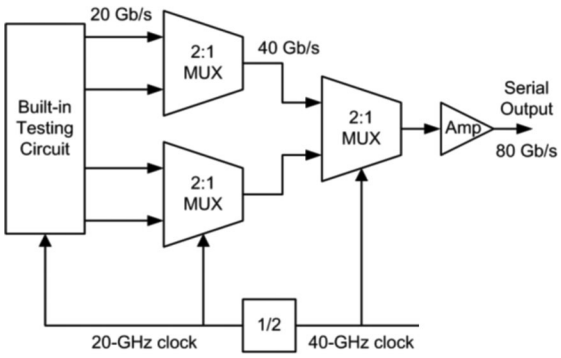

Fig. 7. Block diagram of the 4:1 half-rate serializer.

Using IBM's 8HP 0.13-μm SiGe bipolar process, an 80 Gb/s EO circuit system has been developed using a supply voltage of 3.4 V. Shown in Fig. 6, the circuit system consists of a 4:1 80 Gb/s serializer and a fan-out driver array. The driver circuit receives four parallel input data streams at 20 Gb/s and 4:1 multiplexed to 80 Gb/s using the selector frequencies of 20 and 40 GHz. A single differential output bit rate of 80 Gb/s is then buffered with a three-stage fan-out driver array producing 12 single-ended 80 Gb/s bit rates for the base of the EO modulator.

A. Serializer

Up to date, serializers using 0.13-μm BICMOS technology have been shown to operate at speeds in excess of 80 Gb/s [17]. Shown in Fig. 7, the serializer uses the half-rate clocking scheme where a 40 GHz clock is required for the 4:1 multiplexor (MUX) to produce an output data rate of 80 Gb/s. The serializer consists of a built-in testing circuit, three 2:1 MUXs, an output amplifier, and a clock path. The clock path incorporates an input pad receiver, a frequency divider, and clocking buffers.

For the lack of a high-speed multichannel signal generator, a testing data generator is built on the IC chip providing 4 bits of parallel input data to the 4:1 half-rate serializer. The testing data generator is a linear feedback shift register which can generate a 4-bit wide pseudorandom bit sequence data with a 2^7–1 pattern. The MUX incorporates three 2:1 HRO-MUXs. The HRO-MUX incorporates HLO F/Fs for input data retiming.

The five-latch MUX is one of the most widely used 2:1 MUX design [18], [19]. Pairs of latches can be combined as HLO F/Fs yielding the block diagram in Fig. 8.

The first pair of F/Fs is used to receive the two data paths, D_0 and D_1, and act as to retime the data bit paths. The odd pair latch producing Q_2 is used to offset the data channel Q_1 by a half-clock cycle in the time domain compared with the other

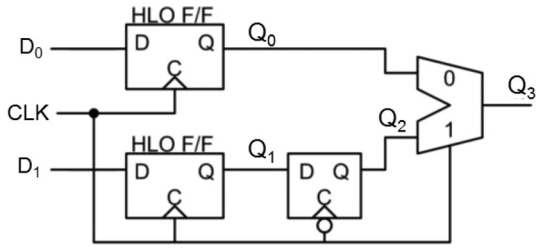

Fig. 8. Simplified block diagram of the HRO-MUX.

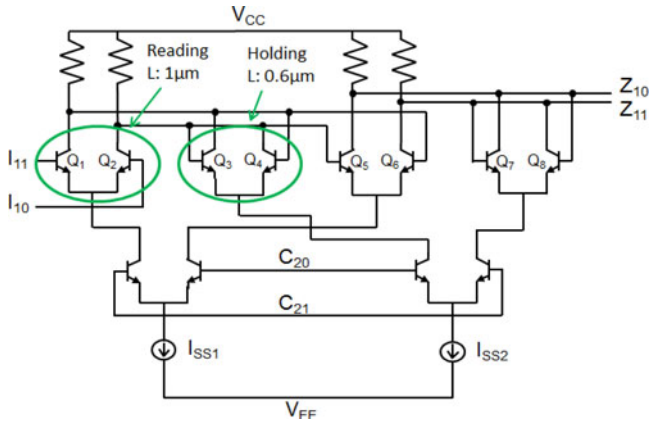

Fig. 9. Schematic diagram of a HLO F/F.

data channel Q_0 in order to avoid simultaneous data transitions between both channels. The selector selects the data channel Q_0 on low clock input while alternatively selecting data channel Q_2 on a high clock input.

The HLO F/F is known to operate about 30% faster than conventional master–slave (MS) F/F [20]. Although there might exist a slightly faster F/F today, HLO F/F is very attractive due to the fact that it uses the same number of transistors and contains the same architectural simplicity as a conventional MS F/F. Architectural simplicity is critical in the design of very high-speed differential circuits because simplicity leads to symmetry. A layout mismatch in a symmetric differential circuit can cause a duty cycle mismatch in its differential signal. Also, symmetry leads to compact layout design, reduction in interconnect wire capacitance, and an improvement to operation performance which can be compensated with a reduction in bias current, thus reducing the overall power consumption of the circuit.

The HLO F/F has two different features compared with a conventional MS F/F: asymmetric transistor sizes and optimized tail currents. The topological configuration of an asymmetric D-latch is identical with a conventional D-latch, but the size of the holding transistor pair is smaller than the reading transistor pair. The smaller transistor size leads to less input capacitance of the holding circuit. Therefore, the holding state time becomes shorter than the reading state time. Consequently, the total delay time in the latching circuit can be reduced. A pair of asymmetric latches can be combined, triggering on alternate values of the clock to make up an asymmetric F/F. The architecture can be improved further by using a cross tail-current path at the second current-mode logic level to achieve peak cutoff frequency f_t performance of all transistor trees as seen in Fig. 9. The differential

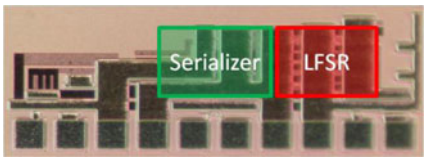

Fig. 10. Micrograph of 4:1 Serializer IC.

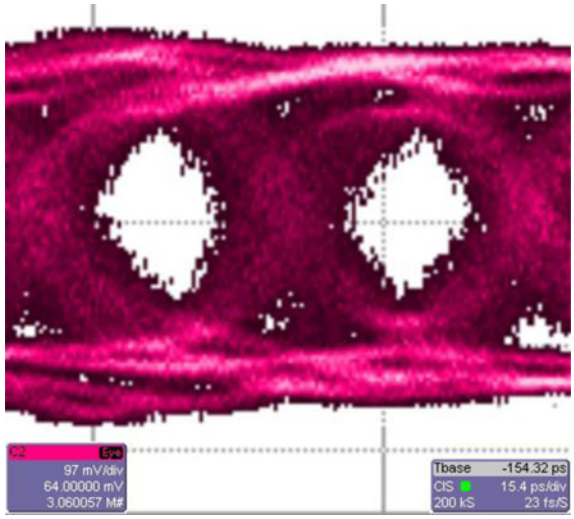

Fig. 11. Measured eye diagram of the modulator serializer at 78 Gb/s.

pairs of Q_3-Q_4 and Q_5-Q_6 are reading circuits while the differential pairs of Q_3-Q_4 and Q_7-Q_8 are holding circuits. The emitter size ratio between the reading and the holding circuits is heuristically decided to be 10/6 [20]. Consequently, HLO F/Fs require 20% less current, ultimately reducing the serializer circuit power consumption by about 7%. A micrographic photo of the serializer circuit is shown in Fig. 10. The eye diagram of the serializer is measured and shown in Fig. 11 with a 2^7–1 PRBS signal. The testing results show that the serializer can work up to 78 Gb/s.

B. EO Modulator Driver Circuit

The EO modulator driver circuit is a three-stage fan-out buffer array where each buffer drives no more than four other buffers. The driver circuit receives one differential input data path and drives 12 single-ended output connections to the base of the modulator device.

All three stages of drivers use the differential ECL configuration in Fig. 12. The input data path is converted from a level 1 to a level 3 via double emitter follower (EF) pairs. The level 3 signal enters the ECL pair, Q_1 and Q_2, with a pull-up resistor pair, R_{C2}, to provide the amplified voltage. R_{E1} and R_{E2} mainly sets the bias current through the EF pairs but can also act as a preamplifying stage. RC1 is used mainly to prevent collector–emitter voltage break down.

Q_1 and Q_2 of the first two stages of the driver array have to be sized correctly to drive the fan-out configuration. At the third and final stage, each driver only has to drive one BJT device of the EO modulator. Thus, sizing of Q_1 and Q_2 at the final stage can be designed slightly smaller than the first two stages. At the final stage, a single-end output is created by using one of the Z outputs and leaving the other floating.

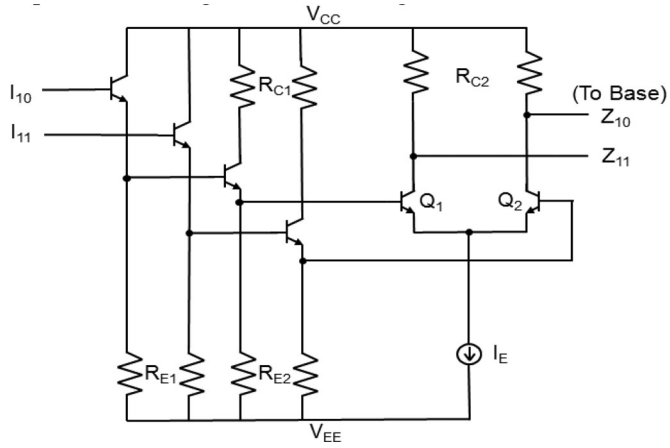

Fig. 12. Schematic diagram of the driver circuit.

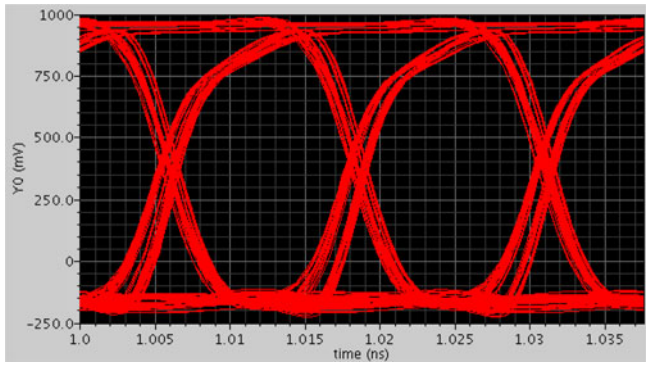

Fig. 13. Output eye diagram of driver output with the HBT modulator as load.

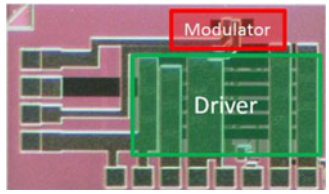

Fig. 14. Micrograph of the EO-Modulator IC.

The base terminal of the HBT modulator is the output port of the driver, while the emitter terminal of the EO modulator is connected to ground. The driver output is taken at V_{BE} with the EO modulator as the load. The simulated eye diagram of V_{BE} is shown in Fig. 13 using a PRBS signal of 2^7–1 bits.

The optical modulator used in this research consists of 12 HBTs, and each of them has an emitter length of 5 μm. A micrographic photo of the modulators and the driver circuits on chip is shown in Fig. 14.

V. Postfabrication and Integration

Postprocessing of the HBT die includes bonding the sample to a Si carrier wafer, thinning the die to roughly 25 μm, coating of SiO_2 to provide under cladding to the HBT waveguide, and removal of the carrier wafer. The HBT die has a total thickness

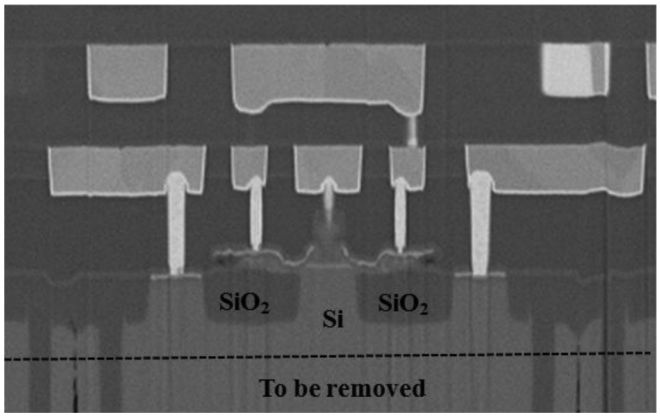

Fig. 15. SEM cross section of SiGe 8HP production line HBT modulator die before SiO_2 under cladding deposition.

of 300 μm. The Si substrate has a thickness of 270 μm and the epilayer of the HBT is about 6 μm thick. The die also consists of eight layers of passivation for electrical interconnects among different levels of metal lines. This passivation and interconnect layer stack is around 24 μm thick. When the die is thinned from the backside, the etch stops at 0.4μm of the epilayer that primarily consists of the collector of the device.

To thin the backside of the HBT die, it is first top-side bonded to a diced Si carrier wafer by a thick layer of SU-8 polymer. The SU-8 polymer is resistant to chemical processing and compatible with Bosch deep reactive ion etching (DRIE) processing methods [21]. After bonding, the backside of the HBT die is etched by an inductively coupled plasma DRIE process. A gas mixture of SF_6 and O_2 is used to etch the crystalline Si at a rate of approximately 10 μm/min. After the Si substrate is thinned to a thickness of 0.4 μm so that a subcollector region remains, we then deposit 2 μm of silicon dioxide (SiO_2) by plasma-enhanced chemical vapor deposition (PECVD). This SiO_2 layer is under the cladding layer of the optical waveguide. Next, a thick ($>$100 μm) SU-8 polymer layer is spin coated and hardened onto the SiO_2 under cladding layer to provide stability to the thinned HBT die. The HBT die is then removed from the original carrier wafer to allow electrical probe access to the top side of the HBT die.

To prove the effectiveness in using the HBT from SiGe 8HP, production line for optical modulator, focused ion beam milling is performed to show the cross-sectional view of the die, as shown in the SEM image in Fig. 15. The shallow trench and the isolation layer, together with the PECVD SiO_2 form the cladding to confine the optical wave within the base and collector region.

VI. Conclusion

The use of SiGe HBT for fast EO modulators is discussed in this paper, and an ultrashort HBT modulator design is presented. The π phase-shift length is 22.6 μm in an MZI configuration. The device bandwidth is estimated to be 30 Gb/s, and a larger bandwidth can be achieved if preemphasis technology is employed. And to verify the functionality of the HBT structure as an EO modulator, an 80 Gb/s driver circuits and SiGe HBT modulator are fabricated using the IBM 8HP SiGe bipolar process. A 78 Gb/s serializer is demonstrated experimentally. Postprocessing to thin down the HBT die is discussed to produce an HBT waveguide.

References

[1] G. T. Reed, *Silicon Photonics: The State of the Art*. New York: Wiley, 2008.
[2] R. A. Soref and B. R. Bennett, "Electrooptical effect in Silicon," *IEEE J. Quantum Electron.*, vol. QE-23, no. 1, pp. 123–129, Jan. 1987.
[3] L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "40 Gbit/s silicon optical modulator for high-speed applications," *Electron. Lett.*, vol. 43, no. 22, pp. 1196–1197, Oct. 2007.
[4] W. M. J. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," *Opt. Exp.*, vol. 15, no. 25, pp. 17106–17113, Dec. 2007.
[5] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon microring silicon modulators," *Opt. Exp.*, vol. 15, pp. 430–436, 2007.
[6] M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow power silicon microdisk modulators and switches," in *Proc. IEEE Group IV Photon. Conf.*, Sep. 2008, pp. 4–6.
[7] T. Neogi, G. Niu, D. Connelly, J. D. Cressler, Z. R. Huang, and J. F. McDonald, "Design of a 250-Gbit/s SiGe HBT electrooptic modulator," *IEEE Photon. J.*, vol. 3, no. 5, pp. 897–914, Oct. 2011.
[8] T. Neogi, S. Deng, J. Novak, J. Guo, R. Clarke, M. R. LeRoy, J. F. McDonald, and Z. Rena Huang, "Modeling and analysis of an 80 Gb/s SiGe HBT electro-optic modulator," *IEEE Photon. J.*, vol. 3, no. 1, pp. 42–56, Feb. 2011.
[9] R. A. Soref and B. R. Bennett, "Kramers-Kronig analysis of electro-optical switching in silicon," *Proc. SPIE*, vol. 704, pp. 32–37, 1986.
[10] L. Zhou and A. W. Poon, "Silicon electro-optic modulators using p-i-n diodes embedded 10-micron-diameter microdisk resonators," *Opt. Exp.*, vol. 14, no. 15, pp. 6851–6857, 2006.
[11] J. T. Verdeyen, *Laser Electronics*, 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 2000, ch. 6.
[12] L. Gu, W. Jiang, X. Chen, and R. T. Chen, "Physical mechanism of p-i-n-diode-based photonic crystal silicon electrooptic modulators for gigahertz operation," *IEEE J. Sel. Top. Quantum Electron.*, vol. 14, no. 4, pp. 1132–1139, Jul./Aug. 2008.
[13] S. Deng and Z. Rena Huang, "Design and analysis of transmission enhanced multi-segment grating in a MZI configuration for slow light applications," *Opt. Exp.*, vol. 19, no. 8, pp. 3872–3884, 2011.
[14] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003.
[15] S. Deng, T. G. Neogi, J. Novak, J. F. McDonald, and Z. Rena Huang, "Design of a short electro-optic modulator based on SiGe HBT structure," *Opt. Exp.*, vol. 18, no. 3, pp. 1994–2001, Feb. 2010.
[16] [Online]. Available: http://www.synopsys.com/tools/tcad/devicesimulation/pages/sentaurusdevice.aspx.
[17] M. Meghelli, "132-Gb/s 4:1 multiplexor in 0.13-um SiGe-Bipolar technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2403–2407, Dec. 2004.
[18] T. O. Dickson, E. Laskin, I. Khalid, R. Beerkens, J. Xie, B. Karajica, and S. P. Voinigescu, "An 80-Gb/s 231-1 pseudorandom binary sequence generator in SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2735–2745, Dec. 2005.
[19] T. Masuda, K. Ohhata, N. Shiramizu, E. Ohue, K. Oda, R. Hayami, H. Shimamoto, M. Kondo, T. Harada, and K. Washio, "SiGe-HBT-based 54-Gb/s 4:1 multiplexer IC with full-rate clock for serial communication systems," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 791–795, Mar. 2005.
[20] K. Murata, T. Otsuji, M. Ohhata, M. Togashi, E. Sano, and M. Suzuki, "A novel high-speed latching operation flip-flop (HLO-FF) circuit and its application to a 19 Gb/s decision circuit using 0.2 μm GaAs MESFET," in *Proc. GaAs IC Symp. Tech. Dig.*, 1994, pp. 193–196.
[21] S. K. Sampath, L. St. Clair, X. Wu, D. V. Ivanov, Q Wang, C Ghosh, and K. R. Farmer, "Rapid MEMS prototyping using SU-8, wafer bonding and deep reactive ion etching," in *Proc. 14th Biennial Univ./Gov./Ind. Microelectron. Symp.*, 2001, pp. 158–161.

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