Crossbar on the C8051F120

EVB Pin:

	P0								P1								P2								P3								Crossbar Register Bits
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
TX0	●																																UART0EN: XBR0.2
RX0		●																															
SCK	●		●																														SPI0EN: XBR0.1
MISO		●		●																													
MOSI			●		●																												
NSS				●		●	NSS is not assigned to a port pin when the SPI is placed in 3-wire mode																										
SDA	●		●	●	●	●	●																										SMB0EN: XBR0.0
SCL		●		●	●	●	●	●																									
TX1	●		●	●	●	●	●	●	●																								UART1EN: XBR2.2
RX1		●		●	●	●	●	●	●	●																							
CEX0	●		●	●	●	●	●	●	●	●	●																						PCA0ME: XBR0.[5:3]
CEX1		●		●	●	●	●	●	●	●	●	●																					
CEX2			●		●	●	●	●	●	●	●	●	●																				
CEX3				●		●	●	●	●	●	●	●	●	●																			
CEX4					●		●	●	●	●	●	●	●	●	●																		
CEX5						●		●	●	●	●	●	●	●	●	●																	
ECI	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●																ECI0E: XBR0.6
CP0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●															CP0E: XBR0.7
CP1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●														CP1E: XBR1.0
T0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●													T0E: XBR1.1
/INT0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●												INT0E: XBR1.2
T1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●											T1E: XBR1.3
/INT1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●										INT1E: XBR1.4
T2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●									T2E: XBR1.5
T2EX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●								T2EXE: XBR1.6
T4	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●							T4E: XBR2.3
T4EX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						T4EXE: XBR2.4
/SYSCLK	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●					SYSCKE: XBR1.7
CNVSTR0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				CNVSTE0: XBR2.0
CNVSTR2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			CNVSTE2: XBR2.5
						ALE	/RD	/WR	AIN2.0/A8	AIN2.1/A9	AIN2.2/A10	AIN2.3/A11	AIN2.4/A12	AIN2.5/A13	AIN2.6/A14	AIN2.7/A15	A8m/A0	A9m/A1	A10m/A2	A11m/A3	A12m/A4	A13m/A5	A14m/A6	A15m/A7	AD0/D0	AD1/D1	AD2/D2	AD3/D3	AD4/D4	AD5/D5	AD6/D6	AD7/D7	
									AIN2 Inputs/Non-muxed Addr H								Muxed Addr H/Non-muxed Addr L								Muxed Data/Non-muxed Data								

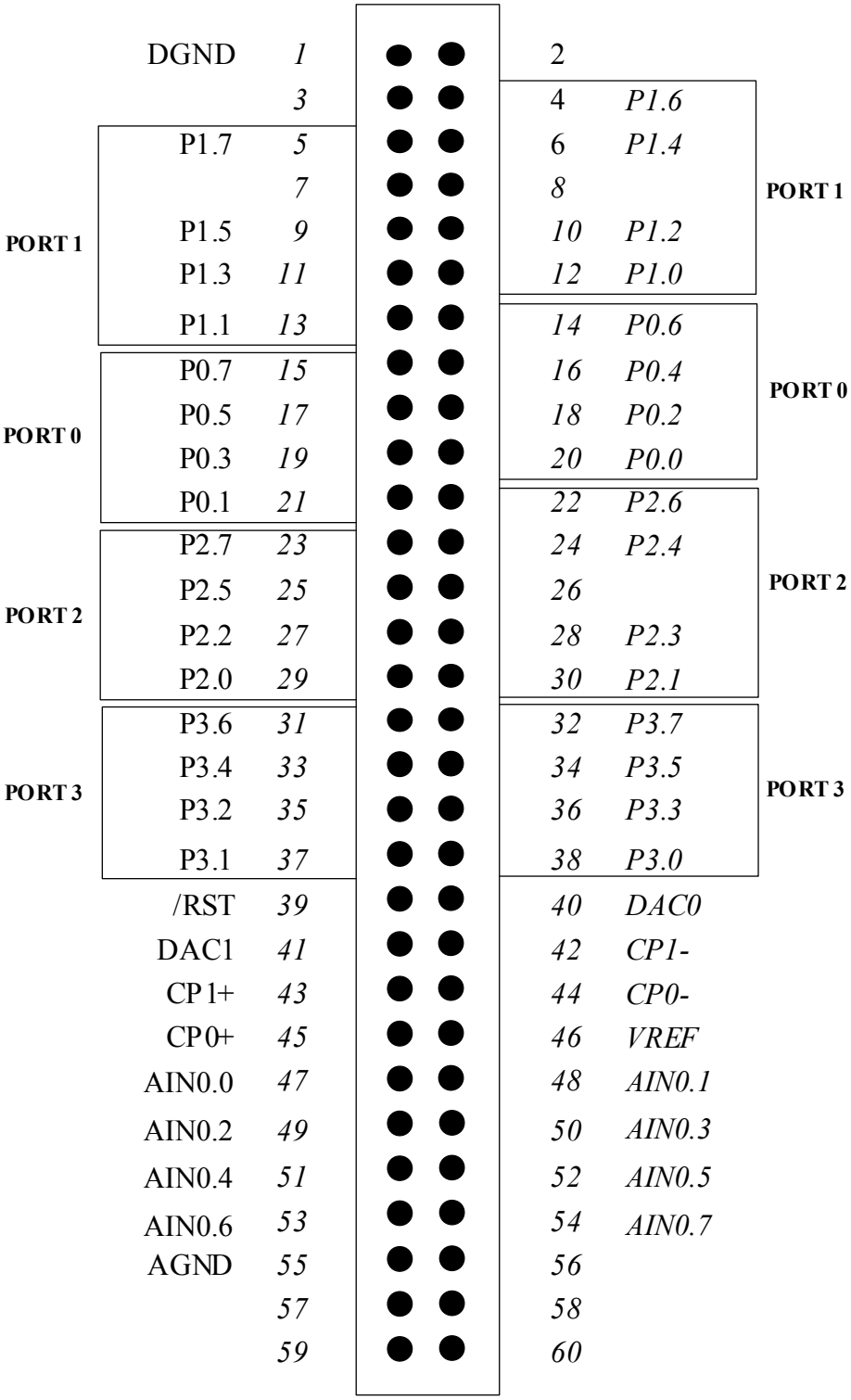
Priority Crossbar Decode Table

	7	6	5	4	3	2	1	0
XBR0 Register	**CP0E** Comparator 0 Output Enable	**ECI0E** PCA0 Exter-nal Counter Input Enable	**PCA0ME** PCA0 Module I/O Enable			**UART0EN** UART0 I/O Enable	**SPI0EN** SPIO Bus I/O Enable	**SMB0EN** SMBus I/O Enable
Priority Order	7	6	5			1	2	3

5	4	3	
0	0	0	No CEXn
0	0	1	CEX0
0	1	0	CEX0, CEX1
0	1	1	CEX0, CEX1, CEX2
1	0	0	CEX0, CEX1, CEX2, CEX3
1	0	1	CEX0, CEX1, CEX2, CEX3, CEX4

XBR0: Port I/O Crossbar Register 0 and Priority Order

C8051 EVB Port Connector 1



C8051 EVB Port Connector 2