Advance Information
24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56303 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high performance, single clock cycle per instruction engine providing a twofold performance increase over Motorola’s popular DSP56000 core family while retaining code compatibility. Significant architectural enhancements to the DSP56300 core family include a barrel shifter, 24 bit addressing, instruction cache, and DMA. The DSP56303 offers 66/80 MIPS using an internal 66/80 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low power dissipation, enabling a new generation of wireless, telecommunications, and multimedia products.

Figure 1  DSP56303 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.
DSP56303 FEATURES

- High performance DSP56300 core
  - 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
  - Object code compatible with the DSP56000 core
  - Highly parallel instruction set
  - Fully pipelined 24 x 24-bit parallel multiplier-accumulator
  - 56-bit parallel barrel shifter
  - 24-bit or 16-bit arithmetic support under software control
  - Position independent code support
  - Addressing modes optimized for DSP applications
  - On-chip instruction cache controller
  - On-chip memory-expandable hardware stack
  - Nested hardware DO loops
  - Fast auto-return interrupts
  - On-chip concurrent six-channel DMA controller
  - On-chip Phase Lock Loop (PLL) and clock generator
  - On-Chip Emulation (OnCE™) module
  - JTAG Test Access Port (TAP)
  - Address tracing mode reflects internal accesses at the external port

- On-chip memories
  - Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable:

<table>
<thead>
<tr>
<th>Instruction Cache</th>
<th>Switch Mode</th>
<th>Program RAM Size</th>
<th>Instruction Cache Size</th>
<th>X Data RAM Size</th>
<th>Y Data RAM Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>disabled</td>
<td>disabled</td>
<td>4096 × 24-bit</td>
<td>0</td>
<td>2048 × 24-bit</td>
<td>2048 × 24-bit</td>
</tr>
<tr>
<td>enabled</td>
<td>disabled</td>
<td>3072 × 24-bit</td>
<td>1024 × 24-bit</td>
<td>2048 × 24-bit</td>
<td>2048 × 24-bit</td>
</tr>
<tr>
<td>disabled</td>
<td>enabled</td>
<td>2048 × 24-bit</td>
<td>0</td>
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<td>1024 × 24-bit</td>
<td>3072 × 24-bit</td>
<td>3072 × 24-bit</td>
</tr>
</tbody>
</table>

- 192 × 24-bit bootstrap ROM
• Off-chip memory expansion
  – Data memory expansion to two 256 K x 24-bit word memory spaces
  – Program memory expansion to one 256 K x 24-bit word memory space
  – External memory expansion port
  – Chip select logic requires no additional circuitry to interface to SRAMs and SSRAMs
  – On-chip DRAM controller requires no additional circuitry to interface to DRAMs
• On-chip peripherals
  – 8-bit parallel Host Interface (HI08), ISA-compatible bus interface, providing a cost-effective solution for applications not requiring the PCI bus
  – Two Enhanced Synchronous Serial Interfaces (ESSI)
  – Serial Communications Interface (SCI) with baud rate generator
  – Triple timer module
  – Up to thirty-four programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled
• Reduced power dissipation
  – Very low power CMOS design
  – Wait and Stop low power standby modes
  – Fully-static logic, operation frequency down to DC
  – Optimized power management circuitry

TARGET APPLICATIONS

The DSP56303 is intended for use in telecommunication applications, such as multi-line voice/data/fax processing, videoconferencing, audio applications, control, and general digital signal processing.
PRODUCT DOCUMENTATION

The three manuals listed in Table 1 are required for a complete description of the DSP56303 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

Table 1  DSP56303 Documentation

<table>
<thead>
<tr>
<th>Document Name</th>
<th>Description of Contents</th>
<th>Order Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP56300 Family Manual</td>
<td>Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set</td>
<td>DSP56300FM/AD</td>
</tr>
<tr>
<td>DSP56303 User’s Manual</td>
<td>Detailed description of DSP56303 memory, peripherals, and interfaces</td>
<td>DSP56303UM/AD</td>
</tr>
<tr>
<td>DSP56303 Technical Data</td>
<td>DSP56303 pin and package descriptions, and electrical and timing specifications</td>
<td>DSP56303/D</td>
</tr>
</tbody>
</table>

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