M68HC12A4EVB
EVALUATION BOARD
USER'S MANUAL

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides the necessary information for using the M68HC12A4EVB Evaluation Board (the EVB), an evaluation, debugging, and code-generation tool for the MC68HC812A4 Microcontroller Unit (MCU) devices. The manual includes:

- A general description of the EVB
- Configuration and setup instructions
- Startup and operating instructions
- Detailed descriptions of the operating firmware's command set
- A detailed hardware-reference section
- Appendices containing reference data

Additional reference items, such as schematic diagrams and parts lists, are shipped as part of the EVB package.

1.2 GENERAL DESCRIPTION AND FEATURES

The EVB is an economical tool for designing and debugging code for, and evaluating the operation of, the MC68HC12 MCU family. By providing the essential MCU timing and I/O circuitry, the EVB simplifies user evaluation of prototype hardware and software.

The board consists of an 8-inch by 8-inch multi-layer printed circuit board (PCB) that provides the platform for interface and power connections to the MC68HC812A4 MCU chip, which is installed in a production socket.

Figure 1-1 shows the EVB’s layout and locations of the major components, as viewed from the component side of the board.

The block diagram in Figure 1-2 depicts the logical relationships and interconnections within the EVB and with external equipment.

Hardware features of the EVB include:

- Power, ground, and 4 signal planes
- Single-supply +3 to +5 Vdc power input (J6)
- Two RS-232C interfaces
- Two memory sockets populated with two 32Kx8 EPROMs (U7, U9A), containing the D-Bug12 monitor program
- Two memory sockets populated with two 8Kx8 SRAMs (U4, U6A)
- Support for up to 1 MB of program space and 512 KB of data space using optional memory configurations
- 16-MHz crystal-controlled clock oscillator (Y2) in a socket that can accommodate optional 8- or 14-pin oscillator chips (XY2)
- Headers for jumper selection of hardware options.\(^1\)
  - Low-voltage inhibit (W1)
  - RAM write-protection (W3)
  - MCU chip selects for memory devices (W11)
  - RAM function select (W12, W13)
  - ROM function select (W22, W24, W29, W32, W33, W36)
  - MCU mode control (W30, W34, W42)
  - Alternate execution from on-chip EEPROM (W20)
  - Serial Communications Interface (SCI) configuration (W10, W14, W21)
- Two 2x30 header connectors for access to the MCU’s I/O and bus lines (J8 and J9)
- Prototype expansion area for customized interfacing with the MCU
- Low-profile reset (S1) and program-abort (S2) push-button switches
- Low voltage inhibit protection (U1)
- LED power-on indicator (DS1)
- Test points for ground connections around the board (E1, E2, E3, E12, E13, E14)
- 2x3 header (J5) provides a connector for using background debug development tools such as the Serial Debug Interface (SDI)
- Phase-Locked Loop (PLL) biasing circuitry for altering the MCU’s time base

\(^1\)For full details of the jumper settings, refer to Table 4-1.

**Firmware features** include:
- The D-Bug12 monitor/debugger program, resident in external EPROM
- Full support for either dumb-terminal or host-computer terminal interface
- Single-line assembler/disassembler
- File-transfer capability from a host computer, allowing off-board code generation
Figure 1-1. EVB Layout and Component Placement
1.3 PERFORMANCE NOTES

The M68HC12A4EVB's external RAM memory chips, U4 and U6A, were chosen to emphasize the EVB's low-voltage and low-power operational capability over the range of +3.5 to +5.0 Vdc.

However, these parts are not fast enough to operate at the 16-MHz speed of the factory-supplied clock oscillator. In order to use them at this external clock speed, the D-Bug12 startup code programs the MCU's RAM chip select to insert one "wait state" into each access of external RAM. Thus, when programs are run from external RAM, performance is approximately 40% slower than it would be if the RAM chips were fast enough to run without wait states. Typical software performance improvements of 80% - 95% can be realized with faster external RAM.
For high-speed performance, the factory-supplied RAM devices may be replaced with faster parts that allow programs to execute at the full external clock speed. Two steps are required for this:

1. Replace the RAM devices, U4 and U6A, with faster parts.
2. Modify the RAM chip select to eliminate the wait state (E-clock stretch).

Detailed instructions for these procedures are found in 2.6 Using Fast External RAM.

**NOTES**

Programs that execute exclusively from the MCU’s on-chip RAM and EEPROM always run at the full clock speed. No wait states are introduced when accessing these areas.

Table 3-5, the default memory map, depicts the addresses of the EVB’s different memory areas.

### 1.4 FUNCTIONAL OVERVIEW

The EVB is factory-configured to execute D-Bug12, the EPROM-resident monitor program, without further configuration by the user. It is ready for use with an RS-232C terminal for writing and debugging user code. Follow the setup instructions in Chapter 2 to prepare for operation.

Optionally, the EVB can accommodate various types and configurations of external memory to suit a particular application’s requirements. These custom configurations are effected by installing the appropriate memory chips in the EVB’s memory sockets and by setting jumpers on the EVB to correctly establish the MC68HC812A4’s memory-access operations. Table 1-1 lists the allowable sizes and types of memory. For the correct jumper settings, refer to 4.2 Configuration Headers and Jumper Settings.

**NOTE**

The D-Bug12 operating instructions in this manual presume the factory-default memory configuration. Other configurations require different operating-software arrangements.

The MC68HC812A4’s two Serial Communications Interface (SCI) ports are associated with separate RS-232C interfaces. D-Bug12 uses one of the SCIs for communications with the user terminal (jumper-selectable; SCI0 by default). The second SCI port is available for user applications. For information on the ports and their connectors, refer to 2.4 EVB to Terminal Connection and 4.4 Terminal Interface.

If the MCU’s single-wire background debug mode (BDM) interface serves as the user interface, both of the SCI ports become available for user applications. This mode requires a background debug development tool, such as Motorola’s Serial Debug Interface (SDI), and a host computer.
with the appropriate interface software. For more information, refer to Appendix F and to the

NOTE

D-Bug12 does not use the BDM interface.

Two methods may be used to generate EVB user code:

1. For small programs or subroutines, D-Bug12's single-line assembler/disassembler may
be used to place object code directly into the EVB's memory.

2. For larger programs, the Motorola MCUasm assembler may be used on a host
computer to generate S-Record object files, which can then be loaded into the EVB's
memory using D-Bug12's LOAD command.

The EVB features a prototype area, which allows custom interfacing with the MCU's I/O and bus
lines. These connections are broken out via headers J8 and J9, which are immediately adjacent to
the prototype area as shown in Figure 1-1.

An on-board push-button switch, S1, provides for resetting the EVB hardware and restarting
D-Bug12. Another on-board switch, S2, allows aborting the execution of a user program —
useful in regaining control of a runaway program. Both of these switch functions are available for
customized use in the prototype area.

The EVB can begin operation in either of two jumper-selectable (W20) modes at reset. In normal
mode, D-Bug12 immediately issues its command prompt on the terminal display and waits for a
user entry. In the alternate mode, execution begins directly with the user code in on-chip
EEPROM. This hardware function is also available for customized use in the prototype area.

D-Bug12 allows programming of the MC68HC812A4's on-chip EEPROM through commands
that directly alter memory. For full details of all the commands, refer to 3.5 D-Bug12 Command
Set.

Due to the fact that the MCU must manage the EVB hardware and execute D-Bug12 in addition
to serving as the user-application processor, there are a few restrictions on its use. For more
information, refer to 3.9 Operational Limitations.

1.5 EXTERNAL EQUIPMENT REQUIREMENTS

In addition to the EVB, the following user-supplied external equipment is required:

- Power supply — see Table 1-1 for voltage and current requirements.
NOTE

Table 1-1 indicates that EVB operation at +3.0 Vdc requires the slower clock speed of 8 MHz. This limitation applies to programs (including the operating firmware, D-Bug12) that use external memory.

If an application program uses on-chip RAM and EEPROM exclusively — i.e., if external memory is not used — the clock speed can remain at 16 MHz with a supply voltage of +3.0 Vdc.

- User terminal — options:
  - RS-232C dumb terminal — allows single-line on-board code assembly and disassembly.
  - Host computer with RS-232C serial port — allows off-board code assembly that can be loaded into the EVB’s memory. Requires a user-supplied communications program capable of emulating a dumb terminal. Examples of acceptable communications programs are given in Appendix B.
  - Host computer using the MCU’s BDM interface — frees both of the MCU’s SCI ports for user applications. Requires a background debug development tool, such as the Motorola Serial Debug Interface (SDI), and the appropriate interface software.

- Power-supply and terminal interconnection cables as required

For full details of equipment setup, cabling, and special requirements, refer to Chapter 2.

1.6 EVB SPECIFICATIONS

Table 1-1 lists the EVB specifications.
Table 1-1. EVB Specifications

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<td>16 MHz clock source</td>
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# 1.7 CUSTOMER SUPPORT

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<td>(31)4998 612 11</td>
</tr>
<tr>
<td></td>
<td>PUERTO RICO</td>
<td></td>
</tr>
<tr>
<td></td>
<td>San Juan</td>
<td>(809)793-2170</td>
</tr>
<tr>
<td>SINGAPORE</td>
<td></td>
<td>(65)4818188</td>
</tr>
<tr>
<td>SPAIN</td>
<td>Madrid</td>
<td>34(1)457-8204</td>
</tr>
<tr>
<td>SWEDEN</td>
<td>Solna</td>
<td>46(8)734-8800</td>
</tr>
<tr>
<td>SWITZERLAND</td>
<td>Geneva</td>
<td>41(22)799 11 11</td>
</tr>
<tr>
<td></td>
<td>Zurich</td>
<td>41(1)730-4074</td>
</tr>
<tr>
<td>TAIWAN</td>
<td>Taipei</td>
<td>886(2)717-7089</td>
</tr>
<tr>
<td>THAILAND</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bangkok</td>
<td>66(2)254-4910</td>
</tr>
<tr>
<td>UNITED KINGDOM</td>
<td>Aylesbury</td>
<td>44(296)395-252</td>
</tr>
<tr>
<td></td>
<td>UNITED STATES</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Phoenix, AZ</td>
<td>1-800-441-2447</td>
</tr>
</tbody>
</table>

For a list of the Motorola sales offices and distributors: http://freeware.aus.sps.mot.com/
CHAPTER 2
CONFIGURATION AND SETUP

2.1 UNPACKING AND PREPARATION

Verify that the following items are present in the EVB package:

- The M68HC12A4EVB board assembly
- Warranty and registration cards
- EVB schematic diagram and parts list
- MC68HC812A4 Technical Summary
- CPU12 Reference Manual
- MC68HC12 Family Brochure
- Demo software
- Assembly Language Development Toolset
- Using D-Bug12 Callable Routines

Save all packing materials for storing and shipping the EVB.

Remove the EVB from its anti-static shipping bag.

Carefully remove the protective case and conductive foam that cover the MCU and its socket during shipment.

Inspect the alignment of the MCU’s pins within its socket. If it appears necessary to reseat the MCU,

1. press down on two opposite sides of the MCU socket
2. gently press the MCU chip into place
3. release the MCU socket.

Verify that all other socketed parts are correctly seated.
2.2 EVB CONFIGURATION

Because the EVB has been factory-configured to operate with D-Bug12, it is not necessary to change any of the jumper settings to begin operating immediately.

Only one jumper (header W20) should be changed during the course of factory-default EVB operation with D-Bug12:

- pins 2-3 jumpered (default) — Normal execution mode. D-Bug12 is executed from external EPROM upon reset. The D-Bug12 prompt appears immediately on the terminal display.

- pins 1-2 jumpered — Alternate execution mode. User code is executed from on-chip EEPROM upon reset. For more information, refer to 3.6 Alternate Execution from EEPROM.

Other jumper settings affect the hardware setup and/or MCU operational modes. For an overview of all jumper-selectable functions, refer to 1.2 General Description and Features. For details of the settings, see Table 4-1.

2.3 EVB TO POWER SUPPLY CONNECTION

The EVB requires a user-provided external power supply. See Table 1-1 for the voltage and current specifications. For full details of the EVB’s power-input circuitry, refer to 4.3 Power Input Circuitry.

Although fuse protection is built into the EVB, a power supply with current-limiting capability is desirable. If this feature is available on the power supply, set it to 200 mA.

Connect the external power supply to connector J6 on the EVB as shown in Figure 2-1, using 20 AWG or smaller insulated wire. Strip each wire’s insulation 1/4 in. from the end, lift the J6 contact lever to release tension on the contact, insert the bare end of the wire into J6, and close the lever to secure the wire. Observe the polarity carefully.

CAUTION

Do not use wire larger than 20 AWG in connector J6. Larger wire could damage the connector.
2.4 EVB TO TERMINAL CONNECTION

For factory-default operation, connect the terminal to J3 or J4 on the EVB, as shown in Table 2-1. This setup uses the MCU’s SCI port 0 (SCI0) and its associated RS-232C interface for communications with the terminal device.

To use SCI1 and the second RS-232C interface for the terminal, the EVB’s hardware setup must be modified. For details, refer to 4.4 Terminal Interface.

Standard, commercially available cables may be used in most cases. Note that the EVB uses only three of the RS-232C signals. Table 2-1 lists these signals and their pin assignments.

The EVB’s RS-232C connectors, J2 (default) and J3 (unpopulated footprint), are wired as Data Circuit-terminating Equipment (DCE) and employ 9-pin subminiature D (DB-9) receptacles. The equivalent 3-pin headers, J1 and J4, serve the same purposes and may be used for customized cabling.

Most terminal devices — whether dumb terminals or the serial ports on host computers — are wired as Data Terminal Equipment (DTE) and employ 9- or 25-pin subminiature D (DB-9 or DB-25) plugs. In these cases, normal straight-through cabling is used between the EVB and the terminal. Adapters are readily available for connecting 9-pin cables to 25-pin terminal connectors.

If the terminal device is wired as DCE, the RXD and TXD lines must be cross-connected, as shown in Table 2-1. Commercial “null modem” adapter cables are available for this purpose.
Table 2-1. RS-232C Interface Cabling

<table>
<thead>
<tr>
<th>EVB Pins (always DCE)</th>
<th>DTE Signal</th>
<th>Terminal Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>J3(1) / J2(2) DB-9 Receptacle</td>
<td>J4(1) / J1(2) 3-Pin Header</td>
<td>DTE(3) Plug</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>Receive Data (RXD)</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>Transmit Data (TXD)</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>Ground (GND)</td>
</tr>
</tbody>
</table>

(1) Factory default (terminal interface uses SCI0)  
(2) Optional (terminal interface uses SCI1). Hardware modifications are required. For details, refer to 4.4 Terminal Interface.  
(3) Normal (DCE-to-DTE) cable connections  
(4) Null modem (DCE-to-DCE) cable connections

Optionally, the MCU’s background debug mode (BDM) interface can serve as the user interface. This setup makes both of the SCI ports available for user applications. Additional hardware and software are required. For more information, refer to the documentation for the background debug development tool being used, such as Motorola’s Serial Debug Interface.

NOTE

D-Bug12 does not use the BDM interface.

2.5 TERMINAL COMMUNICATIONS SETUP

2.5.1 Communication Parameters

The EVB's serial communications ports use the communication parameters listed in Table 2-2. Of these, only the baud rate can be changed. For instructions on changing it, refer to 2.5.4 Changing the Baud Rate.
Table 2-2. Communication Parameters

<table>
<thead>
<tr>
<th>Baud Rate</th>
<th>9600</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Bits</td>
<td>8</td>
</tr>
<tr>
<td>Stop Bits</td>
<td>1</td>
</tr>
<tr>
<td>Parity</td>
<td>none</td>
</tr>
</tbody>
</table>

2.5.2 Dumb-Terminal Setup

Configuring a dumb terminal for use with the EVB consists of setting its parameters as shown in Table 2-2. Many terminals are configurable with externally accessible switches, but the procedure differs between brands and models. Consult the manufacturer’s instructions for the terminal being used.

2.5.3 Host-Computer Setup

One advantage of using a host computer as the EVB’s terminal is the ability to generate code off-board, for subsequent loading into the EVB’s memory. It is thus desirable for the host to be capable of running programs such as Motorola’s MCUasm assembler. For more information, refer to 3.7 Off-Board Code Generation.

To serve as the EVB’s terminal, the host computer must have an RS-232C serial port and an installed communications program capable of operating with the parameters listed in Table 2-2.

Setting up the parameters is normally done within the communications program, after it has been started on the host. Usually, the setup can be saved in a configuration file so that it does not have to be repeated. Procedures vary between programs; consult the user’s guide for the specific program.

Appendix B provides examples of using some of the commonly available communications programs.

2.5.4 Changing the Baud Rate

The EVB’s default baud rate for the RS-232C ports is 9600. This can be changed in two ways:

- For temporary changes, use the D-Bug12 BAUD command. This change remains in effect only until the next reset or power-up, at which time the baud rate returns to 9600.

- For permanent changes, the D-Bug12 baud-rate initialization value stored in EPROM must be modified. For instructions, refer to Appendix D and Appendix E.
2.6 USING FAST EXTERNAL RAM

To replace the two factory-supplied SRAM chips with parts capable of operation at the full 16-MHz external clock speed (8-MHz E-clock) with no wait states, two operations are required:

1. Replace the SRAM chips with suitably fast parts — section 2.6.1.
2. Reprogram the SRAM chip select, CSD*, for zero-wait-state operation — section 2.6.2.

2.6.1 Selecting and Replacing the RAM Chips

The replacement 8K x 8 SRAM devices should have a chip-select access time of less than 60 nanoseconds. An example of a device that has been used successfully is the Integrated Device Technologies part number IDT7164L25P (8K x 8, 25 ns).

When installing the replacement SRAM devices, make sure that their pins align with the rightmost ends of sockets U4 and U6A, as viewed in Figure 1-1.

2.6.2 Reprogramming the RAM Chip Select

Either of two methods may be used to reprogram the RAM chip select, CSD*, to eliminate the wait state.

NOTE

Before attempting either of the following methods, ensure that the EVB is operating properly by following the startup instructions in section 3.1.

Method A — modifying the CSSTR0 register in memory (temporary)

This method may be used without altering the D-Bug12 startup code in EPROM. However, it must be repeated each time the EVB is powered up or reset.

Using D-Bug12's MM command, change the value at memory location $003E from $05 to $04.

Method B — modifying the D-Bug12 startup code in EPROM (permanent)

This method is accomplished by reprogramming a single byte in the factory-supplied, one-time-programmable (OTP) EPROM, U7. An EPROM programmer is required.
NOTES

This method does not work in reverse. If U7 has already been reprogrammed using this technique, it cannot be restored to its original state.

If the EPROMs are to be customized in some other way — for example, to add a user program or to modify another aspect of D-Bug12 — the change to register CSSTR0 can be made in the startup source code. For more information, refer to Appendix C, D-Bug12 Startup Code, and Appendix E, Customizing the EPROMs.

To permanently reprogram U7 for zero RAM wait states, follow these steps:

1. Remove power from the EVB.
2. Being careful not to bend any pins, remove U7 from its socket on the EVB and install it in the appropriate socket on the EPROM programmer.
3. Following the instructions and using the software for the EPROM programmer, perform the steps in Procedure 1 or Procedure 2, as described below.

Some EPROM programmers do not have an editable RAM buffer capable of holding the entire contents of U7. Instead, they program EPROMs directly from the contents of a disk file.

If the programmer being used has an editable RAM buffer large enough to hold the contents of U7, use Procedure 1. Otherwise, to reprogram U7 from a disk file, use Procedure 2.

Procedure 1

1. Select the Atmel device type AT27LV256R.
2. Read the contents of U7 into the EPROM programmer's editable RAM buffer.
3. Before modifying U7, save a copy of its contents to a disk file for backup purposes.
4. Change the contents of the programmer's editable RAM buffer at location $7ED6 from $05 to $04.
5. Reprogram U7 with the edited contents of the programmer's RAM buffer.
6. Reinstall U7 in its socket on the EVB. Be sure that its pins align with the rightmost end of its socket, as viewed in Figure 1-1.
7. Apply power to the EVB and press S1, the reset switch. The D-Bug12 prompt should appear on the terminal display.
8. Ensure that the modification was performed properly by using D-Bug12's MD command to examine the CSSTR0 register at memory location $003E. It should contain the value $04.
Procedure 2

1. Create a text file containing the following two lines:
   
   S1047E6D040C
   S9030000FC

2. Select the Atmel device type AT27LV256R.

3. Before modifying U7, save a copy of its contents to a disk file for backup purposes.

4. Reprogram U7 with the contents of the text file created in Step 1.

5. Reinstall U7 in its socket on the EVB. Be sure that its pins align with the rightmost end of its socket, as viewed in Figure 1-1.

6. Apply power to the EVB and press S1, the reset switch. The D-Bug12 prompt should appear on the terminal display.

7. Ensure that the modification was performed properly by using D-Bug12's MD command to examine the CSSTR0 register at memory location $003E. It should contain the value $04.
CHAPTER 3
OPERATION

3.1 STARTUP

The following startup procedure includes a checklist of configuration and setup items from Chapter 2. To begin operating the M68HC12A4EVB, follow these steps:

1. Configure the EVB if required — section 2.2.
2. Determine whether execution should begin with the D-Bug12 monitor program (factory default) or with user code in on-chip EEPROM. Set the jumper on header W20 accordingly — sections 2.2 and 3.6.
3. Connect the EVB to the external power supply — section 2.3.
4. Connect the EVB to the terminal — section 2.4.
5. Configure the terminal communications interface — section 2.5.
6. Apply power to the EVB and to the terminal. If the terminal is a host computer,
   a. Verify that it has booted correctly.
   b. Start the communications program for terminal emulation — section 2.5.3 and Appendix B.
7. Reset the EVB by pressing and releasing the on-board reset switch (S1).

If the EVB is configured to execute D-Bug12 upon reset (factory default — startup step 2), the D-Bug12 sign-on banner and prompt should appear on the terminal’s display as follows:

D-Bug12 v1.0.2
Copyright 1995 - 1996 Motorola Semiconductor
For Commands type “Help”
>

If the prompt does not appear, check all connections and verify that startup steps 1 through 7 above have been performed correctly.

When the prompt appears, D-Bug12 is ready to accept commands from the terminal as described in sections 3.4 and 3.5.
If the EVB is configured to execute user code upon reset (startup step 2), the code in on-chip EEPROM is executed immediately. For more information, refer to 3.6 Alternate Execution from EEPROM. Control can be returned to the D-Bug12 terminal prompt by doing one of the following:

1. Terminating the user code with appropriate instructions — see section 3.6.
2. Activating the program-abort function — see section 3.3.

3.2 RESET

EVB operation can be restarted at any time by activating the hardware reset function. Do this in one of two ways:

1. Press and release the on-board reset switch, S1 (always applicable).
2. If the hardware reset input has been customized in the prototype area, activate it in accordance with the custom circuitry.

Note that the EVB’s reset circuitry is associated with the low-voltage inhibit protection. For more information, refer to 4.9 Reset and 4.10 Low-Voltage Inhibit.

3.3 PROGRAM ABORT

During software development, bugs in the code can cause a program to get stuck in an endless loop, thereby preventing proper response (i.e., a "crash"). In these situations, use the EVB’s program-abort function to return control of execution to D-Bug12, which then displays the register contents at the point where the user program was terminated.

Activating the program-abort function asserts the MCU’s XIRQ* hardware interrupt line. There are restrictions on its use under certain circumstances; refer to 3.9 Operational Limitations.

Activate the program-abort function by doing one of the following:

1. Press and release the on-board program-abort switch, S2.
2. If the program-abort input has been customized in the prototype area, activate it in accordance with the custom circuitry.
NOTE
If the EVB is configured to begin execution from on-chip EEPROM, D-Bug12 jumps to the starting EEPROM address without before performing all of its initialization and is thus not operable. Do not activate the program-abort function under these conditions. Instead, move the jumper on header W20 to pins 2-3 and activate the reset function to return control to D-Bug12.

3.4 USING D-BUG12 COMMANDS

D-Bug12, the EVB’s firmware-resident monitor program, provides a self-contained operating environment that allows writing, evaluation, and debugging of user programs.

Commands are typed on the terminal’s D-Bug12 prompt line and executed when the carriage-return (ENTER) key is pressed. D-Bug12 then displays either the appropriate response to the command or an error indication.

The D-Bug12 command-line prompt is the greater-than sign (>). Type the command and any other required or optional fields immediately after the prompt, as follows:

command-line syntax:
<command>  [<parameter>]  ...[<parameter>]<ENTER>

where:
<command> is the command mnemonic.
<parameter> is an expression or address.
<ENTER> is the terminal keyboard’s carriage-return or enter key.

NOTES
1. The command-line syntax is illustrated using the following special characters for clarification. Do not type these characters on the command line:
   <>  required syntactical element
   [ ]  optional field
   ...[ ]  repeated optional fields
2. Fields are separated by any number of space characters.
3. All numeric fields, unless noted otherwise, are interpreted as hexadecimal.
4. Command-line entries are case-insensitive and may be typed using any combination of upper- and lower-case letters.
5. A maximum of 80 characters, including the terminating carriage return, may be entered on the command line. After the 80th character, D-Bug12 automatically terminates the command-line entry and processes the characters entered to that point.

6. Before the <ENTER> key is pressed, the command line may be edited using the backspace key. Receiving the backspace character causes D-Bug12 to delete the previously-received character from its input buffer and erase the character from the display.

Table 3-1 summarizes the D-Bug12 commands. For detailed descriptions of each command, refer to 3.5 D-Bug12 Command Set.

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASM &lt;address&gt;</td>
<td>Single-line assembler/disassembler</td>
</tr>
<tr>
<td>BAUD &lt;BAUDRate&gt;</td>
<td>Set the SCI communications baud rate</td>
</tr>
<tr>
<td>BF &lt;StartAddress&gt;&lt;EndAddress&gt; [&lt;Data&gt;]</td>
<td>Block Fill user memory with data</td>
</tr>
<tr>
<td>BR [&lt;Address&gt;&lt;Address&gt;...]</td>
<td>Set/display user breakpoints</td>
</tr>
<tr>
<td>BULK</td>
<td>Bulk erase on-chip EEPROM</td>
</tr>
<tr>
<td>CALL [&lt;Address&gt;]</td>
<td>Execute a user subroutine; return to D-Bug12 when finished</td>
</tr>
<tr>
<td>G [&lt;Address&gt;]</td>
<td>Go — begin execution of user program</td>
</tr>
<tr>
<td>GT &lt;Address&gt;</td>
<td>Go Till — set a temporary breakpoint and begin execution of user program</td>
</tr>
<tr>
<td>HELP</td>
<td>Display D-Bug12 command set and command syntax</td>
</tr>
<tr>
<td>LOAD [&lt;AddressOffset&gt;]</td>
<td>Load user program in S-Record format*</td>
</tr>
<tr>
<td>MD &lt;StartAddress&gt; [&lt;EndAddress&gt;]</td>
<td>Memory Display — display memory contents in hex bytes/ASCII format</td>
</tr>
<tr>
<td>MDW &lt;StartAddress&gt; [&lt;EndAddress&gt;]</td>
<td>Memory Display Word — display memory contents in hex words/ASCII format</td>
</tr>
<tr>
<td>MM &lt;Address&gt; [&lt;data&gt;]</td>
<td>Memory Modify — interactively examine/change memory contents</td>
</tr>
<tr>
<td>MMW &lt;address&gt; [&lt;data&gt;]</td>
<td>Memory Modify Word — interactively examine/change memory contents</td>
</tr>
<tr>
<td>MOVE &lt;StartAddress&gt; &lt;EndAddress&gt; &lt;DestAddress&gt;</td>
<td>Move a block of memory</td>
</tr>
<tr>
<td>NOBR [&lt;Address&gt; &lt;Address&gt;...]</td>
<td>Remove individual user breakpoints</td>
</tr>
</tbody>
</table>
Table 3-1. D-Bug12 Command-Set Summary (continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RD</td>
<td>Register Display — display the CPU register contents</td>
</tr>
<tr>
<td>RM</td>
<td>Register Modify — interactively examine/change CPU register contents</td>
</tr>
<tr>
<td>T [&lt;Count&gt;]</td>
<td>Trace — execute an instruction, disassemble it, and display the CPU registers</td>
</tr>
<tr>
<td>UPLOAD &lt;StartAddress&gt; &lt;EndAddress&gt;</td>
<td>Display memory contents in S-Record format*</td>
</tr>
<tr>
<td>VERF [&lt;AddressOffset&gt;]</td>
<td>Verify memory contents against S-Record Data</td>
</tr>
<tr>
<td>&lt;RegisterName&gt; &lt;RegisterValue&gt;</td>
<td>Set CPU &lt;RegisterName&gt; to &lt;RegisterValue&gt;</td>
</tr>
</tbody>
</table>
* Refer to Appendix A for S-record information.

3.5 D-BUG12 COMMAND SET

In the following command descriptions, the examples represent what is seen on the terminal display. For clarity, the user's entry is underlined. This underlining does not actually appear onscreen.

A typical example looks like this:

```
>baud 9600                     user's entry
Change Terminal BR, Press Return D-Bug12's response
>                                  D-Bug12 prompt for next entry
```
ASM

Assembler/Disassembler

ASM

syntax:

ASM  <Address>

where:

<Address>  is a 16-bit hexadecimal number.

The assembler/disassembler is an interactive memory editor that allows memory contents to be viewed and altered using assembly language mnemonics. Each entered source line is translated into object code and placed into memory at the time of entry. When displaying memory contents, each instruction is disassembled into its source mnemonic form and displayed along with the hexadecimal object code and any instruction operands.

Assembler mnemonics and operands may be entered in any mix of upper and lower case letters. Any number of spaces may appear between the assembler prompt and the instruction mnemonic or between the instruction mnemonic and the operand. Numeric values appearing in the operand field are interpreted as signed decimal numbers. Placing a $ in front of any number will cause the number to be interpreted as a hexadecimal number.

When an instruction is disassembled and displayed, the D-Bug12 prompt is displayed following the disassembled instruction. If a carriage return is the first non-space character entered following the prompt, the next instruction in memory is disassembled and displayed on the next line.

If a CPU12 instruction is entered following the prompt, the entered instruction is assembled and placed into memory. The line containing the new entry is erased and the new instruction is disassembled and displayed on the same line. The next instruction location is then disassembled and displayed on the screen.

The instruction mnemonics and operand formats accepted by the assembler follows the syntax as described in the CPU12 Reference Manual.

There are a number of M68HC11 instruction mnemonics that appear in the CPU12 Reference Manual that do not have directly equivalent CPU12 instructions. These mnemonics, listed in Table 3-2, are translated into functionally equivalent CPU12 instructions. To aid the current M68HC11 users who may desire to continue using the M68HC11 mnemonics, the disassembler portion of the assembler/disassembler recognizes the functionally equivalent CPU12 instructions and disassembles those instructions into the equivalent M68HC11 mnemonics.

When entering branch instructions, the number placed in the operand field should be the absolute destination address of the instruction. The assembler calculates the two’s-complement offset of the branch and places the offset in memory with the instruction.
The assembly/disassembly process may be terminated by entering a period (.) as the first non-space character following the assembler prompt.

restrictions:

None.

<table>
<thead>
<tr>
<th>M68HC11 Mnemonic</th>
<th>CPU12 Instruction</th>
<th>M68HC11 Mnemonic</th>
<th>CPU12 Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLC</td>
<td>ANCC #$FE</td>
<td>INS</td>
<td>LEAS 1, S</td>
</tr>
<tr>
<td>CLI</td>
<td>ANCC #$EF</td>
<td>TAP</td>
<td>TFR A, CC</td>
</tr>
<tr>
<td>CLV</td>
<td>ANCC #$FD</td>
<td>TPA</td>
<td>TFR CC, A</td>
</tr>
<tr>
<td>SEC</td>
<td>ORCC #$01</td>
<td>TSX</td>
<td>TFR S, X</td>
</tr>
<tr>
<td>SEI</td>
<td>ORCC #$10</td>
<td>TSY</td>
<td>TFR S, Y</td>
</tr>
<tr>
<td>SEV</td>
<td>ORCC #$02</td>
<td>XGDX</td>
<td>EXG D, X</td>
</tr>
<tr>
<td>ABX</td>
<td>LEAX B, X</td>
<td>XGDY</td>
<td>EXG D, Y</td>
</tr>
<tr>
<td>ABY</td>
<td>LEAY B, Y</td>
<td>SEX R6, R16</td>
<td>TFR R6, R16</td>
</tr>
<tr>
<td>DES</td>
<td>LEAS -1, S</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

example:

```
>ASM 800
0800 CC1000 LDD #$1000
0803 1803123401FE MOVW #$1234,$01FE
0809 0EF9800001F1 BRSET -32768,PC,$01,$0700
080F 18FF TRAP $FF
0811 183FE3 ETBL <Illegal Addr Mode> >_
```

assembly operand format:

This section describes the operand format used by the assembler when assembling CPU12 instructions. The operand format accepted by the assembler is described separately in the CPU12 Reference Manual. Rather than describe the numeric format accepted for each instruction, some general rules are used. Exceptions and complicated operand formats are described separately.

In general, anywhere the assembler expects a numeric value in the operand field, either a decimal or hexadecimal value may be entered. Decimal numbers are entered as signed constants having a range of -32768 to 65535. A leading minus sign (-) indicates negative numbers, the absence of a leading minus sign indicates a positive number. A leading plus sign (+) is not allowed.
Hexadecimal numbers must be entered with a leading dollar sign ($) followed by one to four hexadecimal digits. The default number base is decimal.

For all branching instructions (Bcc, LBcc, BRSET, BRCLR, DBEQ, DBNE, IBEQ, IBNE, TBEQ, and TBNE), the number entered as the branch address portion of the operand field is the absolute address of the branch destination. The assembler calculates the two's-complement offset to be placed in the assembled object code.

**disassembly operand format:**

The operand format used by the disassembler is described separately in the *CPU12 Reference Manual*. Rather than describing the numeric format used for each instruction, some general rules are applied. Exceptions and complicated operand formats are described separately.

All numeric values disassembled as hexadecimal numbers are preceded by a dollar sign ($) to avoid being confused with values disassembled as signed decimal numbers.

For all branch (Bcc, LBcc, BRSET, BRCLR, DBEQ, DBNE, IBEQ, IBNE, TBEQ, TBNE) instructions the numeric value of the address portion of the operand field is displayed as the hexadecimal absolute address of the branch destination.

All offsets used with indexed addressing modes are disassembled as signed decimal numbers.

All addresses, whether direct or extended, are disassembled as four digit hexadecimal numbers.

All 8-bit mask values (BRSET/BRCLR/ANDCC/ORCC) are disassembled as two-digit hexadecimal numbers.

All 8-bit immediate values are disassembled as hexadecimal numbers.

All 16-bit immediate values are disassembled as hexadecimal numbers.
BAUD

Set Baud Rate

syntax:

    BAUD  <BAUDRate>

where:

    <BAUDRate>      is an unsigned 16-bit decimal number.

The BAUD command is used to change the communications rate of the SCI used by D-Bug12 for the terminal interface.

restrictions:

Because the <BAUDRate> parameter supplied on the command line is a 16-bit unsigned integer, BAUD rates greater than 65535 baud cannot be set using this command. The SCI BAUD rate divider value for the requested BAUD rate is calculated using the M clock value supplied in the Customization Data area. Because the SCI BAUD rate divider is a 13-bit counter, certain BAUD rates may not be supported at particular M clock frequencies. If the value calculated for the SCI's BAUD rate divider is equal to zero or greater than 8191, command execution is terminated and the communications BAUD rate is not changed.

dexample:

    >BAUD 50
    Invalid BAUD Rate
    >BAUD 38400
    Change Terminal BR, Press Return
    >
BF  Block Fill  BF

syntax:

BF  <StartAddress>  <EndAddress>  [<Data>]

where:

<StartAddress> is a 16-bit hexadecimal number.
<EndAddress>  is a 16-bit hexadecimal number.
<Data>       is an 8-bit hexadecimal number.

The Block Fill command is used to place a single 8-bit value into a range of memory locations. <StartAddress> is the first memory location written with <data> and <EndAddress> is the last memory location written with <data>. If the <data> parameter is omitted, the memory range is filled with the value $00.

restrictions:

None.

dexample:

>BF 6400 6fff 0
>BF 6f00 6fff 55
>

3-10
BR Breakpoint Set BR

syntax:

\texttt{BR \ [<Address> \ <Address> \ ...]}

where:

\texttt{<Address> \ are \ optional \ 16-bit \ hexadecimal \ numbers.}

The \texttt{BR} command is used to set a software breakpoint at a specified address or to display any previously set breakpoints. The function of a breakpoint is to halt user program execution when the program reaches the breakpoint address. When a breakpoint address is encountered, D-Bug12 disassembles the instruction at the breakpoint address, prints the CPU12's register contents, and waits for a D-Bug12 command to be entered by the user.

Breakpoints are set by typing the breakpoint command followed by one or more breakpoint addresses. Entering the breakpoint command without any breakpoint addresses will display all the currently set breakpoints.

A maximum of 10 user breakpoints may be set at one time.

restrictions:

D-Bug12 implements the breakpoint function by replacing the instruction opcode at the breakpoint address in the users program with an SWI instruction. For this reason, a breakpoint may not be set on a user SWI instruction. Breakpoints may only be set at an opcode address, and breakpoints may only be placed at memory addresses in modifiable memory.

Even though D-Bug12 supports a maximum of 10 user defined breakpoints, a maximum of 9 breakpoints may be set on the command line at one time. This restriction is due to the limitation of the command line processor, which allows a maximum of 10 command line arguments including the command string.

example:

\texttt{>BR \ 35ec \ 2f80 \ c592}
\texttt{Breakpoints: \ 35EC \ 2F80 \ C592}

\texttt{>BR}
\texttt{Breakpoints: \ 35EC \ 2F80 \ C592}

>
**BULK**

**Bulk Erase On-Chip EEPROM**

**syntax:**

```
BULK
```

The BULK command is used to erase the entire contents of the on-chip EEPROM in a single operation. After the bulk erase operation has been performed, each on-chip EEPROM location is checked for an erased condition.

**restrictions:**

None.

**example:**

```
>BULK
>
```
CALL

Call Subroutine

syntax:

CALL [<Address>]

where:

<Address> is an optional 16-bit hexadecimal number.

The CALL command is used to execute a subroutine and return to the D-Bug12 monitor program when the final RTS of the subroutine is executed. When control is returned to D-Bug12, the CPU register contents are displayed. All CPU registers contain the values at the time the final RTS instruction was executed, with the exception of the program counter (PC). The PC contains the starting address of the subroutine. If a subroutine address is not supplied on the command line, the current value of the Program Counter (PC) is used as the starting address.

NOTE:

No user breakpoints are placed in memory before execution is transferred to user code.

restrictions:

If the called subroutine modifies the value of the stack pointer during its execution, it MUST restore the stack pointer’s original value before executing the final RTS of the called subroutine. This restriction is required because a return address is placed on the user’s stack that returns to D-Bug12 when the final RTS of the subroutine is executed. Obviously, any subroutine must obey this restriction to execute properly.

example:

>CALL 820
Subroutine Call Returned

PC  SP  X   Y  D = A:B  CCR = SXHI NZVC
0820 0A00 057C 0000 0F:F9  1001 0000
>

HC12A4EVBUM/D  3-13
GO

Go Execute a User Program

syntax:

G  [<Address>]

where:

<Address>  is an optional 16-bit hexadecimal number.

The G command is used to begin the execution of user code in real time. Before beginning execution of user code, any breakpoints that were set with the BR command are placed in memory. Execution of the user program continues until a user breakpoint is encountered, a CPU exception occurs, or the EVB’s reset or program-abort switch is pressed.

When user code halts for any of these reasons (except reset, which wipes the slate clean) and control is returned to D-Bug12, a message is displayed explaining the reason for user program termination. In addition, D-Bug12 disassembles the instruction at the current PC address, prints the CPU12’s register contents, and waits for the next D-Bug12 command to be entered by the user.

If a starting address is not supplied in the command line parameter, program execution will begin at the address defined by the current value of the Program Counter.

restrictions:

None.

eexample:

> G 800
User Breakpoint Encountered

PC  SP  X  Y  D  =  A:B  CCR = SXHI NZVC
0820  09FE  057C  0000  00:00  1001  0100
0820  08  INX

>
GT

Go Till

GT

syntax:

GT <Address>

where:

<Address> is a 16-bit hexadecimal number.

The GT command is similar to the G command except that a temporary breakpoint is placed at the address supplied on the command line. Any breakpoints that were set by the use of the BR command are NOT placed in the user code before program execution begins. Program execution begins at the address defined by the current value of the Program Counter. When user code reaches the temporary breakpoint and control is returned to D-Bug12, a message is displayed explaining the reason for user program termination. In addition, D-Bug12 disassembles the instruction at the current PC address, prints the CPU12's register contents, and waits for a command to be entered by the user.

restrictions:

None.

eexample:

>GT 820
Temporary Breakpoint Encountered

<table>
<thead>
<tr>
<th>PC</th>
<th>SP</th>
<th>X</th>
<th>Y</th>
<th>D = A:B</th>
<th>CCR = SXHI</th>
<th>NZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0820</td>
<td>09FE</td>
<td>057C</td>
<td>0000</td>
<td>00:00</td>
<td>1001</td>
<td>0100</td>
</tr>
</tbody>
</table>

>
HELP

Onscreen Help Summary

syntax:

HELP

The HELP command is used to display a summary of the D-Bug12 command set. Each command is shown along with its command line format and a brief description of its function.

restrictions:

None.

d example:

HELP
ASM <Address>  Single line assembler/disassembler
<CR>           Disassemble next instruction
< . >          Exit assembly/disassembly
BAUD <baudrate> Set communications rate for the terminal
BF <StartAddress> <EndAddress> [<data>] Fill memory with data
BR [<Address>]  Set/Display user breakpoints
BULK           Erase entire on-chip EEPROM contents
CALL [<Address>] Call user subroutine at <Address>
G [<Address>]   Begin/continue execution of user code
GT <Address>    Set temporary breakpoint at <Address> & execute user code
HELP           Display this D-Bug12 command summary
LOAD [<AddressOffset>] Load S-Records into memory
MD <StartAddress> [<EndAddress>] Memory Display Bytes
MDW <StartAddress> [<EndAddress>] Memory Display Words
MM <StartAddress> Modify Memory Bytes
< CR >         Examine/Modify next location
< / >          Examine/Modify same location
< ^ >          Examine/Modify previous location
< . >          Exit Modify Memory command
MMW <StartAddress> Modify Memory Words (same subcommands as MM)
MOVE <StartAddress> <EndAddress> <DestAddress> Move a block of memory
NOBR [address]  Remove One/All Breakpoint(s)
RD              Display all CPU registers
RM              Modify CPU Register Contents
T [count> Trace <count> Instructions
UPLOAD <StartAddress> <EndAddress>  S-Record Memory display
VERF [<AddressOffset>] Verify S-Records against memory contents
<Register Name> <Register Value> Set register contents
    Register Names: PC, SP, X, Y, A, B, D
    CCR Status Bits: S, XM, H, IM, N, Z, V, C

>
LOAD

Load S-Record File

syntax:

LOAD  [<AddressOffset>]

{Send File}

where:

<AddressOffset>  is an optional 16-bit hexadecimal number.

{Send File}    is the host-computer communications program's utility for sending
               an ASCII (text) file. Refer to Appendix B for examples.

The Load command is used to load S-Record object files into memory from an external device. The address offset, if supplied, is added to the load address of each S-Record before its data bytes are placed in memory. Providing an address offset other than zero allows object code or data to be loaded into memory at a location other than that for which it was assembled. During the loading process, the S-Record data is not echoed to the control console. However, for each ten S-Records that are successfully loaded, an ASCII asterisk character (*) is sent to the control console. When an S-Record file has been successfully loaded, control returns to the D-Bug12 prompt.

The Load command is terminated when D-Bug12 receives an 'S9' end of file record. If the object file being loaded does not contain an 'S9' record, D-Bug12 does not return its prompt and continues to wait for the end of file record. Pressing the Reset switch returns D-Bug12 to its command line prompt.

restrictions:

None.

element:

>LOAD 1000

************************

>

HC12A4EVBUM/D  3-17
syntax:

MD <StartAddress> [<EndAddress>]

where:

<StartAddress> is a 16-bit hexadecimal number.
<EndAddress> is an optional 16-bit hexadecimal number.

The Memory Display command displays the contents of memory as both hexadecimal bytes and ASCII characters, 16-bytes on each line. The <StartAddress> parameter must be supplied; the <EndAddress> parameter is optional. When the <EndAddress> parameter is not supplied, a single line is displayed.

The number supplied as the <StartAddress> parameter is rounded down to the next lower multiple of 16, while the number supplied as the <EndAddress> parameter is rounded up to the next higher multiple of 16 - 1. This causes each line to display memory in the range of $xxx0 through $xxxF. For example, if $205 is entered as the start address and $217 as the ending address, the actual memory range displayed would be $200 through $21F.

restrictions:

None.

element:

>MD 800
0800 AA 04 37 6A - 00 06 27 F9 - 35 AE 78 0D - B7 56 78 20 .7j..'.5.x..Vx

>MD 800 87F
0800 AA 04 37 6A - 00 06 27 F9 - 35 AE 78 0D - B7 56 78 20 .7j..'.5.x..Vx
0810 B6 36 27 F9 - 35 AE 27 F9 - 35 9E 27 F9 - 35 BE B5 28 .6'.5.'..'.5..( 
0820 27 F9 35 D6 - 37 B6 00 0F - 37 82 01 0A - 37 36 FF F0 '5.7...7...76..
0830 7C 10 37 B3 - 00 00 37 B6 - 00 0F AA 04 - A5 02 37 B6 1.7...7...7....7.
0840 00 0F 27 78 - 37 6A 00 06 - 27 F9 35 78 - 27 F9 35 56 ..'x7j.'..5x'.5V
0850 78 0D B7 10 - 78 3B 37 86 - 00 DC 27 F9 - 35 48 78 57 x...x;7...'.5HxW
0860 37 86 00 DE - F5 01 EA 09 - 37 B5 0D 0A - 27 F9 36 2A 7........7....'.6*
0870 A5 00 37 65 - 00 02 27 F9 - 35 E8 37 9C - 37 4C F5 02 ..7e..'5.7.7L..
MDW

Memory Display, Word

syntax:

    MDW  <StartAddress>  [<EndAddress>]

where:

    <StartAddress>  is a 16-bit hexadecimal number.
    <EndAddress>    is an optional 16-bit hexadecimal number.

The Memory Display Word command displays the contents of memory as hexadecimal words and ASCII characters, 16-bytes on each line. The <StartAddress> parameter must be supplied; the <EndAddress> parameter is optional. When the <EndAddress> parameter is not supplied, a single line is displayed.

The number supplied as the <StartAddress> parameter is rounded down to the next lower multiple of 16, while the number supplied as the <EndAddress> parameter is rounded up to the next higher multiple of 16 - 1. This causes each line to display memory in the range of $\text{x}0$ through $\text{x}FF$. For example, if $\text{205}$ is entered as the start address and $\text{217}$ as the ending address, the actual memory range displayed would be $\text{200}$ through $\text{21F}$.

restrictions:

None.

description:

None.

example:

> MDW 800

0800 AA04 376A - 0006 27F9 - 35AE 780D - B756 7820 ..7J..'.5.x..Vx

> MDW 800 87F

0800 AA04 376A - 0006 27F9 - 35AE 780D - B756 7820 ..7J..'.5.x..Vx
0810 B636 27F9 - 35AE 27F9 - 359E 27F9 - 35BE B528 .6'.5.'5.'5.'5...(1
0820 27F9 35D6 - 37B8 000F - 3782 010A - 3736 FFF0 '.5.'7...7..76..
0830 7C10 37B3 - 0000 37B6 - 000F AA04 - A502 37B6 | 17...7...........
0840 000F 2778 - 376A 0006 - 27F9 3578 - 27F9 3556 ..'x7j..'5x'5V
0850 780D B710 - 783B 3786 - 00DC 27F9 - 3548 7857 x.x;7...'.5HxW
0860 3786 00DE - F501 EA09 - 37B5 000A - 27F9 362A ?.....7...'.6*
0870 A500 3765 - 0002 27F9 - 35E8 379C - 374C F502 ..7e..'5.7.7L...

>
Memory Modify

**Syntax:**

```
MM <Address> [Data]
```

**Where:**

- `<Address>` is a 16-bit hexadecimal number.
- `<Data>` is an optional 8-bit hexadecimal number.

The Memory Modify command allows the contents of memory to be examined and/or modified as 8-bit hexadecimal data. If the 8-bit data parameter is present on the command line, the byte at memory location `<Address>` is replaced with `<Data>` and the command is terminated. If not, D-Bug12 enters the interactive memory modify mode. In the interactive mode, each byte is displayed on a separate line following the data's address. Once the memory modify command has been entered, single-character sub-commands are used for the modification and verification of memory contents. These sub-commands have the following format:

- `[Data] <CR>` Optionally update current location and display the next location.
- `[Data] /` or `<=` Optionally update current location and redisplay the current location.
- `[Data] `<` or `<>` Optionally update current location and display the previous location.
- `[Data] `<.` Optionally update current location and exit Memory Modify.

With the exception of the carriage return, the sub-command must be separated from any entered data with at least one space character. If an invalid sub-command character is entered, an appropriate error message is issued and the contents of the current memory location are redisplayed.

**Restrictions:**

None.

**Example:**

```
>MM 800
0800 00 <CR>
0801 F0 FF
0802 00 ^
0801 FF <CR>
0802 00 <CR>
0803 08 55 7
0803 55 _
>
```
**MMW**

**Memory Modify, Word**

**MMW**

**syntax:**

```
MMW  <Address>  [Data]
```

**where:**

- `<Address>` is a 16-bit hexadecimal number.
- `<Data>` is an optional 16-bit hexadecimal number.

The Memory Modify Word command allows the contents of memory to be examined and/or modified as 16-bit hexadecimal data. If the 16-bit data parameter is present on the command line, the word at memory location `<Address>` is replaced with `<Data>` and the command is terminated. If not, D-Bug12 enters the interactive memory modify mode. In the interactive mode, each word is displayed on a separate line following the data’s address. Once the memory modify command has been entered, single-character sub-commands are used for the modification and verification of memory contents. These sub-commands have the following format:

```
[Data]  <CR>  Optionally update current location and display the next location.
[Data]  /  or  <CR>  Optionally update current location and redisplay the current location.
[Data]  ^  or  <>  Optionally update current location and display the previous location.
[Data]  <>  Optionally update current location and exit Memory Modify.
```

With the exception of the carriage return, the sub-command must be separated from any entered data with at least one space character. If an invalid sub-command character is entered, an appropriate error message is issued and the contents of the current memory location are redisplayed.

**restrictions:**

None.

**example:**

```
>MMW  800
 0800  00F0  <CR>
 0802  0008  AA55 /
 0804  843F  ^
 0802  AA55  <CR>
 0804  843F  <CR>
 0806  C000  ^
>
```
MOVE

Move Memory Block

**syntax:**

```
MOVE <StartAddress> <EndAddress> <DestAddress>
```

**where:**

- `<StartAddress>` is a 16-bit hexadecimal number.
- `<EndAddress>` is a 16-bit hexadecimal number.
- `<DestAddress>` is a 16-bit hexadecimal number.

The MOVE command is used to move a block of memory from one location to another, one byte at a time. The number of bytes moved is one more than the `<EndAddress> - <StartAddress>`. The block of memory beginning at the destination address may overlap the memory block defined by the `<StartAddress>` and `<EndAddress>`.

One of the uses of the MOVE command might be to copy a program from RAM into the on-chip EEPROM memory.

**restrictions:**

A minimum of one byte may be moved if the `<StartAddress>` is equal to the `<EndAddress>`. The maximum number of bytes that may be moved is \(2^{16} - 1\).

**example:**

```
>MOVE 800 8ff 1000
>
```
NOBR Remove Breakpoints

syntax:

    NOBR  [<Address>  <Address>  ...]

where:

    <Address>  is an optional 16-bit hexadecimal number.

The NOBR command can be used to remove one or more previously entered breakpoints. If the NOBR command is entered without any arguments, all user breakpoints are removed from the breakpoint table.

restrictions:

None.

example:

    >BR 800 810 820 830
    Breakpoints: 0800 0810 0820 0830

    >NOBR 810 820
    Breakpoints: 0800 0830

    >NOBR
    All Breakpoints Removed

    >
RD

Register Display

syntax:

RD

The Register Display command is used to display the CPU12’s registers.

restrictions:

None.

example:

```
>RD
PC   SP   X   Y   D = A:B   CCR = SXHI NZVC
0206 03FF 1000 3700  27:FF 1001 0001
>
```
Register Modify

**syntax:**

```
RM
```

The Register Modify command is used to examine and/or modify the contents of the CPU12's registers in an interactive manner. As each register and its contents is displayed, D-Bug12 allows the user to enter a new value for the register in hexadecimal. If modification of the displayed register is not desired, entering a carriage return will cause the next CPU12 register and its contents to be displayed on the next line. When the last of the CPU12's registers has been examined and/or modified, the RM command displays the first register, giving the user an opportunity to make additional modifications to the CPU12's register contents. Typing a period (.) as the first non-space character on the line will exit the interactive mode of the register modify command and return to the D-Bug12 prompt. The registers are displayed in the following order, one register per line: PC, SP, X, Y, A, B, CCR.

**restrictions:**

None.

**example:**

```
>RM
PC=0206 200
SP=03FF <CR>
X=1000 1004
Y=3700 <CR>
A=27 <CR>
B=FF <CR>
CCR=D0 D1
PC=0200 .
>  
```
### Syntax:

T [<Count>]

### Where:

- `<Count>` is an optional 8-bit decimal number in the range 1 to 255.

The Trace command is used to execute one or more user program instructions beginning at the current Program Counter (PC) location. As each program instruction is executed, the CPU12's register contents are displayed and the next instruction to be executed is displayed. A single instruction may be executed by entering the trace command immediately followed by a carriage return.

### Restrictions:

Because of the method used to execute a single instruction, branch instructions (Bcc, LBcc, BRSET, BRCLR, DBEQ/NE, IBEQ/NE, TBEQ/NE) that contain an offset that branches back to the instruction opcode DO NOT execute. The terminal appears to become stuck at the branch instruction and does not execute the instruction even if the condition for the branch instruction is satisfied. This limitation can be overcome by using the GT (Go Till) command to set a temporary breakpoint at the instruction following the branch instruction.

When the CPU12 is not operating in background debug mode, there is no specialized hardware available to execute a single instruction. The Trace command makes use of temporary software breakpoints as a means to control CPU execution. For this reason, only instructions that reside in alterable memory may be executed with the Trace command.

### Example:

```
> T

<table>
<thead>
<tr>
<th>PC</th>
<th>SP</th>
<th>X</th>
<th>Y</th>
<th>D=A:B</th>
<th>CCR=SXHI NZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0803</td>
<td>09FE</td>
<td>057C</td>
<td>0000</td>
<td>10:00</td>
<td>1001 0000</td>
</tr>
<tr>
<td>0803</td>
<td>830001</td>
<td>SUBD</td>
<td>#0001</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

> T 3

<table>
<thead>
<tr>
<th>PC</th>
<th>SP</th>
<th>X</th>
<th>Y</th>
<th>D=A:B</th>
<th>CCR=SXHI NZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0806</td>
<td>09FE</td>
<td>057C</td>
<td>0000</td>
<td>0F:FF</td>
<td>1001 0000</td>
</tr>
<tr>
<td>0806</td>
<td>26FB</td>
<td>BNE</td>
<td>$0803</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PC</th>
<th>SP</th>
<th>X</th>
<th>Y</th>
<th>D=A:B</th>
<th>CCR=SXHI NZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0803</td>
<td>09FE</td>
<td>057C</td>
<td>0000</td>
<td>0F:FF</td>
<td>1001 0000</td>
</tr>
<tr>
<td>0803</td>
<td>830001</td>
<td>SUBD</td>
<td>#0001</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
<table>
<thead>
<tr>
<th>PC</th>
<th>SP</th>
<th>X</th>
<th>Y</th>
<th>D=A:B</th>
<th>CCR=SXHI NZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0806</td>
<td>09FE</td>
<td>057C</td>
<td>0000</td>
<td>0F:FE</td>
<td>1001 0000</td>
</tr>
<tr>
<td>0806</td>
<td>26FB</td>
<td>BNE</td>
<td></td>
<td></td>
<td>$0803</td>
</tr>
</tbody>
</table>

>
UPLOAD Display Memory in S-Record Format

**syntax:**

UPLOAD  <StartAddress>  <EndAddress>

**where:**

<StartAddress> is a 16-bit hexadecimal number.
<EndAddress> is a 16-bit hexadecimal number.

The UPLOAD command is used to display the contents of memory in Motorola S-Record format. In addition to displaying the specified range of memory, the UPLOAD command also outputs an S9 end-of-file record. The output of this command may be captured by the users terminal program and saved to a disk file.

**restrictions:**

None.

**example:**

> upload 400 5ff
S12304000F0000843FC0000F50F379F37BF43FCF50F27FA757F177FA047504177FA21C5
S123042037B50FF37FAFB0437B5400037FAFB061735FB0037B3500137F6A003715379C01
S1230440F50F379D37BC012C37BD40008509A003C023D02377C0140B6EE7A0F400037B583
S123046000037FAFA4C37FAFA5037FAFA5437B552037FAFA4E37B5302037FAFA5237B58A
S1230480682037FAFA5637BD014037BC000095006A003C023D02377D0172B6EE37BD017259
S12304A037BC02095058A003C023D02377D018B6EE27F937B0F50F379C37BC00CE27F901
S12304C000FC27F9104C27F90E68378000B6A0D442D42756731620563162033202D20E3
S12304E04465627567204D6F6E69746F7220466F7220546865204D3638483316204661ED
S12305006D69C79A0D2843292031393932204D6F746F7266C612053656D69636F6E64BD
S123052075637467220496E632E000037B5FF0237FAFA4837B580B37FAFA47A0F005E52
S123054000000000000000000020002040208020C0210000000000000000000001214F
S12305600000000000000000000000000000000000000000000000002187A0F3BAC7A0F3BC7A0F11E87A0F62
S12305803C727A0F3C847A0F3C967A0F3CA8F50F379C379D379E27FAFA50F379F37F37CE8
S12305A07501177A40541735405236043612C27F90088BD637BC01BC360227F70A0D3E00A9
S12305C0450B70427F936BC3C01BF027F7277537BC400017BC405027F936CC780DB60477
S12305E027F936A0274A27F77803B6FE803A7808B6162776B7DE373000127F93686752002
S9030000FC >
VERF Verify S-Record File against Memory VERF

syntax:

VERF  [<AddressOffset>]
{Send File}

where:

<AddressOffset>    is an optional 16-bit hexadecimal number.

{Send File}        is the host-computer communications program's utility for sending
                    an ASCII (text) file. Refer to Appendix B for examples.

The VERF command is used to compare the data contained in an S-Record object file to the contents of EVB memory. The address offset, if supplied, is added to the load address of each S-Record before an S-Record's data bytes are compared to the contents of memory. Providing an address offset other than zero allows the S-Record's object code or data to be compared against memory other than that for which the S-Record was assembled.

During the verification process, an ASCII asterisk character (*) is sent to the control console for each ten S-Records that are successfully verified. When an S-Record file has been successfully verified, control returns to the D-Bug12 prompt.

If the contents of EVB memory do not match the corresponding data in the received S-Records, an error message is displayed and the Verify command is terminated. D-Bug12 then returns to its command-line prompt. If the host computer continues to send S-Records to the EVB, D-Bug12 tries to interpret each S-Record as a command and issues error message for each S-Record received.

If the contents of EVB memory match the contents of the received S-Records, the Verify command terminates when D-Bug12 receives an S9 end-of-file record. If the object file being verified does not contain an S9 record, D-Bug12 continues to wait for an S9 record without returning to the command-line prompt. Pressing the reset switch, S1, returns D-Bug12 to its command-line prompt.

restrictions:    None.

example:

> VERF 1000
***************
>

HC12A4EVBUM/D
<Register Name> Modify Register Value <Register Name>

**syntax:**

```
<RegisterName>  <RegisterValue>
```

**where:**

- `<RegisterName>` is one of the CPU12 registers listed in Table 3-3.
- `<RegisterValue>` is an 8- or 16-bit hexadecimal number.

**Table 3-3. CPU12 Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
<th>Legal Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>Program Counter</td>
<td>$0 to $FFFF</td>
</tr>
<tr>
<td>SP</td>
<td>Stack Pointer</td>
<td>$0 to $FFFF</td>
</tr>
<tr>
<td>X</td>
<td>X-Index Register</td>
<td>$0 to $FFFF</td>
</tr>
<tr>
<td>Y</td>
<td>Y-Index Register</td>
<td>$0 to $FFFF</td>
</tr>
<tr>
<td>A</td>
<td>A Accumulator</td>
<td>$0 to $FF</td>
</tr>
<tr>
<td>B</td>
<td>B Accumulator</td>
<td>$0 to $FF</td>
</tr>
<tr>
<td>D</td>
<td>D Accumulator (A:B)</td>
<td>$0 to $FFFF</td>
</tr>
<tr>
<td>CCR</td>
<td>Condition Code Register</td>
<td>$0 to $FF</td>
</tr>
</tbody>
</table>

Each of the fields in the Condition Code Register (CCR) may be modified by using the bit names in Table 3-4.
Table 3-4. Condition Code Register Bits

<table>
<thead>
<tr>
<th>CCR Bit Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>STOP Enable</td>
<td>0 or 1</td>
</tr>
<tr>
<td>H</td>
<td>Half Carry</td>
<td>0 or 1</td>
</tr>
<tr>
<td>N</td>
<td>Negative Flag</td>
<td>0 or 1</td>
</tr>
<tr>
<td>Z</td>
<td>Zero Flag</td>
<td>0 or 1</td>
</tr>
<tr>
<td>V</td>
<td>Two's Complement Overflow Flag</td>
<td>0 or 1</td>
</tr>
<tr>
<td>C</td>
<td>Carry Flag</td>
<td>0 or 1</td>
</tr>
<tr>
<td>IM</td>
<td>IRQ Interrupt Mask</td>
<td>0 or 1</td>
</tr>
<tr>
<td>XM</td>
<td>XIRQ Interrupt Mask</td>
<td>0 or 1</td>
</tr>
</tbody>
</table>

This set of “commands” uses a CPU12 register name as the command name to allow changing the register’s contents. Each register name or CCR bit name is entered on the command line followed by a space, then followed by the new register or bit contents. After successful alteration of a CPU register or CCR bit, the entire CPU register set is displayed.

restrictions:

None.

eexample:

```
>PC 700e
PC SP X Y D=A:B CCR=SXHI NZVC
700E 0A00 7315 7D62 47:44 1001 0000
>X 1000
PC SP X Y D=A:B CCR=SXHI NZVC
700E 0A00 1000 7D62 47:44 1001 0000
>C 1
PC SP X Y D=A:B CCR=SXHI NZVC
700E 0A00 1000 7D62 47:44 1001 0001
>Z 1
PC SP X Y D=A:B CCR=SXHI NZVC
700E 0A00 1000 7D62 47:44 1001 0101
>D adf7
PC SP X Y D=A:B CCR=SXHI NZVC
700E 0A00 1000 7D62 AD:F7 1001 0101
>```

HC12A4EVBUM/D 3-31
3.6 ALTERNATE EXECUTION FROM EEPROM

In this hardware-configured mode (pins 1-2 jumpered on header W20), the EVB begins operation out of reset by executing the user program in on-chip EEPROM starting at address $1000, as shown in Table 3-5.

This mode is effected using the MCU’s PAD0 line, which is broken out in J9 for possible custom use in the prototype area.

Control can be returned to D-Bug12 in the following ways:

1. Move the jumper on W20 to pins 2-3 and reset the EVB. *Do not activate the program abort function — see note in section 3.3.*

2. Terminate the user program with code that returns to D-Bug12 after execution has finished.

To return to D-Bug12 after a user program has finished, include the following lines as the last instructions to be executed in the program:

```
STACKTOP:     equ   $0c00    ; stack at top of on-chip RAM
DEBUG12:      equ   $fd90

;    
lds #STACKTOP
jmp DEBUG12   ; jump to start of D-Bug12 code
```

3.7 OFF-BOARD CODE GENERATION

To generate a user program on a host computer and load it into the EVB’s memory, follow these steps:

NOTE

For steps 2 and 3, follow the instructions in the *Motorola Microcontroller Families MCUasm User’s Manual.*

1. Set up the EVB system with a host computer as the terminal — see section 2.5.3.

2. In the host computer’s native operating mode — i.e., before starting the communications program that allows it to serve as the EVB’s terminal — write and assemble the program using Motorola’s MCUasm assembler.

3. Using the MCUasm assembler’s HEX utility, generate a Motorola S-Record file from the object (.HEX) file. Appendix A contains detailed information about the S-Record formats.

4. Start the EVB with D-Bug12 as the default operating mode, using the procedure in section 3.1.
5. At the D-Bug12 prompt, issue D-Bug12’s LOAD command with any parameters. Note that this requires interaction with the terminal communications program’s “send file” utility — see Appendix B for examples.

3.8 MEMORY USAGE

3.8.1 Description

The EVB’s memory usage and requirements are described below and summarized in Table 3-5. Note that this memory mapping applies only to the factory-default memory configuration.

The monitor program, D-Bug12, occupies 24 Kbytes in the two 32 Kbyte EPROMs, U7 and U9A. The remaining 8 Kbytes are available for user programs and utilities, but since this ROM area cannot be directly written, special techniques are required to take advantage of it. For information on using it, refer to Appendix E Customizing the EPROMs.

Since the MCU must manage the execution of D-Bug12 and other EVB functions, 512 bytes of on-chip RAM, from $0A00 to $0BFF, are required for stack and variable storage. The remaining 512 bytes of on-chip RAM, from $0800 to $09FF, are available for variable storage and stack space by user programs.

NOTE

D-Bug12 sets the default value of the user’s stack pointer to $0A00. This is not a mistake. The M68HC12’s stack pointer points to the last byte that was pushed onto the stack, rather than to the next available byte on the stack, as the M68HC11 does. The M68HC12 first decrements its stack pointer, then stores data on the stack. The M68HC11 stores data on the stack and then decrements its stack pointer.

The 16 Kbytes of external RAM, from $4000 to $7FFF, are available for user code and data.
3.8.2 Memory Map

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Description</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0000 - $01FF</td>
<td>CPU registers</td>
<td>on-chip (MCU)</td>
</tr>
<tr>
<td>$0800 - $09FF</td>
<td>user code/data</td>
<td>1K on-chip RAM (MCU)</td>
</tr>
<tr>
<td>$0A00 - $0BFF</td>
<td>reserved for D-Bug12</td>
<td></td>
</tr>
<tr>
<td>$1000 - $1FFF</td>
<td>user code/data</td>
<td>4K on-chip EEPROM (MCU)</td>
</tr>
<tr>
<td>$4000 - $7FFF</td>
<td>user code/data</td>
<td>16K external RAM (U4, U6A)</td>
</tr>
<tr>
<td>$8000 - $9FFF</td>
<td>available for user programs*</td>
<td>32K external EPROM (U7, U9A)</td>
</tr>
<tr>
<td>$A000 - $FD7F</td>
<td>D-Bug12 program</td>
<td></td>
</tr>
<tr>
<td>$FD80 - $FDFF</td>
<td>D-Bug12 startup code*</td>
<td></td>
</tr>
<tr>
<td>$FE00 - $FE7F</td>
<td>user-accessible functions</td>
<td></td>
</tr>
<tr>
<td>$FE80 - $FEFF</td>
<td>D-Bug12 customization data*</td>
<td></td>
</tr>
<tr>
<td>$FF00 - $FF7F</td>
<td>available for user programs*</td>
<td></td>
</tr>
<tr>
<td>$FF80 - $FFFF</td>
<td>reserved for interrupt and reset vectors</td>
<td></td>
</tr>
</tbody>
</table>

*Code in these areas may be modified. Requires reprogramming of the EPROMs — refer to Appendix E Customizing the EPROMs.

3.9 OPERATIONAL LIMITATIONS

D-Bug12 and other EVB functions require some of the MC68HC812A4’s resources for management. For this reason, the EVB cannot provide true emulation of a target system. These limitations are described in the following sections.

3.9.1 On-Chip RAM

D-Bug12 requires 512 bytes of on-chip RAM for stack and variable storage. This usage is shown in Table 3-5.
3.9.2 SCI Port Usage

D-Bug12 requires one of the MCU’s Serial Communications Interface (SCI) ports for the terminal interface. The SCI port used for this purpose is jumper-selectable (W14), but the one selected is unavailable for other uses.

3.9.3 Dedicated MCU Pins

As used on the EVB with D-Bug12, the following MCU lines perform specific functions. If an application requires their use, the EVB hardware and/or operating software must be custom-configured, or special precautions must be taken in the application code to avoid conflicts with the D-Bug12 usage.

**PE0/XIRQ** — program-abort function (S2). Additionally, there are two software limitations on the program-abort function:

1. D-Bug12 enables the hardware XIRQ interrupt by initializing the XM bit in the Condition Code Register (see Table 3-4). If this interrupt is subsequently disabled in software, for example with the D-Bug12 RM command, it cannot be directly enabled again.

2. If the user code replaces the D-Bug12 interrupt handler with one of its own, the program-abort function is effectively disabled.

**PAD0** — selects normal or alternate execution mode (W20)

**PAD1** — selects the SCI port used for the terminal interface (W14).

**PF4/CSD** and **PF5/CSP0** — dedicated to chip-select usage. Not available for I/O in the default configuration.

**Ports A, B, C, D, and G** — dedicated to address/data bus usage. Not available as I/O ports in the default configuration.

3.9.4 Terminal Communications

High baud rates occasionally result in dropped characters on the terminal display. This is not the result of a baud rate mismatch; it is due to the host processor being too busy or too slow to process incoming data at the selected baud rate. The D-Bug12 MD, MDW, T, and HELP commands may be affected by this problem. Sometimes the problem can be ignored without harm. If it requires correcting, try the following:

- Use a slower baud rate.
- Try a different communications program.
- In multitasking environments such as Windows 3.1 and the MacIntosh System 7, the problem can occur when several applications are running at once. Try closing unnecessary applications or exiting Windows.

- When using the MD, MDW, or T commands, try displaying fewer address locations or tracing fewer instructions at a time.
CHAPTER 4
HARDWARE REFERENCE

4.1 PCB DESCRIPTION

The EVB printed circuit board (PCB) is an 8-inch by 8-inch board with six layers — one power, one ground, and four signal layers. The signal layers containing cut-trace header footprints, described in section 4.2, comprise the top and bottom layers for accessibility.

Most of the connection points on the EVB are headers on 1/10-inch centers, with the following exceptions:

- Subminiature D connectors for the SCI RS-232C interfaces
- Loop-style hardware connections for test points
- External power-supply connections

4.2 CONFIGURATION HEADERS AND JUMPER SETTINGS

The EVB is designed for maximum flexibility — there are 45 PCB footprints available for configuration headers. These are of two types:

**Factory-installed headers** are those most likely to be used for configuration without major alteration of the EVB's hardware operation. These headers are populated, and the factory-installed jumpers on them are preset for the default EVB hardware and firmware (D-Bug12) configurations. Table 4-1 lists these headers by function and describes their default and optional jumper settings.

**Cut-trace header footprints** offer EVB hardware options that are less likely to be changed. These footprints are not populated. The default connection between pins is a trace on the PCB. To change a cut-trace footprint, the PCB trace must be cut. To return to the original configuration, a header and a jumper must be installed to re-establish the shunt.

**NOTE**

Use of the cut-trace header footprints requires a thorough understanding of the MCU and of the EVB hardware. Refer to the *MC68HC812A4 Technical Summary* and to the EVB schematic diagram for design information.
CAUTION

When cutting a PCB trace to customize a header footprint, be careful not to cut adjacent traces. Do not damage the underlying PCB layers by cutting too deeply.

Key to Table 4-1:

- [ ] 2-pin header with no jumper installed
- [ ] 2-pin header with jumper installed
- [ ] 3-pin header with no jumper installed
- [ ] 3-pin header with jumper installed on left 2 pins
- **1-2** bold pin numbers indicate factory-default settings
### Table 4-1. Jumper-Selectable Functions

<table>
<thead>
<tr>
<th>Diagram</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W1</strong></td>
<td>Low-Voltage Inhibit (LVI)</td>
<td></td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>low-voltage inhibit is enabled</td>
</tr>
<tr>
<td></td>
<td>off</td>
<td>low-voltage inhibit is disabled</td>
</tr>
</tbody>
</table>

**W3** RAM Write-Protection

| ![Diagram](image) | 1-2 | RAM write-protection is disabled |
|                  | 2-3 | RAM write-protection is enabled |

**W10** TXD1 — RS-232C Transmit Data (TXD) Enable, SCI Port 1

| ![Diagram](image) | 1-2 | TXD on SCI port 1 is enabled |
|                  | 2-3 | TXD on SCI port 1 is disabled |

**W11** ROM and RAM Chip Select (CS)

| ![Diagram](image) | 1-2 | connects an MCU chip select to the devices installed in the ROM sockets |
|                  | 2-3 | connects an MCU chip select to the devices installed in the RAM sockets |
| **CS0** | connects an MCU chip select to the devices installed in the ROM sockets |
| **CS1** | connects an MCU chip select to the devices installed in the RAM sockets |
| **CS2** | connects an MCU chip select to the devices installed in the ROM sockets |
| **CS3** | connects an MCU chip select to the devices installed in the RAM sockets |
| **CSD** | connects an MCU chip select to the devices installed in the ROM sockets |
| **CSP0** | connects an MCU chip select to the devices installed in the RAM sockets |
| **CSP1** | connects an MCU chip select to the devices installed in the RAM sockets |
| **ROM** | DEFAULT: CSP0* is the ROM chip select |
| **RAM** | CSD* is the RAM chip select |

**W12** RAM Pin Assignment — pin 30 of 32-pin package or pin 28 of 28-pin package

| ![Diagram](image) | 1-2 | pin is connected to MCU address line A17 — for Narrow modes |
|                  | 3-4 | pin is connected to MCU address line A18 — for Wide modes |
|                  | 5-6 | pin is connected to V_{DD} — for 28-pin devices |

**W13** RAM Pin Assignment — pin 28 of 32-pin package or pin 28 of 28-pin package

| ![Diagram](image) | 1-2 | pin is connected to MCU address line A13 — for Narrow modes |
|                  | 3-4 | pin is connected to MCU address line A14 — for Wide modes |
|                  | 5-6 | pin is connected to V_{DD} — for the device's chip enable (CE2) |
### Table 4-1. Jumper-Selectable Functions (continued)

<table>
<thead>
<tr>
<th>Diagram</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>W14</td>
<td></td>
<td>SCI Port Assignment to Terminal Interface</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>SCI port 0 serves as the D-Bug12 terminal interface</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>SCI port 1 serves as the D-Bug12 terminal interface</td>
</tr>
<tr>
<td>W20</td>
<td></td>
<td>D-Bug12 (normal) or EEPROM (alternate) Execution Mode</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>the code in on-chip EEPROM is executed out of reset</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>D-Bug12 is executed out of reset</td>
</tr>
<tr>
<td>W21</td>
<td></td>
<td>TXD0 — RS-232C Transmit Data (TXD) Enable, SCI Port 0</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>TXD on SCI port 0 is enabled</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>TXD on SCI port 0 is disabled</td>
</tr>
<tr>
<td>W22</td>
<td></td>
<td>ROM Pin Assignment — pin 31 of 32-pin package</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>pin is connected to MCU address line A18 — for Narrow modes</td>
</tr>
<tr>
<td></td>
<td>3-4</td>
<td>pin is connected to MCU address line A19 — for Wide modes</td>
</tr>
<tr>
<td></td>
<td>5-6</td>
<td>pin is connected to VDD — to disable the device's write enable (WE*)</td>
</tr>
<tr>
<td>W23</td>
<td></td>
<td>ROM Pin Assignment — pin 30 of 32-pin package or pin 28 of 28-pin package</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>pin is connected to MCU address line A17 — for Narrow modes</td>
</tr>
<tr>
<td></td>
<td>3-4</td>
<td>pin is connected to MCU address line A18 — for Wide modes</td>
</tr>
<tr>
<td></td>
<td>5-6</td>
<td>pin is connected to VDD — for 28-pin devices</td>
</tr>
<tr>
<td>W24</td>
<td></td>
<td>ROM Pin Assignment — pin 29 of 32-pin package or pin 27 of 28-pin package</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>pin is connected to MCU address line A14 — for Narrow modes</td>
</tr>
<tr>
<td></td>
<td>3-4</td>
<td>pin is connected to MCU address line A15 — for Wide modes</td>
</tr>
<tr>
<td></td>
<td>5-6</td>
<td>pin is connected to VDD — to disable the device's write enable (WE*)</td>
</tr>
<tr>
<td>W30</td>
<td></td>
<td>MCU Background Mode Select</td>
</tr>
<tr>
<td><img src="image" alt="Diagram" /></td>
<td>1-2</td>
<td>MCU's BKGD pin is connected to VSS</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>MCU's BKGD pin is connected to VDD</td>
</tr>
</tbody>
</table>
Table 4-1. Jumper-Selectable Functions (continued)

<table>
<thead>
<tr>
<th>Diagram</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W32</strong>&lt;sup&gt;(2)&lt;/sup&gt; ROM Pin Assignment — pin 28 of 32-pin package or pin 26 of 28-pin package</td>
<td>1-2</td>
<td>pin is connected to MCU address line A13 — for Narrow modes</td>
</tr>
<tr>
<td>2 4 6</td>
<td>3-4</td>
<td>pin is connected to MCU address line A14 — for Wide modes</td>
</tr>
<tr>
<td></td>
<td>5-6</td>
<td>pin is connected to V&lt;sub&gt;DD&lt;/sub&gt; — to enable the device's chip enable (CE2)</td>
</tr>
<tr>
<td>1 3 5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| **W33**<sup>(2)</sup> ROM Pin Assignment — pin 3 of 32-pin package or pin 1 of 28-pin package | 1-2 | pin is connected to MCU address line A15 — for Narrow modes |
| 2 4 6 | 3-4 | pin is connected to MCU address line A16 — for Wide modes |
| | 5-6 | pin is connected to V<sub>DD</sub> — for ROM program voltage (V<sub>PP</sub>) |
| 1 3 5 | |

| **W34**<sup>(3)</sup> MCU MODB Select | 1-2 | MCU's PE6/MODB pin is connected to V<sub>SS</sub> |
| 2 3 | 2-3 | MCU's PE6/MODB pin is connected to V<sub>DD</sub> |

| **W36**<sup>(2)</sup> ROM Pin Assignment — pin 2 of 32-pin package | 1-2 | pin is connected to MCU address line A16 — for Narrow modes |
| 2 4 6 | 3-4 | pin is connected to MCU address line A17 — for Wide modes |
| | 5-6 | pin is connected to V<sub>DD</sub> |
| 1 3 5 | |

| **W42**<sup>(3)</sup> MCU MODA Select | 1-2 | MCU's PE5/MODA pin is connected to V<sub>SS</sub> |
| 2 3 | 2-3 | MCU's PE5/MODA pin is connected to V<sub>DD</sub> |

**NOTES:**

<sup>(1)</sup> W12 and W13 together select the type of RAM installed.
<sup>(2)</sup> W22, W24, W29, W32, W33, and W36 together select the type of ROM installed.
<sup>(3)</sup> W30, W34, and W42 together determine the MCU's mode of operation.
4.3 POWER INPUT CIRCUITRY

The input power connector on the EVB is a 2-pin, lever-actuated connector (J6), illustrated in Figure 2-1. Fuse F1 (1.5 amp), Zener diode VR1, and diode CR1 provide over-voltage and reverse-polarity protection. Decoupling capacitors filter ripple and noise from the supply voltage. A red LED (DS1) serves as the power-on indicator.

Cut-trace header footprints (see section 4.2) on the EVB allow isolating the VSS (ground) and VDD (+Vdc) power circuits for different functional areas. These individually filtered circuits can then be connected to separate power sources. This can be helpful for purposes such as power-usage analysis. The following power circuits can be isolated:

- VSS / VDD — MCU core usage
- VSSX0 / VDDX0, VSSX1 / VDDX1, VSSX2 / VDDX2 — three separate circuits for MCU I/O pins
- VSSPLL / VDDPLL — Phase-Locked Loop (PLL)
- VSSA / VDDA, VRL / VRH — A/D Converter power and reference voltages

Refer to the EVB schematic diagram to locate the cut-trace header footprint that isolate these circuits.

4.4 TERMINAL INTERFACE

An RS-232C transceiver (U5B) links the MCU’s two Serial Communications Interfaces (SCI0 and SCI1) with separate RS-232C ports on the EVB. One of these ports (SCI0 by default) serves as the terminal interface for D-Bug12 operation. The other port is available for user applications. The communications parameters for these ports are described in 2.5 Terminal Communications Setup.

There are two possible connectors for each port — a right-angle DB-9 receptacle wired as DCE (for standard RS-232C cabling) and a functionally equivalent 3-pin header (for customized cabling). SCI0 uses connectors J3 or J4; SCI1 uses connectors J1 or J2. The pin assignments for these connectors are listed in Table 2-1. Note that the EVB’s serial ports use only three of the RS-232C signals: Receive Data (RXD), Transmit Data (TXD), and Ground (GND).

To change the D-Bug12 terminal port from SCI0 (the factory default) to SCI1, move the jumper on header W14 to pins 2-3, as shown in Table 4-1. Header J1 can then be used for the terminal port connection without further hardware modification. If a standard RS-232C cable connection is needed for this port, install a right-angle DB-9 receptacle in the footprint for J2 (not populated at the factory).

The EVB’s RS-232C output signals (Transmit Data) can be disabled by setting the jumpers on headers W10 and W21, as shown in Table 4-1.
4.5 MICROCONTROLLER

The MC68HC812A4 is the first of a family of next generation M68HC11 microcontrollers with on-chip memory and peripheral functions. The CPU12 is a high-speed, 16-bit processing unit. The programming model and stack frame are identical to those of the standard M68HC11 CPU. The CPU12 instruction set is a proper superset of the M68HC11 instruction set. All M68HC11 instruction mnemonics are accepted by CPU12 assemblers with no changes.

The EVB-resident MC68HC812A4 (U8) has seven modes of operation. These modes are determined at reset by the state of three mode pins — BKGD, MODB, and MODA — as shown in Table 4-2.

The EVB is factory-configured for MCU operation in the Normal Expanded Wide (x16) mode. In this mode of operation, the expanded bus is present with a 16-bit data bus. Port D is the low byte data bus and Port C is the high byte data bus. Table 3-5, the Factory-Configuration Memory Map, lists the MCU resource usage in this default configuration.

In the Normal Expanded Narrow (x8) mode of operation, the expanded bus is present with an 8-bit data bus. Port C functions as the data bus in this mode. Port D is available for general purpose I/O.

In the Normal Single Chip mode of operation, no external bus is available. All program and data fetches are from on-chip memory or peripheral registers. Ports A, B, C, and D are available for general purpose I/O.

The Special Peripheral mode of operation is a test mode. The CPU is not active. On-chip peripherals may be accessed directly by an external bus master. It is not possible to change from or to this mode without going through reset.
The Special Expanded Wide, Special Expanded Narrow, and Special Single Chip modes provide basically the same functionality as the respective normal modes. These special modes are primarily for testing and provide access to several key features, including:

Special Expanded Narrow — to view 16-bit accesses without changing the instruction cycle times, port D may be used to view the upper 8 bits of the data bus.

Special Single Chip — background debug mode is immediately active out of reset. Execution begins from the background debug ROM. Commands are sent to the CPU through the background debug interface pin. A background debug interface is required, as described in section 4.12.

For more information on the CPU, refer to the CPU12 Reference Manual.

<table>
<thead>
<tr>
<th>BKGD Header W30</th>
<th>MODB Header W34</th>
<th>MODA Header W42</th>
<th>Mode Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (2)</td>
<td>0 (2)</td>
<td>0 (2)</td>
<td>Special Single Chip</td>
</tr>
<tr>
<td>0 (2)</td>
<td>0 (2)</td>
<td>1 (1)</td>
<td>Special Expanded Narrow</td>
</tr>
<tr>
<td>0 (2)</td>
<td>1 (1)</td>
<td>0 (2)</td>
<td>Special Peripheral</td>
</tr>
<tr>
<td>0 (2)</td>
<td>1 (1)</td>
<td>1 (1)</td>
<td>Special Expanded Wide</td>
</tr>
<tr>
<td>1 (1)</td>
<td>0 (2)</td>
<td>0 (2)</td>
<td>Normal Single Chip</td>
</tr>
<tr>
<td>1 (1)</td>
<td>0 (2)</td>
<td>1 (1)</td>
<td>Normal Expanded Narrow</td>
</tr>
<tr>
<td>1 (1)</td>
<td>1 (1)</td>
<td>0 (2)</td>
<td>Reserved (currently defaults to peripheral mode)</td>
</tr>
<tr>
<td>1 (1)</td>
<td>1 (1)</td>
<td>1 (1)</td>
<td>Normal Expanded Wide</td>
</tr>
</tbody>
</table>

(1) Install jumper on header pins 2 and 3.
(2) Install jumper on header pins 1 and 2.
4.6 MEMORY

4.6.1 Memory Types and Sockets

The EVB has footprints for two SRAM sockets (U4, U6A) and two ROM sockets (U7, U9A). The ROM sockets hold memory for D-Bug12, the EVB operating firmware, or for user programs. The SRAM sockets hold memory for user data or programs. The 8-bit memory arrangement allows MCU operation in both single-byte and double-byte modes. The RAM and ROM footprints support different memory device types (SRAM, EPROM, and EEPROM) and sizes (28- and 32-pin, 8 to 512 Kbytes, 300 or 600-mil spacing). Figure 4-1 shows how the external memory sockets are used.

Table 3-5 depicts the EVB’s default memory usage. Note that the map is valid only for the factory-supplied memory configuration.

Note that the user-available area in factory-supplied EPROM requires that the ROM chips be reprogrammed with the custom code. For more information, refer to Appendix E Customizing the EPROMs.
Because the EVB is factory-configured for the MCU’s Normal Expanded Wide mode, the two RAM and the two ROM sockets are populated with 8-bit memory devices. Only the 600-mil footprints are populated with sockets. There are two RAM and six ROM jumper headers that allow configuration of the memory sockets for use with various types and sizes of memory. These headers are preset for the factory-supplied memories. The default and optional settings are described in Table 4-1. Table 4-3 provides information about the supplied memories.
Table 4-3. EVB Memories Supplied

<table>
<thead>
<tr>
<th>Type</th>
<th>EPROM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>Atmel</td>
<td>Dallas</td>
</tr>
<tr>
<td>Part Number</td>
<td>AT27LV256R-20PC</td>
<td>DS2064</td>
</tr>
<tr>
<td>Size</td>
<td>256K bits (32K x 8)</td>
<td>64K bits (8K x 8)</td>
</tr>
<tr>
<td>Package Width</td>
<td>600 MIL</td>
<td>600 mil</td>
</tr>
<tr>
<td>Pin Count</td>
<td>28 pin</td>
<td>28 pin</td>
</tr>
<tr>
<td>Power Supply</td>
<td>+3.0 to +5.5 Vdc</td>
<td>+2.7 to +5.5 Vdc</td>
</tr>
<tr>
<td>Access Times</td>
<td>200 ns</td>
<td>150 ns @ 5V, 300 ns @ 3V</td>
</tr>
<tr>
<td>Wait States Required</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

4.6.2 Chip Selects

Header W11 connects an MCU chip select signal to memory devices in the ROM (U7, U9A, U9B) and RAM (U4, U6A, U6B) sockets. Pins in columns 1 and 2 determine the chip select used for memory devices in ROM sockets. Pins in columns 2 and 3 determine the chip select used for memory devices in RAM sockets.

Figure 4-2 shows the W11 jumper settings for the factory-default memory configuration. The illustration demonstrates the correct settings for CSP0* to serve as the ROM chip select and CSD* to serve as the RAM chip select.
4.6.3 Glue Logic

Glue logic is required for the MCU to operate with 8-bit memory devices in Wide Expanded modes. It is not needed in Narrow Expanded modes. The EVB allows either an OR gate (U3 — factory-supplied) or a PAL array (U2 — optional, not populated) to serve as the glue logic. Figure 4-3 shows the circuitry for the ROM and RAM logic.
4.7 CLOCK CIRCUITRY

The EVB comes with a 16-MHz crystal oscillator installed in a 14-pin DIP socket (XY2). The socket wiring allows the use of various types of oscillator packages. Additionally, there is ancillary circuitry that includes a footprint for a discrete crystal (Y1). This flexible arrangement facilitates the construction of custom oscillators. When designing a custom oscillator, refer to the EVB schematic diagram to locate the applicable components and the headers that must be changed.
An external clock input can be supplied to the MCU’s EXTAL by installing a right-angle BNC connector in footprint J7. Refer to the EVB schematic diagram to locate the headers that must be changed.

4.8 PHASE-LOCKED LOOP (PLL)

The PLL can be used to run the MCU on a time base that differs from the clock frequency. To alter the time base, capacitors must be installed between the MCU’s XFC pin and the PLL’s ground reference, VSS\textsubscript{PLL}. Connection points E4, E5, E6, E7, E8, and E9 provide space for these capacitors. Header footprint W37 connects the XFC pin to the capacitors.

For more information, refer to the EVB schematic diagram. More detailed information on the operation of the PLL is found in the \textit{MC68HC812A4 Technical Summary}.

4.9 RESET

The reset circuit includes a pull-up resistor, debounce capacitor, and optional connection to an installed undervoltage sensing device (U1, as described in section 4.10). The reset circuit drives the MCU’s RESET* pin directly.

4.10 LOW-VOLTAGE INHIBIT

Low voltage inhibition (LVI) uses a Motorola undervoltage sensing device (U1) to automatically drive the MCU’s RESET* pin low whenever V\textsubscript{DD} is below legal limits (2.8 V\textsubscript{dc} typical). This prevents the accidental corruption of EEPROM data if the power-supply voltage should drop below the allowable level. Header W1 allows for the disconnection of the LVI circuit.

4.11 ANALOG-TO-DIGITAL (A/D) CONVERTER

The MCU’s A/D converter is fully documented in the \textit{MC68HC812A4 Technical Summary}.

Note that two of the A/D bus lines, PAD0 and PAD1, are used by the EVB and D-Bug12 for configuration purposes. These lines are not available for A/D usage in the factory-default configuration.

The accuracy of the A/D converter can be increased by supplying the MCU’s A/D circuitry with the same supply voltages used by the target hardware. These supply lines (V\textsubscript{DDA} and V\textsubscript{SSA}) and the associated A/D reference voltages (V\textsubscript{THT} and V\textsubscript{RL}) can be isolated from the EVB’s power bus with cut-trace footprints W15, W16, W17, and W18. Refer to the EVB schematic diagram for details.
4.12 BACKGROUND DEBUG MODE (BDM) INTERFACE

The MCU's serial BDM interface can be accessed through J5, a 2x3 header. The pin assignments are shown in Table 4-4.

Note that the BDM interface requires a development tool such as Motorola's Serial Debug Interface. For more information, refer to Appendix F and to the Motorola Serial Debug Interface User's Manual.

Table 4-4. BDM Connector J5 Pin Assignments

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BKGD</td>
</tr>
<tr>
<td>2</td>
<td>Vss</td>
</tr>
<tr>
<td>3</td>
<td>no connection</td>
</tr>
<tr>
<td>4</td>
<td>RESET*</td>
</tr>
<tr>
<td>5</td>
<td>no connection</td>
</tr>
<tr>
<td>6</td>
<td>Vdd</td>
</tr>
</tbody>
</table>

4.13 PROTOTYPE AREA

The EVB's prototype area allows construction of custom I/O circuitry that can be connected to the MCU's I/O lines through connectors J8 and J9. This 2-inch by 8-inch area is a grid of holes (79 by 20) on 1/10-inch centers. This spacing accommodates most sockets, headers, and device packages..

Figure 4-4 shows the component-side view of the prototype area. Ground (Vss) connections are provided along the three outboard peripheries, with three loop-style test points for connecting clips or probes. Vdc (Vdd) connections are provided along the inboard periphery.
Figure 4-4. Prototype Area (Component-Side View)
4.14 MCU CONNECTORS

Two 2x30 pin header connectors, J8 and J9, provide access to the MCU’s I/O and bus lines. These connectors are located adjacent to the prototype area for use as described in section 4.13. They also provide connection points for instrumentation probes and interfaces to target hardware. Figure 4-5 and Figure 4-6 depict the pin assignments for J8 and J9. Table 4-5 and Table 4-6 provide descriptions of the signals.

Note that the EXTAL, XFC, and XTAL signals are not directly connected to these headers due to impedance considerations. Header footprints W37, W38, and W39 can be used to make these connections.

```
PJ6  1  ●  ●  2  PJ7
PJ4  3  ●  ●  4  PJ5
PJ2  5  ●  ●  6  PJ3
PJ0  7  ●  ●  8  PJ1
VSSEX0 9  ●  ●  10  VDDEX0
PG4  11  ●  ●  12  PG5
PG2  13  ●  ●  14  PG3
PG0  15  ●  ●  16  PG1
VSSI  17  ●  ●  18  VDDI
BKGD 19  ●  ●  20  NC
PC6  21  ●  ●  22  PC7
PC4  23  ●  ●  24  PC5
PC2  25  ●  ●  26  PC3
PC0  27  ●  ●  28  PC1
PD6  29  ●  ●  30  PD7
PD4  31  ●  ●  32  PD5
PD2  33  ●  ●  34  PD3
PD0  35  ●  ●  36  PD1
PE6  37  ●  ●  38  PE7
PE4  39  ●  ●  40  PE5
PE2  41  ●  ●  42  PE3
PE0  43  ●  ●  44  PE1
NC  45  ●  ●  46  NC
RESET* 47  ●  ●  48  XFC
VSSPLL 49  ●  ●  50  VDDPLL
XTAL  51  ●  ●  52  EXTAL
PB6  53  ●  ●  54  PB7
PB4  55  ●  ●  56  PB5
PB2  57  ●  ●  58  PB3
PB0  59  ●  ●  60  PB1
```

Figure 4-5. MCU Connector J8 (Component-Side View)
<table>
<thead>
<tr>
<th>VSSEX1</th>
<th>1</th>
<th></th>
<th>2</th>
<th>VDDEX1</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA6</td>
<td>3</td>
<td></td>
<td>4</td>
<td>PA7</td>
</tr>
<tr>
<td>PA4</td>
<td>5</td>
<td></td>
<td>6</td>
<td>PA5</td>
</tr>
<tr>
<td>PA2</td>
<td>7</td>
<td></td>
<td>8</td>
<td>PA3</td>
</tr>
<tr>
<td>PA0</td>
<td>9</td>
<td></td>
<td>10</td>
<td>PA1</td>
</tr>
<tr>
<td>PF6</td>
<td>11</td>
<td></td>
<td>12</td>
<td>NC</td>
</tr>
<tr>
<td>PF4</td>
<td>13</td>
<td></td>
<td>14</td>
<td>PF5</td>
</tr>
<tr>
<td>PF2</td>
<td>15</td>
<td></td>
<td>16</td>
<td>PF3</td>
</tr>
<tr>
<td>PF0</td>
<td>17</td>
<td></td>
<td>18</td>
<td>PF1</td>
</tr>
<tr>
<td>VSSAD</td>
<td>19</td>
<td></td>
<td>20</td>
<td>VDDAD</td>
</tr>
<tr>
<td>PAD6</td>
<td>21</td>
<td></td>
<td>22</td>
<td>PAD7</td>
</tr>
<tr>
<td>PAD4</td>
<td>23</td>
<td></td>
<td>24</td>
<td>PAD5</td>
</tr>
<tr>
<td>PAD2</td>
<td>25</td>
<td></td>
<td>26</td>
<td>PAD3</td>
</tr>
<tr>
<td>PAD0</td>
<td>27</td>
<td></td>
<td>28</td>
<td>PAD1</td>
</tr>
<tr>
<td>VRL</td>
<td>29</td>
<td></td>
<td>30</td>
<td>VRH</td>
</tr>
<tr>
<td>PH6</td>
<td>31</td>
<td></td>
<td>32</td>
<td>PH7</td>
</tr>
<tr>
<td>PH4</td>
<td>33</td>
<td></td>
<td>34</td>
<td>PH5</td>
</tr>
<tr>
<td>PH2</td>
<td>35</td>
<td></td>
<td>36</td>
<td>PH3</td>
</tr>
<tr>
<td>PH0</td>
<td>37</td>
<td></td>
<td>38</td>
<td>PH1</td>
</tr>
<tr>
<td>VSSEX2</td>
<td>39</td>
<td></td>
<td>40</td>
<td>VDDEX2</td>
</tr>
<tr>
<td>PS6</td>
<td>41</td>
<td></td>
<td>42</td>
<td>PS7</td>
</tr>
<tr>
<td>PS4</td>
<td>43</td>
<td></td>
<td>44</td>
<td>PS5</td>
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<tr>
<td>PS2</td>
<td>45</td>
<td></td>
<td>46</td>
<td>PS3</td>
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<tr>
<td>PS0</td>
<td>47</td>
<td></td>
<td>48</td>
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<td>PT6</td>
<td>49</td>
<td></td>
<td>50</td>
<td>PT7</td>
</tr>
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<td>PT4</td>
<td>51</td>
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<td>52</td>
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<td>PT2</td>
<td>53</td>
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<td>54</td>
<td>PT3</td>
</tr>
<tr>
<td>PT0</td>
<td>55</td>
<td></td>
<td>56</td>
<td>PT1</td>
</tr>
<tr>
<td>VSS</td>
<td>57</td>
<td></td>
<td>58</td>
<td>VDD</td>
</tr>
<tr>
<td>VSS</td>
<td>59</td>
<td></td>
<td>60</td>
<td>VDD</td>
</tr>
</tbody>
</table>

Figure 4-6. MCU Connector J9 (Component-Side View)
### Table 4-5. MCU Connector J8 Pin Assignments

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Mnemonic</th>
<th>Signal Name And Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PJ6/KWJJ6</td>
<td>PORT J (bits 0-7) — general purpose I/O or key wake-up</td>
</tr>
<tr>
<td>2</td>
<td>PJ7/KWJJ7</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PJ4/KWJJ4</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PJ5/KWJJ5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PJ2/KWJJ2</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PJ3/KWJJ3</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PJ0/KWJJ0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>PJ1/KWJJ1</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>VSSEX0</td>
<td>VSSX/VDDX — external (V_{SS}) and (V_{DD}) connections</td>
</tr>
<tr>
<td>10</td>
<td>VDDEX0</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>PG4/A20</td>
<td>PORT G (bits 0-5) — general purpose I/O or memory expansion lines</td>
</tr>
<tr>
<td>12</td>
<td>PG5/A21</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>PG2/A18</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>PG3/A19</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>PG0/A16</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PG1/A17</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>VSSI</td>
<td>VSSI/VDDI — internal (V_{SS}) and (V_{DD}) connections for the MCU</td>
</tr>
<tr>
<td>18</td>
<td>VDDI</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>BKGD</td>
<td>BACKGROUND — an I/O line dedicated to the background debug function. If it is a zero out of reset then the MCU is in special mode. This pin can be used for bi-directional communications with the MCU.</td>
</tr>
<tr>
<td>20</td>
<td>NC</td>
<td>not connected</td>
</tr>
<tr>
<td>21</td>
<td>PC6/D14/D6</td>
<td>PORT C (bits 0-7) — general purpose I/O or data bus</td>
</tr>
<tr>
<td>22</td>
<td>PC7/D15/D7</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>PC4/D12/D4</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>PC5/D13/D5</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PC2/D10/D2</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>PC3/D11/D3</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>PC0/D8/D0</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>PC1/D9/D1</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>PD6/D6/KWJD8</td>
<td>PORT D (bits 0-7) — general purpose I/O, data bus, or key wake-up</td>
</tr>
<tr>
<td>30</td>
<td>PD7/D7/KWJD7</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>PD4/D4/KWJD4</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>PD5/D5/KWJD5</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>PD2/D2/KWJD2</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>PD3/D3/KWJD3</td>
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</tr>
<tr>
<td>35</td>
<td>PD0/D0/KWJD0</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>PD1/D1/KWJD1</td>
<td></td>
</tr>
<tr>
<td>Pin Number</td>
<td>Signal Mnemonic</td>
<td>Signal Name And Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>37</td>
<td>PE6/MODB/IPipe1</td>
<td>PORT E (bits 0-7) — general purpose I/O or external signals such as mode select, auxiliary reset, E clock, read/write, strobe low, XIRQ, and IRQ</td>
</tr>
<tr>
<td>38</td>
<td>PE7/ARSIE</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>PE4/E</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>PE5/MODA/IPipe0</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>PE2/RW*</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>PE3/LSTRB*</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>PE0/XIRQ*</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>PE1/IRQ*</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>NC</td>
<td>not connected</td>
</tr>
<tr>
<td>46</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>RESET*</td>
<td>Reset — active-low bi-directional control line used to initialize the MCU</td>
</tr>
<tr>
<td>48</td>
<td>XFC</td>
<td>XFC — optional filter-capacitor connection for PLL circuit</td>
</tr>
<tr>
<td>49</td>
<td>VSSPLL</td>
<td>VSSPLL/VDDPLL — $V_{SS}$ and $V_{DD}$ connections for the PLL circuit.</td>
</tr>
<tr>
<td>50</td>
<td>VDDPLL</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>XTAL</td>
<td>CRYSATL OUTPUT — crystal oscillator output</td>
</tr>
<tr>
<td>52</td>
<td>EXTAL</td>
<td>EXTERNAL CLOCK INPUT — crystal oscillator input. The frequency applied to this pin must be twice the desired bus speed.</td>
</tr>
<tr>
<td>53</td>
<td>PB6/A8</td>
<td>PORT B (bits 0-7) — general purpose I/O or low byte address bus</td>
</tr>
<tr>
<td>54</td>
<td>PB7/A7</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>PB4/A4</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>PB5/A5</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>PB2/A2</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>PB3/A3</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>PB0/A0</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>PB1/A1</td>
<td></td>
</tr>
<tr>
<td>Pin Number</td>
<td>Signal Mnemonic</td>
<td>Signal Name And Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>1</td>
<td>VSSEX1</td>
<td>VSSX/VDDX — external $V_{SS}$ and $V_{DD}$ connections</td>
</tr>
<tr>
<td>2</td>
<td>VDDEX1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PA8/A14</td>
<td>PORT A (bits 0-7) — general purpose I/O or high byte address bus</td>
</tr>
<tr>
<td>4</td>
<td>PA7/A15</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PA4/A12</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PA5/A13</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PA2/A10</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>PA3/A11</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>PA0/A8</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>PA1/A9</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>PF6/CSP1*</td>
<td>PORT F (bit 6) — general purpose I/O or chip select</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>not connected</td>
</tr>
<tr>
<td>13</td>
<td>PF4/CSD*</td>
<td>PORT F (bits 0-5) — general purpose I/O port or chip selects</td>
</tr>
<tr>
<td>14</td>
<td>PF5/CSP0*</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>PF2/CS2*</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PF3/CS3*</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>PF0/CS0*</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>PF1/CS1*</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>VSSAD</td>
<td>VSSAD/VDDAD — $V_{SS}$ and $V_{DD}$ connections for the MCU's A/D converter</td>
</tr>
<tr>
<td>20</td>
<td>VDDAD</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>PAD6</td>
<td>PORT AD — A/D converter channel or general purpose I/O</td>
</tr>
<tr>
<td>22</td>
<td>PAD7</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>PAD4</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>PAD5</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PAD2</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>PAD3</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>PAD0</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>PAD1</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>VRL</td>
<td>VOLTAGE REFERENCE, LOW and HIGH — reference voltages for the MCU's A/D converter. These can improve the accuracy of A/D conversions.</td>
</tr>
<tr>
<td>30</td>
<td>VRH</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>PH6/KWUH6</td>
<td>PORT H (bits 0-7) — general purpose I/O or key wake-up</td>
</tr>
<tr>
<td>32</td>
<td>PH7/KWUH7</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>PH4/KWUH4</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>PH5/KWUH5</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>PH2/KWUH2</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>PH3/KWUH3</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>PH0/KWUH0</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>PH1/KWUH1</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>VSSEX2</td>
<td>VSSX/VDDX — external $V_{SS}$ and $V_{DD}$ connections</td>
</tr>
<tr>
<td>340</td>
<td>VDDEX2</td>
<td></td>
</tr>
</tbody>
</table>
Table 4-6. MCU Connector J9 Pin Assignments (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Mnemonic</th>
<th>Signal Name And Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>41</td>
<td>PS6/SCK</td>
<td>PORT S (bits 0-7) — general purpose I/O or Multiple Serial Interface (MSI) lines. The MSI lines consist of serial peripheral and serial communication interfaces. The signal functions are serial clock, slave select, master in/slave out, master out/slave in, receiver data input, and transmitter data out.</td>
</tr>
<tr>
<td>42</td>
<td>PS7/SS*</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>PS4/MISO</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>PS5/MOSI</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>PS2/RXD1</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>PS3/TXD1</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>PS0/RXD0</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>PS1/TXD0</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>PT6/IOC6</td>
<td>PORT T (bits 0-7) — general purpose I/O or timer lines</td>
</tr>
<tr>
<td>50</td>
<td>PT7/IOC7/PAIN</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>PT4/IOC4</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>PT5/IOC5</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>PT2/IOC2</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>PT3/IOC3</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>PT0/IOC0</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>PT1/IOC1</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>VSS</td>
<td>VSS/VDD — EVB system return (Vss) and power (Vdd)</td>
</tr>
<tr>
<td>58</td>
<td>VDD</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>VSS</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>VDD</td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX A
S-RECORD FORMAT

DESCRIPTION

The S-record format for output modules was devised for the purpose of encoding programs or data files in a printable format for transportation between computer systems. The transportation process can thus be visually monitored and the S-records can be more easily edited.

S-RECORD CONTENT

When viewed by the user, S-records are essentially character strings made of several fields that identify the record type, record length, memory address, code/data, and checksum. Each byte of binary data is encoded as a 2-character hexadecimal number: the first character represents the high-order 4 bits, and the second represents the low-order 4 bits of the byte.

The 5 fields that comprise an S-record are shown below:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>RECORD LENGTH</th>
<th>ADDRESS</th>
<th>CODE/DATA</th>
<th>CHECKSUM</th>
</tr>
</thead>
</table>

The S-Record fields are composed as follows:

<table>
<thead>
<tr>
<th>Field</th>
<th>Printable Characters</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>2</td>
<td>S-record type - S0, S1, etc.</td>
</tr>
<tr>
<td>Record length</td>
<td>2</td>
<td>The count of the character pairs in the record, excluding the type and record length.</td>
</tr>
<tr>
<td>Address</td>
<td>4, 6, or 8</td>
<td>The 2-, 3-, or 4-byte address at which the data field is to be loaded into memory.</td>
</tr>
<tr>
<td>Code/data</td>
<td>0-2n</td>
<td>From 0 to n bytes of executable code, memory-loadable data, or descriptive information. For compatibility with teletypewriters, some programs may limit the number of bytes to as few as 28 (56 printable characters in the S-record).</td>
</tr>
<tr>
<td>Checksum</td>
<td>2</td>
<td>The least significant byte of the one's complement of the sum of the values represented by the pairs of characters making up the record length, address, and the code/data fields.</td>
</tr>
</tbody>
</table>

Each record may be terminated with a CR/LF/NULL. Additionally, an S-record may have an initial field to accommodate other data such as line numbers generated by some time-sharing systems.

Accuracy of transmission is ensured by the record length (byte count) and checksum fields.

**S-RECORD TYPES**

Eight types of S-records have been defined to accommodate the several needs of the encoding, transportation, and decoding functions. The various Motorola upload, download, and other record transportation control programs, as well as cross assemblers, linkers, and other file-creating or debugging programs, utilize only those S-records that serve the purpose of the program. For specific information on which S-records are supported by a particular program, the user manual for that program must be consulted.

**NOTE**

D-Bug12 supports only the S1 and S9 records. All data before the first S1 record is ignored. Thereafter, all records must be S1 type until the S9 record terminates data transfer.

An S-record format module may contain S-records of the following types:

| S0 | The header record for each block of S-records. The code/data field may contain any descriptive information identifying the following block of S-records. The address field is normally zeroes. |
S-RECORD FORMAT

<table>
<thead>
<tr>
<th>S1</th>
<th>A record containing code/data and the 2-byte address at which the code/data is to reside.</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2-S8</td>
<td>Not applicable to EVB.</td>
</tr>
<tr>
<td>S9</td>
<td>A termination record for a block of S1 records. The address field may optionally contain the 2-byte address of the instruction to which control is to be passed. If not specified, the first entry point specification encountered in the object module input will be used. There is no code/data field.</td>
</tr>
</tbody>
</table>

Only one termination record is used for each block of S-records. Normally, only one header record is used, although it is possible for multiple header records to occur.

S-RECORD EXAMPLE

Shown below is a typical S-record format module, as printed or displayed:

S00600004844521B
S1130000285F245F2212226A000424290008237C2A
S113001000020000800082629001853812341001813
S113002041E900084E42234300182342000824A952
S107003000144ED492
S9030000FC

The above module consists of an S0 header record, four S1 code/data records, and an S9 termination record.

The S0 header record is comprised of the following character pairs:

<table>
<thead>
<tr>
<th>S0</th>
<th>S-record type S0, indicating a header record.</th>
</tr>
</thead>
<tbody>
<tr>
<td>06</td>
<td>Hexadecimal 06 (decimal 6), indicating six character pairs (or ASCII bytes) follow.</td>
</tr>
<tr>
<td>00</td>
<td>Four-character 2-byte address field, zeroes.</td>
</tr>
<tr>
<td>48</td>
<td>ASCII H, D, and R - &quot;HDR&quot;.</td>
</tr>
<tr>
<td>52</td>
<td></td>
</tr>
<tr>
<td>1B</td>
<td>Checksum of S0 record.</td>
</tr>
</tbody>
</table>
The first S1 code/data record is explained as follows:

<table>
<thead>
<tr>
<th>S1</th>
<th>S-record type S1, indicating a code/data record to be loaded/verified at a 2-byte address.</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>Hexadecimal 13 (decimal 19), indicating 19 character pairs, representing 19 bytes of binary data, follow.</td>
</tr>
<tr>
<td>00</td>
<td>Four-character 2-byte address field; hexadecimal address 0000, indicates location where the following data is to be loaded.</td>
</tr>
</tbody>
</table>

The next 16 character pairs are the ASCII bytes of the actual program code/data. In this assembly language example, the hexadecimal opcodes of the program are written in sequence in the code/data fields of the S1 records:

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 5F</td>
<td>BHCC $0161</td>
</tr>
<tr>
<td>24 5F</td>
<td>BCC $0163</td>
</tr>
<tr>
<td>22 12</td>
<td>BHI $0118</td>
</tr>
<tr>
<td>22 6A</td>
<td>BHI $0172</td>
</tr>
<tr>
<td>00 04 24</td>
<td>BRSET 0,04,$012F</td>
</tr>
<tr>
<td>29 00</td>
<td>BHCS $010D</td>
</tr>
<tr>
<td>08 23 7C</td>
<td>BRSET 4,$23,$018C</td>
</tr>
</tbody>
</table>

(Balance of this code is continued in the code/data fields of the remaining S1 records, and stored in memory location 0010, etc.)

* 2A Checksum of the first S1 record.

The second and third S1 code/data records each also contain $13 (19) character pairs and are ended with checksums 13 and 52, respectively. The fourth S1 code/data record contains 07 character pairs and has a checksum of 92.

The S9 termination record is explained as follows:

<table>
<thead>
<tr>
<th>S9</th>
<th>S-record type S9, indicating a termination record.</th>
</tr>
</thead>
<tbody>
<tr>
<td>03</td>
<td>Hexadecimal 03, indicating three character pairs (3 bytes) follow.</td>
</tr>
<tr>
<td>00</td>
<td>Four-character 2-byte address field, zeroes.</td>
</tr>
<tr>
<td>FC</td>
<td>Checksum of S9 record.</td>
</tr>
</tbody>
</table>
Each printable character in an S-record is encoded in hexadecimal (ASCII in this example) representation of the binary bits which are actually transmitted. For example, the first S1 record above is sent as shown below.

<table>
<thead>
<tr>
<th>TYPE</th>
<th>LENGTH</th>
<th>ADDRESS</th>
<th>CODE/DATA</th>
<th>CHECKSUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>1</td>
<td>13</td>
<td>0 0 0 0</td>
<td>2 8 5 F</td>
</tr>
<tr>
<td>3 3 3 1</td>
<td>3 1 3 3 3 0 3 0 3 0 3 0</td>
<td>3 2 3 8 3 5 4 8 3 2 4 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0101 0011 0001 0011 0011 0000 0011 0000 0011 0000 0011 0000 0110 0011 0100 0100</td>
<td>0011 0010 0001 0001</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX B
COMMUNICATIONS PROGRAM EXAMPLES

INTRODUCTION

In all of these examples, first follow the EVB startup procedure in section 3.1. When the startup procedure calls for setting up the host computer's communications program for terminal emulation, follow the steps in the examples.

Keyboard entries are illustrated in this appendix using the following conventions:

- **<ENTER>** Press the keyboard's Enter, Carriage Return, or Return key.
- **<ALT-P>** While holding down the ALTERNATE key, press the P key.
- **<CTL-I>** While holding down the CONTROL key, press the backslash key.
- **<filename>** Supply the appropriate file name when required.

The stepwise procedures in this appendix are as accurate as possible. However, it is not feasible to document all of the communications programs that are available or to guarantee that a newer revision of a program behaves in exactly the same way as the version used to develop the procedure. For this reason, the steps are as generic as possible in their descriptions. They can thus serve as guidelines for programs not exemplified in this manual. *Always consult the documentation for the program being used.*

PROCOMM FOR DOS — IBM PC

Setup

To set up Procomm using DOS on an IBM-compatible PC for use as the EVB terminal, first refer to section 3.1 for the EVB startup procedure, which is inter-related with this example. Then follow these steps:

1. At the DOS prompt, Invoke the Procomm program by typing:
   
   PROCOMM<RETURN>

2. Enter the Setup menu by pressing <ALT-S>.

3. From the TERMINAL SETUP submenu, select the following:
   
   Terminal emulation       WYSE 100
   Duplex                   FULL
Flow control        NONE  
CR translation (in)  CR    
CR translation (out) CR    
BS translation       DEST  
BS key definition    BS    
Line wrap            OFF   
Scroll               ON    
Break Length (ms)    350   
Enquiry (CTRL-E)     OFF   

4. From the ASCII TRANSFER SETUP submenu, select the following:
   Echo locally        YES   
   Expand blank lines  YES   
   Pace character      0 (ASCII)  
   Character pacing    25 (1/1000th sec)  
   Line pacing         10 (1/10th sec)    
   CR translation      NONE  
   LF translation      NONE  

5. Enter the Line Settings menu by pressing <ALT-P>. Select the following:
   baud rate            9600 (or the customized EVB setting)  
   data bits            8     
   stop bits            1     
   parity               none    
   COM port             the host port used as the EVB terminal interface 

6. Reset the EVB by pressing S1 or by activating the appropriate custom reset circuitry.


S-Record Transfers to EVB Memory

To load an S-Record file from the host computer into EVB memory using Procomm on an IBM-compatible host computer, first verify that the host is correctly configured and operating as the EVB terminal. Then follow these steps:

1. At the D-Bug12 prompt, enter the LOAD or VERF command with any parameters.
2. Instruct Procomm to send the S-Record file by pressing the <Page Up> key. Follow the onscreen instructions to select the S-Record file for transfer, using ASCII transfer protocol.

Upon completion of the S-Record file transfer, the D-Bug12 prompt is displayed.

**KERMIT FOR DOS — IBM PC**

**Setup**

To set up Kermit using DOS on an IBM-compatible PC for use as the EVB terminal, first refer to section 3.1 for the EVB startup procedure, which is inter-related with this example. Then follow these steps:

1. At the DOS prompt, invoke Kermit by typing:
   
   kermit<ENTER>

2. Set the baud rate to 9600 (or the customized EVB setting) by typing:
   
   set baud 9600<ENTER>

3. Connect to the EVB by typing:
   
   connect<ENTER>

4. Reset the EVB by pressing S1 or by activating the appropriate custom reset circuitry. The D-Bug12 prompt should appear on the display. Continue with the startup procedure in section 3.1.

**S-Record Transfers to EVB Memory**

To load an S-Record file from the host computer into EVB memory using Kermit on an IBM-compatible host computer, first verify that the host is correctly configured and operating as the EVB terminal. Then follow these steps:

1. At the D-Bug12 prompt, enter the LOAD or VERF command with any parameters.

2. "Escape" from the D-Bug12 prompt and start the Kermit file transfer by typing:
   
   <CTL-]>c
   
   push<ENTER>
   
   type <filename> > com1<ENTER>

Upon completion of the S-Record file transfer, the D-Bug12 prompt is displayed.

**KERMIT — SUN WORKSTATION**
Setup

To set up Kermit on the Sun Workstation for use as the EVB terminal, first refer to section 3.1 for the EVB startup procedure, which is inter-related with this example. Then follow these steps:

1. In a shell window, invoke Kermit by typing:
   
   `kermit<ENTER>`

2. Set the serial port to the one in use for the EVB (ttya, ttyb, etc.) by typing:
   
   `set line /dev/ttya<ENTER>`

3. Set the baud rate to 9600 (or the customized EVB setting) by typing:
   
   `set speed 9600<ENTER>`

4. Connect to the EVB by typing:
   
   `connect<ENTER>`

5. Reset the EVB by pressing S1 or by activating the appropriate custom reset circuitry. The D-Bug12 prompt should appear on the display. Continue with the startup procedure in section 3.1.

S-Record Transfers to EVB Memory

To load an S-Record file from the host computer into EVB memory using Kermit on a Sun Workstation, first verify that the host is correctly configured and operating as the EVB terminal. Then follow these steps:

1. In the shell window being used for the EVB terminal interface, at the D-Bug12 prompt, enter the LOAD or VERF command with any parameters.

2. Open a shell window separate from the one being used for the EVB terminal interface. In this window, type:
   
   `cat <filename> > /dev/ttya<ENTER>`

Upon completion of the S-Record file transfer, the D-Bug12 prompt is displayed in the shell window being used for the EVB terminal interface.
MACTERMINAL — APPLE MACINTOSH

Setup

To set up MacTerminal on an Apple MacIntosh computer for use as the EVB terminal, first refer to section 3.1 for the EVB startup procedure, which is inter-related with this example. Then follow these steps:

1. Select the following from the Terminal Settings menu:
   - Terminal: TTY
   - Cursor Shape: Underline
   - Line Width: 80 Columns
   - Select: On Line
   - Click on: OK

2. Select the following from the Compatibility Settings menu:
   - Baud Rate: 9600 (or the customized EVB setting)
   - Bits per Character: 8 Bits
   - Parity: None
   - Handshake: None
   - Connection: Modem or Another Computer
   - Connection Port: Modem or Printer
   - Click on: OK

3. Reset the EVB by pressing S1 or by activating the appropriate custom reset circuitry.


S-Record Transfers to EVB Memory

To load an S-Record file from the host computer into EVB memory using MacTerminal, first verify that the host is correctly configured and operating as the EVB terminal. Then follow these steps:

1. At the D-Bug12 prompt, enter the LOAD or VERF command with any parameters.

2. From the Macintosh File menu, select Send File - ASCII.

3. From the dialog box, select the S-Record file to be transferred.
4. Click on Send.

NOTES

1. S-Records are not displayed during the file transfer.

2. Following the file transfer, MacTerminal sends a carriage return-line feed pair, which D-Bug12 interprets as an erroneous command. To return to the D-Bug12 prompt, reset the EVB.

RED RYDER — APPLE MACINTOSH

Setup

To set up Red Ryder on an Apple MacIntosh computer for use as the EVB terminal, first refer to section 3.1 for the EVB startup procedure, which is inter-related with this example. Then follow these steps:

1. Launch the Red Ryder program.

2. Set up the Red Ryder parameters as follows:

   9600 baud (or the customized EVB setting)
   8 data bits
   1 stop bit
   no parity
   full duplex

3. Reset the EVB by pressing S1 or by activating the appropriate custom reset circuitry.


S-Record Transfers to EVB Memory

To load an S-Record file from the host computer into EVB memory using Red Ryder, first verify that the host is correctly configured and operating as the EVB terminal. Then follow these steps:

1. At the D-Bug12 prompt, enter the LOAD or VERF command with any parameters.

2. From the MacIntosh File menu, select Send File - ASCII.

3. From the dialog box, select the S-Record file to be transferred.

4. Click on Send.
NOTE

S-Records are not displayed during the file transfer.

Upon completion of the S-Record file transfer, the D-Bug12 prompt is displayed.
APPENDIX C
D-BUG12 STARTUP CODE

The D-Bug12 startup code is located in the EPROMs, U7 and U9A, in the address range $FD80 to $FDFF, as shown in Table 3-5.

To customize this startup code, it is necessary to reprogram the EPROMs. For more information, refer to Appendix E, Customizing the EPROMs.

The following D-Bug12 startup code is distilled from the source listing for clarity. To assemble the startup code for programming into the EPROMs, the .DEFINES must be included ahead of the code listed below. These are available on the Internet at http://www.mot.com/m68hc12.

```
opt    lis ; assembler directive to turn
        ; listing on

0A00   MonRAMStart  equ $0A00
0200   MonRAMSize   equ $0200
0800   RAM_START   equ $0800
0400   RAMSize     equ $0400
0C00   STACKTOP    equ RAM_START+RAMSize ; stack at top of int RAM
1000   EE_START    equ $1000 ; 4K EEPROM located here out
        ; of reset(in expanded modes)
FD80   org $fd80

;******************************************************************************
; INITIALIZATION
;
; Initialization code for the M68HC12A4EVB D-Bug12 monitor program
;******************************************************************************

FD80   CODE_START:

; set PortE bit 7 to an output to eliminate possible noise
; problems associated with unterminated input pins.
```
FD80 4C0980  bset  DDRE,80h ; set the data direction to
              ; configure PortE, bit 7 as an
              ; output.

FD83 4C0880  bset  PORTE,80h ; set PortE, bit 7 to logic 1.

FD86 CF0C00  lds   #STACKTOP ; initialize D-Bug12 stack
              ; pointer

FD89 4F6F0103  brclr  PORTAD,01h,DEBUG12; if bit 0 of A/D port is 1,
FD8D 061000  jmp   EE_START ; then jump to the start of
              ; internal EEPROM
              ; otherwise, remain in D-Bug12

FD90  DEBUG12:

 ; Clear all monitor RAM to start from a known state

FD90 CE0A00  ldx   #MonRAMStart
FD93 6930  ClrRAM:  clr   1,x+ ; clear one and inc pointer
FD95 8E0C00  cpn   #MonRAMStart+MonRAMSize
FD98 26F9  bne   ClrRAM ; loop till RAM clear

 ; Enable pipe signals, E, low strobe and read/write in port E
 ; PIPOE, NECLK, LSTRE and RDWE are write once in normal modes
 ; PEAR [ARSIE:CDLTE :PIPOE :NECLK !LSTRE : RDWE : 0 : 0 ]$0A

FD9A 862C  ldaa  #$2c ; prevent later protection
              ; lock
FD9C 5A0A  staa  PEAR ; PROTLK is write-once

 ; Without changing modes, enable internal visibility
 ; MODE [SMODN: MODB : MODA : ESTR ! IVIS : 0 : EMD : EME ]$0B

FD9E 4C0B08  bset  MODE,$08 ; set IVIS

 ; Disable the COP watchdog by CR2:CR1:CR0 = 0:0:0
 ; COPCTRL = $07 when reset in normal modes
 ; FCME and CRx bits are write once in normal modes

FDA1 790016  clr   COPCTRL ; disable watchdog

 ; Enable Program chip select 0 and Data chip select
 ; CSCTL0 = $20 after reset (CSP0 on others off)
 ; also set data chip select to cover $0000-7FFF (will mirror
 ; to fill space)
 ; internal resources have higher priority in case of overlaps
 ;
 ; CSCTL0[ 0 :CSP1E :CSP0E : CSDE ! CS3E : CS2E : CS1E : CS0E ]$3C
 ; CSCTL1[ 0 :CSP1FL:CSPA21:CSDHF !CS3EP : 0 : 0 : 0 ]$3D

FDA4 8630  ldaa  #$30
FDA6 5A3C  staa  CSCTL0 ; CSP0E and CSDE on
FDA8 8610  ldaa  #$10
FDAA 5A3D  staa  CSCTL1 ; CSD to cover $0000-7FFF
; Set stretch for CSP0 and CSD to 1 extra E-speed cycle per
; access (to accomodate slower external RAM and EPROM)
;
; CSSTR0[ 0 : 0 ]SRP1A :SRP1B !SRP0A :SRP0B :STRDA :STRDB ]$3E
FDAC 8605  ldaa #$05
FDAE 5A3E  staa CSSTR0 ; CSP0E and CSDE on

; Enable EEPROM so D-Bug12 can program/erase bytes
FDB0 86FC  ldaa #$fc ; prevent later protection
             ; lock
FDB2 5AF0  staa EEMCR ; PROTlk is write-once
FDB4 7900F1 clra BPROT ; allow EE program and erase
FDB7 CEFE00 ldx #$fe00 ; point to the table of user
             ; accessible routines.
FDBA 05E30000 jmp [0,x] ; the first entry is a pointer
             ; to main. GO.........

; The following subroutine produces a delay of approximately
; 20 mS, based on the following conditions:
;
; 1.) An 8.00 MHz E-clock
; 2.) Subroutine located in external EPROM - selected by CSP0
; 3.) CSP0 programmed for 1 E-clock stretch
;
; This routine is called by D-Bug12's WriteEEByte() function
; through a pointer stored in the Customization Data Table.

FDBE EEDelay:
FDBE CE2710  ldx #10000 ; load delay count into x
FDC1 09  dsex ; decrement count
FDC2 26FD  bnez  DlyLoop ; loop till done.
FDC4 3D  rts ; return.
APPENDIX D
D-BUG12 CUSTOMIZATION DATA

The Customization Data area, located in EPROM from $FE80 to $FEFF, allows users to change default data parameters used by D-Bug12. The data contained in this area is described by C data structure. The CustomData typedef is shown below. For those unfamiliar with C an assembly language equivalent is also shown. The purpose of each field is explained in the following paragraphs.

typedef struct {
    Byte UserCCR;    /* User CPU Condition Code Register */
    Byte UserB;     /* User CPU B-accumulator */
    Byte UserA;     /* User CPU A-accumulator */
    Address UserX;  /* User CPU X-index register */
    Address UserY;  /* User CPU Y-index register */
    Address UserPC; /* User CPU Program Counter */
    Address UserSP; /* User CPU Stack Pointer */
    unsigned long SysClk;  /* System Clock frequency (in Hz) */
    Address IOBase; /* Base address of the I/O registers */
    unsigned int SCIBaudRegVal; /* Initial SCI BAUD register value */
    Address EEBase; /* Base address of on-chip EEPROM */
    unsigned int EESize;  /* size of the on-chip EEPROM */
    void (*Delay)(void); /* pointer to EEPROM program/erase */
    /* delay routine */
    int AuxCmdCount; /* number of commands in the */
    /* auxiliary command table */
    CmdTblEntryP AuxCmdTableP; /* pointer to the auxiliary command */
    /* table */
} CustomData;

org $FE80

CustomData equ *
UserCCR  dc.b $90 ; User CPU Condition Code Register
UserB dc.b $00 ; User CPU B-accumulator
UserA dc.b $00 ; User CPU A-accumulator
UserX dc.w $0000 ; User CPU X-index register
UserY dc.w $0000 ; User CPU Y-index register
UserPC dc.w $0000 ; User CPU Program Counter
UserSP dc.w $0A00 ; User CPU Stack Pointer
SysClk dc.w 8000000 ; System Clock frequency (in Hz)
IOBase dc.w $0000 ; Base address of the I/O registers
SCIBaudRegVal dc.w 52 ; Initial SCI BAUD register value
EEBase dc.w $1000 ; Base address of the on-chip EEPROM
EESize dc.w 4096 ; Size of the on-chip EEPROM
EEDelay dc.w _EEDELAY ; Address of EEPROM program/erase delay
    /* routine
AuxCmdCount dc.w 0 ; Number of commands in the auxiliary
    /* command table
AuxCmdTableP dc.w $0000 ; Pointer to the auxiliary command table
Initial User CPU Register Values

The first seven fields in the CustomData typedef struct are used to provide default values for the user CPU12 registers. The user CCR value is set to 0x90. This sets the S-bit, disabling the STOP instruction, and the I-bit, inhibiting IRQ interrupts. The X-bit is cleared to allow the use of the XIRQ interrupt as a programmer's abort switch. The user SP value is set to 0x0a00, which is one byte beyond the last on-chip RAM location available to the user. The CPU12 stack pointer points to the last byte pushed onto the stack. All of the other registers contain the value zero.

SysClk Field

The SysClk field is used to inform D-Bug12 of the system clock frequency, M. Its value, in Hz, is set to 8,000,000. The E-clock frequency is the same as the system clock frequency, M. SysClk is used by the D-Bug12 BAUD command in calculating the new value of the SCI Baud register for the requested baud rate.

NOTE

It is the responsibility of the startup code to perform any actions necessary to set the system clock frequency. D-Bug12 DOES NOT set or change the system clock frequency using the SysClk value.

IOBase Field

The IOBase field defines the base address of the I/O registers. This address is used by D-Bug12 when accessing the I/O registers associated with the SCI and when programming or erasing the on-chip EEPROM. On the MC68HC812A4 the I/O registers are mappable to any 2k memory space. Therefore, the IOBase entry should only be a multiple of 2048. The value of IOBase is set to 0x0000 which is the default address of the I/O registers for the MC68HC812A4.

NOTE

It is the responsibility of the startup code to set the base address of the I/O registers. D-Bug12 DOES NOT set or change the I/O register base address.

SCIBaudRegVal Field

The SCIBaudRegVal field is used to set the initial baud rate of the SCI used for console I/O by D-Bug12. Note that the value in SCIBaudRegVal is written directly to the Baud register of the console SCI. The value is NOT the desired baud rate. The calculation of this value is NOT made by D-Bug12 because of the possibility of an invalid Baud register value. Without a valid Baud register value during SCI initialization, D-Bug12 would have no way to inform the user that a problem existed. Not all combinations of baud rates and system clock frequencies produce a valid Baud register value. The formula used to calculate the Baud register value is:

\[ \text{BaudRegVal} = \frac{\text{MCLK}}{16 \times \text{SCIBaudRate}} \]
The initial Baud register value is 52 (0x0034). At a system clock frequency of 8.0 MHz, this sets the communications rate of 9600 baud.

NOTE

Because of the ability to choose either SCI0 or SCI1 for use as the control console, D-Bug12 takes care of initializing the SCI registers. The chosen SCI is set to 8-data bits, 1-start bit, 1-stop bit, and no parity.

EEBase and EESize Fields

The EEBase and EESize fields are used to describe the base address and range of the M68HC12's on-chip EEPROM. This information is used by D-Bug12's WriteMem() function to determine when a byte is being written to the on-chip EEPROM. D-Bug12 then calls its WriteEEByte() function to place the data in the on-chip EEPROM. On the MC68HC812A4 the EEPROM base address is mappable to any 4k memory space. Therefore, the EEBase entry should only be a multiple of 0x1000. The value of EEBase is set to 0x1000 which is the default base address of the on-chip EEPROM for the MC68HC812A4. The value of EESize is also set to 0x1000 (4096) which is the size of the on-chip EEPROM. Setting the value of EESize to zero disables the WriteMem() function's ability to write to on chip EEPROM.

NOTE

It is the responsibility of the startup code to set the base address of the EEPROM. D-Bug12 DOES NOT set or change the EEPROM base address.

EEPROM Erase/Program Delay Function Pointer Field

The (void) (*)(Delay)(void) field is a function pointer that points to an EEPROM program/erase delay routine. For the MC68HC812A4, the routine should produce a delay of 20 mS before it returns. The delay routine is nothing more than a software delay loop. The subroutine is located in the startup code area of the D-Bug12 EPROM from $FD80 – $FDFF. See Appendix C, D-Bug12 Startup Code.
Auxiliary Command Table Entries

The last two entries in this table provide a mechanism to extend the command set of D-Bug12. The AuxCmdTableP points to an auxiliary command table, and AuxCmdCount contains the number of entries in the auxiliary command table. The table consists of an array of CmdTblEntry's. Each CmdTblEntry in the auxiliary command table has the following structure:

```c
typedef struct {
    const char *CommandStr; /* pointer to the command */
    /* string */
    int (*ExecuteCmd)(int argc, char *argv[]); /* pointer to function that */
    /* implements the command */
} CmdTblEntry, *CmdTblEntryP;
```

As the `typedef` shows, the first field is a character pointer pointing to a null terminated character array containing the command name. The command name string must be in upper case. The second field, a function pointer, points to a function that implements the new D-Bug12 command. The first parameter to this function is a count of the number of command line arguments that the command line interpreter found on the command line. This count includes the command name itself. The command line may contain no more than a total of 10 parameters. The second function parameter is a pointer to an array of char *. Each char * points to one of the command line parameters parsed by the command line interpreter.

The function implementing the new command can report any error conditions to the user in one of two ways. If the error condition can be described by one of the error messages in the enumerated constant list below, the user defined command should return the appropriate constant. If some other message text needs to be conveyed to the user, the command should communicate the error message directly to the user by using the printf() function which is one of the available user callable functions. In this case, the user defined command should return an error code of noErr.

```c
enum Error {
    WrongNumArgs = 6,       /* Wrong Number of Arguments */
    BadStartAddress = 7,    /* Invalid Starting Address */
    BadEndAddress = 8,      /* Invalid Ending Address */
    StartEndError = 9,      /* Start Address Greater Than End Address */
    BadHexData = 10,        /* Invalid Hex Data */
    DataSizeError = 11,     /* Data Out Of Range */
    NoTargetWrite = 12,     /* Can't Write Target Memory */
};
```
APPENDIX E
CUSTOMIZING THE EPROMS

The following blocks in the factory-supplied EPROMs can be reprogrammed with user code or D-Bug12 code that has been modified for custom operation:

$8000 - $9FFF — available for user programs
$FD80 - $FDFF — D-Bug12 startup code. See Appendix C.
$FE80 - $FEFF — D-Bug12 customization data. See Appendix D.
$FF00 - $FFBF — available for user programs

Since the EPROMs also contain D-Bug12 and other EVB operating firmware, the factory programming must be retained and burned into the custom chips along with the custom code. The table below maps the EVB’s logical addresses (from Table 3-5) to the pin-level physical addresses of U7 and U9A.

Note that the lower half of each EPROM — from $0000 to $3FFF — is unused and is filled with ones. This is necessary because of the chip select, CSP0*, used by the MCU for EPROM access. For more information on this subject, refer to 4.6.2 Chip Selects.

NOTE

Do not reprogram the factory-supplied EPROMs. Keep them as masters, using expendable chips for new programming.
### Physical EPROM Addresses

<table>
<thead>
<tr>
<th>MCU Logical Address</th>
<th>Data</th>
<th>U9A Physical Address</th>
<th>U7 Physical Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>$FF</td>
<td>$0000 - $3FFF</td>
<td>$0000 - $3FFF</td>
</tr>
<tr>
<td>$8000 - $9FFE even addresses</td>
<td>custom</td>
<td>$4000 - $4FFF</td>
<td>—</td>
</tr>
<tr>
<td>$8001 - $9FFF odd addresses</td>
<td>custom</td>
<td>—</td>
<td>$4000 - $4FFF</td>
</tr>
<tr>
<td>$A000 - $FD7E even addresses</td>
<td>factory</td>
<td>$5000 - $7EBF</td>
<td>—</td>
</tr>
<tr>
<td>$A001 - $FD7F odd addresses</td>
<td>factory</td>
<td>—</td>
<td>$5000 - $7EBF</td>
</tr>
<tr>
<td>$FD80 - $FDFF even addresses</td>
<td>factory or modified</td>
<td>$7EC0 - $7EFF</td>
<td>—</td>
</tr>
<tr>
<td>$FD81 - $FDFF odd addresses</td>
<td>factory or modified</td>
<td>—</td>
<td>$7EC0 - $7EFF</td>
</tr>
<tr>
<td>$FE00 - $FE7E even addresses</td>
<td>factory</td>
<td>$7F00 - $7F3F</td>
<td>—</td>
</tr>
<tr>
<td>$FE01 - $FE7F odd addresses</td>
<td>factory</td>
<td>—</td>
<td>$7F00 - $7F3F</td>
</tr>
<tr>
<td>$FE80 - $FEFF even addresses</td>
<td>factory or modified</td>
<td>$7F40 - $7F7F</td>
<td>—</td>
</tr>
<tr>
<td>$FE81 - $FEFF odd addresses</td>
<td>factory or modified</td>
<td>—</td>
<td>$7F40 - $7F7F</td>
</tr>
<tr>
<td>$FF00 - $FFBE even addresses</td>
<td>custom</td>
<td>$7F80 - $7FBF</td>
<td>—</td>
</tr>
<tr>
<td>$FF01 - $FFBF odd addresses</td>
<td>custom</td>
<td>—</td>
<td>$7F80 - $7FBF</td>
</tr>
<tr>
<td>$FFC0 - $FFF odd addresses</td>
<td>factory</td>
<td>$7FC0 - $7FFF</td>
<td>—</td>
</tr>
<tr>
<td>$FFC1 - $FFFF odd addresses</td>
<td>factory</td>
<td>—</td>
<td>$7FC0 - $7FFF</td>
</tr>
</tbody>
</table>
APPENDIX F
SDI CONFIGURATION

To configure the EVB for use with Motorola's Serial Debug Interface (SDI), follow these steps:

1. Remove the jumper on header W11 from CSD*.

2. Move the CSP0* jumper on W11 to pins 2-3.
   Steps 1 and 2 disable the external EPROM and map the CSP0* chip select to external RAM.

3. Remove the jumper from W30.
   Step 3 allows the SDI to drive the MCU's BKGD pin low at reset.

4. Move the jumper on W34 to pins 1-2.

5. Move the jumper on W42 to pins 1-2.
   Steps 4 and 5 place the MCU in Special Single Chip mode.

6. Move the base address of the MCU's on-chip EEPROM from $F000 (the default in Special Single Chip mode) to $1000. To do this, change the data at address $0012 to a value of $11 using the appropriate debugging tool. For MCUdebug, the correct command is:
   MM 12 11

   Step 6 must be repeated each time the EVB is reset in this mode, as the EEPROM's base address defaults to $F000 at reset.

Table 4-1 provides full descriptions of these jumper changes. See Figure 4-2 for details of header W11. See Figure 1-1 for header locations on the EVB.

Note that CSP0* covers the address range from $8000 to $FFFF. The 16 Kbytes of RAM appear in the new memory map from $C000 to $FFFF. This SDI memory map is shown in the table below.
This configuration provides the following enhancements when using the SDI:

- The MCU’s on-chip RAM, from $0800 to $0BFF, is entirely available for user data.
- Data can be loaded into the vector area, which was reserved under the D-Bug12 operating configuration.

For information on using the SDI, refer to the *Motorola Serial Debug Interface User’s Manual*.

### SDI Memory Map

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Description</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0000 - $01FF</td>
<td>CPU registers</td>
<td>on-chip (MCU)</td>
</tr>
<tr>
<td>$0800 - $0BFF</td>
<td>user data area</td>
<td>1K on-chip RAM (MCU)</td>
</tr>
<tr>
<td>$1000 - $1FFF</td>
<td>user code area</td>
<td>4K on-chip EEPROM (MCU)</td>
</tr>
<tr>
<td>$C000 - $FFFF</td>
<td>user code/data area</td>
<td>16K external RAM (U4, U8A)</td>
</tr>
</tbody>
</table>
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