Excimer

PowerPC
Embedded Controller Module

Digital DNA
from Motorola
NOTES:

1) Unless otherwise specified:
   All resistors are 1% (0.5% for ±10%).
   All capacitors are ±10%. ±5% for ±10%.
   All inductors are ±10%
   All ferites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   All ferrites are Z=50 ohms at 100 MHz.
   All resistors are ±10%.
   All capacitors are ±10%.
2) Most IC devices shown have default connections to
   appropriate power and ground levels unless shown
   explicitly otherwise.
3) Part numbers used are for reference only; compatible
   parts may be used; refer to the bill of materials.
4) Motorola and the Motorola Colophon are registered
   trademarks of Motorola Inc. IBM and the IBM
   logo are registered trademarks of International
   Business Machines Corporation. PowerPC is a
   trademark of International Business Machines
   Corporation. IBM and the IBM logo are registered
   trademarks of International Business Machines
   Corporation. PowerPC is a trademark of
   International Business Machines Corporation.
   All rights reserved. I've got good news! That
gum you like is going to come back in style. All rights reserved.
5) The sheet-to-sheet cross reference format is:
   Sheet: "X" VertZone Letter HorizZone Number
6) Components surrounded by a dashed/crossed-out line are
   not to be installed by default; they are for test or manufacturing
   purposes only.
7) All buses follow little-endian bit-numbering order (bit 0 is
   the most-significant bit), except where industry standards
   apply (i.e. PCI). Little-endian numbering is noted at the
   source component.

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Excimer
Embedded Controller Module
Version X3
Copyright 1998 by Motorola Inc.
Mates with wall-mount power supply module FRIWO or equivalent. Maximum power needed is 1.5A @ 5V (7.5W).

**HEATSINK REQUIRED**

Heat dissipation depends on the processor used and the bus frequency and PLL multipliers selected.

Excimer w/603R @ 50MHz/300MHz (bus/core):
- 3.3V: 350mA * 1.15W
- 2.5V: 600mA * 1.0W

Power Dissipation:
- 3.3V: 350mA * (5-3.3) = 6.8W
- 2.5V: 600mA * (5-2.5) = 1.0W

A heatsink is recommended for the 2.5V regulator. A "1"x"1" copper fill area on the PCB may be used.

**VCORE OUTPUT**

Normal value is 2.5V. May be changed by changing RA and RB:

\[
\text{VCORE} = 1.25 \times (1 + \frac{RB}{RA}) + 55 \times 10^{-6} \times RB
\]

- 3.3V: 350mA * (5-3.3) = 0.6W
- 2.5V: 600mA * (5-2.5) = 1.5W

A heatsink is recommended for the 2.5V regulator.
1. **System Clock**
   - Replace crystal oscillator with standard 3.3V oscillator to set bus frequency.

2. **Reset Switch**
   - Press switch and power supply monitor.

3. **Diagnostic LEDs**
   - Optional installation. All legend to PCB silkscreen for identification.
Universal 255BGA Symbol

Shows connections for MPGF51, MPGF62 and
MPGF74. Not all pins are present on all devices.
ISP PORT
Optional in-circuit programming of FPGA Options.
smaller SRAMs, the MSB's must be ordered properly.

1) SRAM Address is little endian - LSB is CA0.  
2) Pin 48 and 50 of the MCM69P737 are the MSBs of the address. Ordinarily
   the upper address ordering is unimportant; however, to allow the use of
   smaller SRAMs, the MSB's must be ordered properly.
Flash ROM
NOTE: These little-endian numbered devices are connected to the big-endian-numbered PowerPC bus. While the bits may appear to be reversed, it is correct - the MSB of each device is D15, which is connected to the MSB of the PPC bus (D0).

Sector Protect
Connect to +12V to enable/disable sector protection.
LITTLE ENDIAN DUART
Note bit reversal on changing between big and little-endian devices.

5V ISOLATION BUFFER
CE10 device converts between 5V UART signals to 3.3V PowerPC signals.
Processor debug via BlackBox or ESP/RiscWatch.

COP Connector

NOTE: Connector pin numbering varies widely. This connector shown below is correct as physically viewed from above, with a key at location 14.

Customer Expansion

Unpopulated header for customer expansion. Includes 5V isolated data bus and unused FPGA pins.

Place two-pin Berg adjacent to end of COP header so that it is wound around pins 19 and 20 of a 2x10 Berg with pins 17 and 16 missing.

COP Expansion

TYPICAL CPU PLL SETTINGS