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Introduction

The primary objective of this document is to provide a concise method by which system software and hardware developers and application programmers may more readily provide software that is compatible across the family of PowerPC processors and other devices. A more detailed account of the following topics or the PowerPC architecture in general, may be obtained from the PowerPC Microprocessor Family: The Programming Environments, referred to as The Programming Environments Manual. (The PowerPC Architecture: A Specification for a New Family of RISC Processors defines the architecture from the perspective of the three programming environments and remains the defining document for the PowerPC architecture.)

This document is divided into four parts:

• Part 1, “Register Summary,” on page 4 provides a brief overview of the PowerPC register set, including a programming model and quick reference guides for both 32- and 64-bit registers.
• Part 2, “Memory Control Model,” on page 28 provides a brief outline of the page table entry and segment table entry for both 32- and 64-bit implementations.
• Part 3, “Exception Vectors,” on page 40 provides a quick reference for exception types and the conditions that cause them.
• Part 4, “PowerPC Instruction Set,” on page 41 provides detailed information on the instruction field summary—including syntax and notation conventions. Also included, is the entire PowerPC instruction set, sorted by mnemonic and opcode.

In this document, the term “60x” is used to denote a 32-bit microprocessor from the PowerPC architecture family. 60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

Table 1 contains acronyms and abbreviations that are used in this document. Note that the meanings for some acronyms (such as SDR1 and XER) are historical, and the words for which an acronym stands may not be intuitively obvious.
<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASR</td>
<td>Address space register</td>
</tr>
<tr>
<td>BAT</td>
<td>Block address translation</td>
</tr>
<tr>
<td>BUlD</td>
<td>Bus unit ID</td>
</tr>
<tr>
<td>CR</td>
<td>Condition register</td>
</tr>
<tr>
<td>CTR</td>
<td>Count register</td>
</tr>
<tr>
<td>DAR</td>
<td>Data address register</td>
</tr>
<tr>
<td>DBAT</td>
<td>Data BAT</td>
</tr>
<tr>
<td>DEC</td>
<td>Decrementer register</td>
</tr>
<tr>
<td>DSISR</td>
<td>Register used for determining the source of a DSI exception</td>
</tr>
<tr>
<td>DTLB</td>
<td>Data translation lookaside buffer</td>
</tr>
<tr>
<td>EA</td>
<td>Effective address</td>
</tr>
<tr>
<td>EAR</td>
<td>External access register</td>
</tr>
<tr>
<td>FPR</td>
<td>Floating-point register</td>
</tr>
<tr>
<td>FPSCR</td>
<td>Floating-point status and control register</td>
</tr>
<tr>
<td>GPR</td>
<td>General-purpose register</td>
</tr>
<tr>
<td>IBAT</td>
<td>Instruction BAT</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IU</td>
<td>Integer unit</td>
</tr>
<tr>
<td>LR</td>
<td>Link register</td>
</tr>
<tr>
<td>MMU</td>
<td>Memory management unit</td>
</tr>
<tr>
<td>msb</td>
<td>Most significant bit</td>
</tr>
<tr>
<td>MSR</td>
<td>Machine state register</td>
</tr>
<tr>
<td>NaN</td>
<td>Not a number</td>
</tr>
<tr>
<td>No-Op</td>
<td>No operation</td>
</tr>
<tr>
<td>OEA</td>
<td>Operating environment architecture</td>
</tr>
<tr>
<td>PTE</td>
<td>Page table entry</td>
</tr>
<tr>
<td>PTEG</td>
<td>Page table entry group</td>
</tr>
<tr>
<td>PVR</td>
<td>Processor version register</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced instruction set computing</td>
</tr>
<tr>
<td>SDR1</td>
<td>Register that specifies the page table base address for virtual-to-physical address translation</td>
</tr>
<tr>
<td>SIMM</td>
<td>Signed immediate value</td>
</tr>
<tr>
<td>SLB</td>
<td>Segment lookaside buffer</td>
</tr>
</tbody>
</table>
Table 2 describes instruction field notation conventions used in this document.

Table 2. Instruction Field Conventions

<table>
<thead>
<tr>
<th>The Architecture Specification</th>
<th>Equivalent to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>BA, BB, BT</td>
<td>crBA, crBB, crBD (respectively)</td>
</tr>
<tr>
<td>BF, BFA</td>
<td>crFD, crFS (respectively)</td>
</tr>
<tr>
<td>D</td>
<td>d</td>
</tr>
<tr>
<td>DS</td>
<td>ds</td>
</tr>
<tr>
<td>FLM</td>
<td>FM</td>
</tr>
<tr>
<td>FXM</td>
<td>CRM</td>
</tr>
<tr>
<td>RA, RB, RT, RS</td>
<td>rA, rB, rD, rS (respectively)</td>
</tr>
<tr>
<td>SI</td>
<td>SIIMM</td>
</tr>
<tr>
<td>U</td>
<td>IMM</td>
</tr>
<tr>
<td>UI</td>
<td>UIIMM</td>
</tr>
<tr>
<td>l, r, h</td>
<td>0...0 (shaded)</td>
</tr>
</tbody>
</table>

Table 1. Acronyms and Abbreviated Terms (Continued)

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
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<tbody>
<tr>
<td>SPR</td>
<td>Special-purpose register</td>
</tr>
<tr>
<td>SPRGr</td>
<td>Registers available for general purposes</td>
</tr>
<tr>
<td>SR</td>
<td>Segment register</td>
</tr>
<tr>
<td>SRR0</td>
<td>Machine status save/restore register 0</td>
</tr>
<tr>
<td>SRR1</td>
<td>Machine status save/restore register 1</td>
</tr>
<tr>
<td>TB</td>
<td>Time base register</td>
</tr>
<tr>
<td>TLB</td>
<td>Translation lookaside buffer</td>
</tr>
<tr>
<td>UIMM</td>
<td>Unsigned immediate value</td>
</tr>
<tr>
<td>UIISA</td>
<td>User instruction set architecture</td>
</tr>
<tr>
<td>VEA</td>
<td>Virtual environment architecture</td>
</tr>
<tr>
<td>XER</td>
<td>Register used for indicating conditions such as carries and overflows for integer operations</td>
</tr>
</tbody>
</table>
Part 1 Register Summary

This section describes the register organization defined by the three levels of the PowerPC architecture—user instruction set architecture (UISA), virtual environment architecture (VEA), and operating environment architecture (OEA). The PowerPC architecture defines register-to-register operations for all computational instructions. Source data for these instructions are accessed from the on-chip registers or are provided as immediate values embedded in the opcode. The three-register instruction format allows specification of a target register distinct from the two source registers, thus preserving the original data for use by other instructions and reducing the number of instructions required for certain operations. Data is transferred between memory and registers with explicit load and store instructions only.

Figure 1 shows a graphic representation of the entire PowerPC register set. The number to the right of the register name indicates the number that is used in the syntax of the instruction operands to access the register (for example, the number used to access the XER is SPR1).

Many of the SPRs can be accessed only by supervisor-level instructions; any attempt to access these SPRs with user-level instructions results in a supervisor-level exception. Some SPRs are implementation-specific. In some cases, not all of a register’s bits are implemented in hardware. When a PowerPC microprocessor detects SPR encodings other than those defined in this document, it either takes a program exception (if bit 0 of the SPR encoding is set) or it treats the instruction as a no-op (if bit 0 of the SPR encoding is clear).

Note that the general purpose registers (GPRs), link register (LR), count register (CTR), machine state register (MSR), data address register (DAR), SDR1, save and restore registers 0 and 1 (SRR0 and SRR1), SPRG0–SPRG3, and data address breakpoint register (DABR) are 64 bits in length in 64-bit implementations and 32 bits in length in 32-bit implementations.
### Figure 1. PowerPC Programming Model—Registers

<table>
<thead>
<tr>
<th>USER MODEL</th>
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<tbody>
<tr>
<td>General-Purpose Registers</td>
<td>GPR0</td>
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<td></td>
<td>GPR1</td>
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<td></td>
<td>⋮</td>
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<tr>
<td></td>
<td>SPR31</td>
</tr>
<tr>
<td>Floating-Point Registers</td>
<td>FPR0</td>
</tr>
<tr>
<td></td>
<td>FPR1</td>
</tr>
<tr>
<td></td>
<td>⋮</td>
</tr>
<tr>
<td></td>
<td>FPR31</td>
</tr>
<tr>
<td>Condition Register</td>
<td>CR</td>
</tr>
<tr>
<td>Floating-Point Status and Control Register</td>
<td>FPSCR</td>
</tr>
<tr>
<td>XER Register</td>
<td>XER SPR 1</td>
</tr>
<tr>
<td>Link Register</td>
<td>LR SPR 8</td>
</tr>
<tr>
<td>Count Register</td>
<td>CTR SPR 9</td>
</tr>
<tr>
<td>Time Base Facility (Read-Only)</td>
<td>TBL SPR 268</td>
</tr>
<tr>
<td></td>
<td>TBR SPR 269</td>
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<table>
<thead>
<tr>
<th>SUPERVISOR MODEL</th>
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<tr>
<td>Configuration Registers</td>
<td>Machine State Register MSR</td>
</tr>
<tr>
<td></td>
<td>Processor Version Register PVR SPR 287</td>
</tr>
<tr>
<td>Memory Management Registers</td>
<td>Instruction BAT Registers</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IBAT0U SPR 528</td>
</tr>
<tr>
<td></td>
<td>IBAT0L SPR 529</td>
</tr>
<tr>
<td></td>
<td>IBAT1U SPR 530</td>
</tr>
<tr>
<td></td>
<td>IBAT1L SPR 531</td>
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<td>IBAT3U SPR 534</td>
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<tr>
<td></td>
<td>IBAT3L SPR 535</td>
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<tr>
<td>SDR1 Register</td>
<td>SDR1 SPR 25</td>
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<tr>
<td>Address Space Register</td>
<td>ASR SPR 280</td>
</tr>
<tr>
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<td>⋮</td>
</tr>
<tr>
<td></td>
<td>SR15</td>
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<table>
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<tr>
<th>USER MODEL</th>
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<tbody>
<tr>
<td>General-Purpose Registers</td>
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<td>GPR1</td>
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<tr>
<td></td>
<td>SPR31</td>
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<tr>
<td>Floating-Point Registers</td>
<td>FPR0</td>
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<td></td>
<td>FPR1</td>
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<td>⋮</td>
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<td></td>
<td>FPR31</td>
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<tr>
<td>Condition Register</td>
<td>CR</td>
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<tr>
<td>Floating-Point Status and Control Register</td>
<td>FPSCR</td>
</tr>
<tr>
<td>XER Register</td>
<td>XER SPR 1</td>
</tr>
<tr>
<td>Link Register</td>
<td>LR SPR 8</td>
</tr>
<tr>
<td>Count Register</td>
<td>CTR SPR 9</td>
</tr>
<tr>
<td>Time Base Facility (Read-Only)</td>
<td>TBL SPR 268</td>
</tr>
<tr>
<td></td>
<td>TBR SPR 269</td>
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<table>
<thead>
<tr>
<th>USER MODEL</th>
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<tbody>
<tr>
<td>General-Purpose Registers</td>
<td>GPR0</td>
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<td></td>
<td>SPR31</td>
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<tr>
<td>Floating-Point Registers</td>
<td>FPR0</td>
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<td>Condition Register</td>
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<tr>
<td>Floating-Point Status and Control Register</td>
<td>FPSCR</td>
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<tr>
<td>XER Register</td>
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<td>CTR SPR 9</td>
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<tr>
<td>Time Base Facility (Read-Only)</td>
<td>TBL SPR 268</td>
</tr>
<tr>
<td></td>
<td>TBR SPR 269</td>
</tr>
</tbody>
</table>

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1 These registers are in 32-bit implementations only.
2 These registers are in 64-bit implementations only.
3 These registers are optional in the PowerPC architecture.
Table 3 provides a quick method by which to reference the SPR and TBR numbers and bit fields for all 32-bit PowerPC registers. Note that reserved bits are shaded.

Table 3. Quick Reference Guide—32-Bit Registers

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<tr>
<td>0F</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. For all SPR numbers refer to Figure 1
2. Write-Only
3. Read-Only
Table 4 provides a quick method by which to reference the SPR and TBR numbers and bit fields for all 64-bit PowerPC registers. Note that reserved bits are shaded.

Table 4. Quick Reference Guide—64-Bit Registers

<table>
<thead>
<tr>
<th>SPR</th>
<th>MSR</th>
<th>Branch Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPR 8</td>
<td>CTRL</td>
<td></td>
</tr>
<tr>
<td>SPR 9</td>
<td>LRR</td>
<td></td>
</tr>
<tr>
<td>SPR 19</td>
<td>DAR</td>
<td></td>
</tr>
<tr>
<td>SPR 25</td>
<td>SRR0</td>
<td></td>
</tr>
<tr>
<td>SPR 27</td>
<td>SRR1</td>
<td></td>
</tr>
<tr>
<td>SPR 272</td>
<td>SPRUN</td>
<td></td>
</tr>
<tr>
<td>SPR 280</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPR 528</td>
<td>BEPI</td>
<td></td>
</tr>
<tr>
<td>SPR 529</td>
<td>BRPN</td>
<td></td>
</tr>
<tr>
<td>SPR 1019</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBR 268</td>
<td>TBU</td>
<td></td>
</tr>
<tr>
<td>TBR 269</td>
<td>TBU</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. For all SPR numbers refer to Figure 1
2. Read-only

For the MSR bits, refer to 1.8, “Machine State Register (MSR),” on page 16.

1.1 General-Purpose Registers (GPRs)

Integer data is manipulated in the processor’s 32 GPRs shown in Figure 2. These registers are 64-bit registers in 64-bit implementations and 32-bit registers in 32-bit implementations. The GPRs are accessed as source and destination registers in the instruction syntax.

Figure 2. General-Purpose Registers (GPRs)

1.2 Floating-Point Registers (FPRs)

The PowerPC architecture provides thirty-two 64-bit FPRs as shown in Figure 3. These registers are accessed as source and destination registers for floating-point instructions. Each FPR supports the double-precision floating-point format. Every instruction that interprets the contents of an FPR as a floating-point value uses the double-precision floating-point format for this interpretation.
All floating-point arithmetic instructions operate on data located in FPRs and, with the exception of compare instructions, place the result into an FPR. Information about the status of floating-point operations is placed into the FPSCR and in some cases, into the CR after the completion of instruction execution.

The floating-point arithmetic instructions produce intermediate results that may be regarded as infinitely precise. After normalization or denormalization, if the precision of the intermediate result cannot be represented in the destination format (single or double precision), it is rounded to the specified precision before being placed in the target FPR. The final result is then placed into the FPR in the double-precision format.

<table>
<thead>
<tr>
<th>FPR0</th>
<th>FPR1</th>
<th>...</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>63</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3. Floating-Point Registers (FPRs)

1.3 XER Register (XER)

The XER register (XER) is shown in Figure 4.

![Figure 4. XER Register](image)

Table 5 provides bit setting information for XER.

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SO</td>
<td>Summary overflow. The summary overflow bit (SO) is set whenever an instruction (except mt Spr) sets the overflow bit (OV). Once set, the SO bit remains set until it is cleared by an mt Spr instruction (specifying the XER) or an mCrX instruction. It is not altered by compare instructions, nor by other instructions (except mt Spr to the XER, and mCrX) that cannot overflow. Executing an mt Spr instruction to the XER, supplying the values zero for SO and one for OV, causes SO to be cleared and OV to be set.</td>
</tr>
<tr>
<td>1</td>
<td>OV</td>
<td>Overflow. The overflow bit (OV) is set to indicate that an overflow has occurred during execution of an instruction. Add, subtract from, and negate instructions having OE = 1 set the OV bit if the carry out of the msb is not equal to the carry out of the msb + 1, and clear it otherwise. Multiply low and divide instructions having OE = 1 set the OV bit if the result cannot be represented in 64 bits (mulld, divld, divldu) or in 32 bits (mullw, divw, divwu), and clear it otherwise. The OV bit is not altered by compare instructions that cannot overflow (except mt Spr to the XER, and mCrX).</td>
</tr>
</tbody>
</table>
1.4 Floating-Point Status and Control Register (FPSCR)

Figure 5 shows the format of the floating-point status and control register (FPSCR).

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–23</td>
<td>CA</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Add carrying, subtract from carrying, add extended, and subtract from extended instructions set CA if there is a carry out of the msb, and clear it otherwise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Shift right instructions set CA if any 1 bits have been shifted out of a negative operand, and clear it otherwise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The CA bit is not altered by compare instructions, nor by other instructions that cannot carry (except shift right algebraic, mtspr to the XER, and mcrxr).</td>
</tr>
<tr>
<td>25–31</td>
<td>Reserved</td>
<td>This field specifies the number of bytes to be transferred by a Load String Word Indexed (lswx) or Store String Word Indexed (stswx) instruction.</td>
</tr>
</tbody>
</table>

Table 5. XER Bit Definitions (Continued)

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VXIDI</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>1</td>
<td>VXISI</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>2</td>
<td>VXSAIN</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>3</td>
<td>VXZOZ</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>4</td>
<td>VXSOFT</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>5</td>
<td>VXZDZ</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>6</td>
<td>VXMI2</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>7</td>
<td>VXIM2</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>8</td>
<td>VXCV</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
<tr>
<td>9</td>
<td>VXCVI</td>
<td>Carry. The carry bit (CA) is set during execution of the following instructions:</td>
</tr>
</tbody>
</table>

The FPSCR contains bits to do the following:

- Record exceptions generated by floating-point operations
- Record the type of the result produced by a floating-point operation
- Control the rounding mode used by floating-point operations
- Enable or disable the reporting of exceptions (invoking the exception handler)

Bits 0–23 are status bits. Bits 24–31 are control bits. Status bits in the FPSCR are updated at the completion of the instruction execution.

Except for the floating-point enabled exception summary (FEX) and floating-point invalid operation exception summary (VX), the exception condition bits in the FPSCR (bits 0–12 and 21–23) are sticky. Once set, sticky bits remain set until they are cleared by an mcrls, mtsfls, mtfsln, or mtfsbl instruction.

FEX and VX are the logical ORs of other FPSCR bits. Therefore, these two bits are not listed among the FPSCR bits directly affected by the various instructions.
FPSCR bit settings are shown in Table 6.

### Table 6. FPSCR Bit Settings

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FX</td>
<td>Floating-point exception summary. Every floating-point instruction, except <code>mtfsi</code> and <code>mtfsf</code>, implicitly sets FPSCR[FX] if that instruction causes any of the floating-point exception bits in the FPSCR to transition from 0 to 1. The <code>mcfrs</code>, <code>mtfsi</code>, <code>mtfsf</code>, <code>mtfsb0</code>, and <code>mtfsb1</code> instructions can alter FPSCR[FX] explicitly. This is a sticky bit.</td>
</tr>
<tr>
<td>1</td>
<td>FEX</td>
<td>Floating-point enabled exception summary. This bit signals the occurrence of any of the enabled exception conditions. It is the logical OR of all the floating-point exception bits masked by their respective enable bits. The <code>mcfrs</code>, <code>mtfsi</code>, <code>mtfsf</code>, <code>mtfsb0</code>, and <code>mtfsb1</code> instructions cannot alter FPSCR[FEX] explicitly. This is not a sticky bit.</td>
</tr>
<tr>
<td>2</td>
<td>VX</td>
<td>Floating-point invalid operation exception summary. This bit signals the occurrence of any invalid operation exception. It is the logical OR of all of the invalid operation exceptions. The <code>mcfrs</code>, <code>mtfsi</code>, <code>mtfsf</code>, <code>mtfsb0</code>, and <code>mtfsb1</code> instructions cannot alter FPSCR[VX] explicitly. This is not a sticky bit.</td>
</tr>
<tr>
<td>3</td>
<td>OX</td>
<td>Floating-point overflow exception. This is a sticky bit.</td>
</tr>
<tr>
<td>4</td>
<td>UX</td>
<td>Floating-point underflow exception. This is a sticky bit.</td>
</tr>
<tr>
<td>5</td>
<td>ZX</td>
<td>Floating-point zero divide exception. This is a sticky bit.</td>
</tr>
</tbody>
</table>
| 6      | XX   | Floating-point inexact exception. This is a sticky bit. FPSCR[XX] is the sticky version of FPSCR[FI]. The following rules describe how FPSCR[XX] is set by a given instruction:  
  - If the instruction affects FPSCR[FI], the new value of FPSCR[XX] is obtained by logically ORing the old value of FPSCR[XX] with the new value of FPSCR[FI].  
  - If the instruction does not affect FPSCR[FI], the value of FPSCR[XX] is unchanged. |
| 7      | VXSNAN | Floating-point invalid operation exception for SNaN. This is a sticky bit. |
| 8      | VXSI  | Floating-point invalid operation exception for $-\infty$. This is a sticky bit. |
| 9      | VXIDI | Floating-point invalid operation exception for $\infty'\infty$. This is a sticky bit. |
| 10     | VXZDZ | Floating-point invalid operation exception for 0'0. This is a sticky bit. |
| 11     | VXMZ  | Floating-point invalid operation exception for $-\infty'0$. This is a sticky bit. |
| 12     | VXVC  | Floating-point invalid operation exception for invalid compare. This is a sticky bit. |
| 13     | FR    | Floating-point fraction rounded. The last arithmetic or rounding and conversion instruction that rounded the intermediate result incremented the fraction. This bit is not sticky. |
| 14     | FI    | Floating-point fraction inexact. The last arithmetic or rounding and conversion instruction either rounded the intermediate result (producing an inexact fraction) or caused a disabled overflow exception. This is not a sticky bit. For more information regarding the relationship between FPSCR[FI] and FPSCR[XX], see the description of the FPSCR[XX] bit. |
Table 7 illustrates the floating-point result flags used by PowerPC processors. The result flags correspond to FPSR bits 15–19.

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15–19</td>
<td>FPRF</td>
<td>Floating-point result flags. For arithmetic, rounding, and conversion instructions the field is based on the result placed into the target register, except that if any portion of the result is undefined, the value placed here is undefined.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 Floating-point result class descriptor (C). Arithmetic, rounding and conversion instructions may set this bit with the FPCC bits to indicate the class of the result; see Table 7.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16–19 Floating-point condition code (FPCC). Floating-point compare instructions always set one of the FPCC bits to one and the other three FPCC bits to zero. Arithmetic, rounding and conversion instructions may set the FPCC bits with the C bit to indicate the class of the result. Note that in this case the high-order three bits of the FPCC retain their relational significance indicating that the value is less than, greater than, or equal to zero.</td>
</tr>
</tbody>
</table>
|        |            | 16 Floating-point less than or negative (FL or <)  
|        |            | 17 Floating-point greater than or positive (FG or >)  
|        |            | 18 Floating-point equal or zero (FE or =)  
|        |            | 19 Floating-point unordered or NaN (FU or ?)  
|        |            | These are not sticky bits.                                                                                                                  |
| 20     | —          | Reserved                                                                                                                                                                                                  |
| 21     | VXSOFT     | Floating-point invalid operation exception for software request. This is a sticky bit. This bit can be altered only by the `mcrfs`, `mtfsi`, `mtfsi`, `mtfsb0`, or `mtfsb1` instructions.                             |
| 22     | VXSQRT     | Floating-point invalid operation exception for invalid square root. This is a sticky bit.                                                                                                                 |
| 23     | VXCVI      | Floating-point invalid operation exception for invalid integer convert. This is a sticky bit.                                                                                                          |
| 24     | VE         | Floating-point invalid operation exception enable. This is not a sticky bit.                                                                                                                             |
| 25     | OE         | IEEE floating-point overflow exception enable. This is not a sticky bit.                                                                                                                                |
| 26     | UE         | IEEE floating-point underflow exception enable. This is not a sticky bit.                                                                                                                                  |
| 27     | ZE         | IEEE floating-point zero divide exception enable. This is not a sticky bit.                                                                                                                               |
| 28     | XE         | Floating-point inexact exception enable. This is not a sticky bit.                                                                                                                                       |
| 29     | NI         | Floating-point non-IEEE mode. If this bit is set, results need not conform with IEEE standards and the other FPSR bits may have meanings other than those described here. If the bit is set and if all implementation-specific requirements are met and if an IEEE-conforming result of a floating-point operation would be a denormalized number, the result produced is zero (retaining the sign of the denormalized number). Any other effects associated with setting this bit are described in the user’s manual for the implementation. Effects of the setting of this bit is implementation-dependent. This is not a sticky bit. |
| 30–31  | RN         | Floating-point rounding control.  
|        |            | 00 Round to nearest  
|        |            | 01 Round toward zero  
|        |            | 10 Round toward +infinity  
|        |            | 11 Round toward −infinity  
|        |            | These are not sticky bits.                                                                                                                  |

Table 6. FPSCR Bit Settings (Continued)
1.5 Condition Register (CR)

The format of the condition register (CR) is shown in Figure 6.

<table>
<thead>
<tr>
<th>C</th>
<th>&lt;</th>
<th>&gt;</th>
<th>=</th>
<th>?</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 7. Floating-Point Result Flags in FPSCR

<table>
<thead>
<tr>
<th>Result Flags (Bits 15–19)</th>
<th>Result Value Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>10001</td>
<td>Quiet NaN</td>
</tr>
<tr>
<td>01001</td>
<td>−Infinity</td>
</tr>
<tr>
<td>01000</td>
<td>−Normalized number</td>
</tr>
<tr>
<td>11000</td>
<td>−Denormalized number</td>
</tr>
<tr>
<td>10010</td>
<td>−Zero</td>
</tr>
<tr>
<td>00010</td>
<td>+Zero</td>
</tr>
<tr>
<td>10100</td>
<td>+Denormalized number</td>
</tr>
<tr>
<td>00100</td>
<td>+Normalized number</td>
</tr>
<tr>
<td>00101</td>
<td>+Infinity</td>
</tr>
</tbody>
</table>

The CR fields can be set in one of the following ways:

- Specified fields of the CR can be set by a move instruction (mtcrf) to the CR from a GPR.
- A specified field of the CR can be moved to another CR field with the mcrf instruction.
- A specified field of the XER can be copied to the CR by the mcrxr instruction.
- A specified field of the FPSCR can be copied to the CR by the mcrfs instruction.
- Condition register logical instructions can be used to perform logical operations on specified bits in the condition register.
- CR0 can be the implicit result of an integer instruction.
- CR1 can be the implicit result of a floating-point instruction.
- A specified CR field can indicate the result of either an integer or floating-point compare instruction.

Note that branch instructions are provided to test individual CR bits.
The following tables, Table 8–Table 10, provide bit setting information for CR0, CR1, and the CRn fields, respectively.

### Table 8. Bit Settings for CR0 Field of CR

<table>
<thead>
<tr>
<th>CR0 Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Negative (LT)—This bit is set when the result is negative.</td>
</tr>
<tr>
<td>1</td>
<td>Positive (GT)—This bit is set when the result is positive (and not zero).</td>
</tr>
<tr>
<td>2</td>
<td>Zero (EQ)—This bit is set when the result is zero.</td>
</tr>
<tr>
<td>3</td>
<td>Summary overflow (SO)—This is a copy of the final state of XER(SO) at the completion of the instruction.</td>
</tr>
</tbody>
</table>

### Table 9. Bit Settings for CR1 Field of CR

<table>
<thead>
<tr>
<th>CR1 Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Floating-point exception (FX)—This is a copy of the final state of FPSCR[FX] at the completion of the instruction.</td>
</tr>
<tr>
<td>5</td>
<td>Floating-point enabled exception (FEX)—This is a copy of the final state of FPSCR[FEX] at the completion of the instruction.</td>
</tr>
<tr>
<td>6</td>
<td>Floating-point invalid exception (VX)—This is a copy of the final state of FPSCR[VX] at the completion of the instruction.</td>
</tr>
<tr>
<td>7</td>
<td>Floating-point overflow exception (OX)—This is a copy of the final state of FPSCR[OX] at the completion of the instruction.</td>
</tr>
</tbody>
</table>

*Note:* For more information on the FPSCR refer to Section 1.4, “Floating-Point Status and Control Register (FPSCR).”
1.6 Link Register (LR)

The link register (LR) is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. The LR supplies the branch target address for the Branch Conditional to Link Register (bclr) instruction, and can be used to hold the logical address of the instruction that follows a branch and link instruction. The format of LR is shown in Figure 7.

Table 10. CRn Field Bit Settings for Compare Instructions

<table>
<thead>
<tr>
<th>CRn Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Less than or floating point less than (LT, FL). For integer compare instructions: RA &lt; SIMM or RB (signed comparison) or RA &lt; UIMM or RB (unsigned comparison). For floating-point compare instructions: fRA &lt; fRB.</td>
</tr>
<tr>
<td>1</td>
<td>Greater than or floating point greater than (GT, FG). For integer compare instructions: RA &gt; SIMM or RB (signed comparison) or RA &gt; UIMM or RB (unsigned comparison). For floating-point compare instructions: fRA &gt; fRB.</td>
</tr>
<tr>
<td>2</td>
<td>Equal or floating point equal (EQ, FE). For integer compare instructions: RA = SIMM, UIMM, or RB. For floating-point compare instructions: fRA = fRB.</td>
</tr>
<tr>
<td>3</td>
<td>Summary overflow or floating point unordered (SO, FU). For integer compare instructions: This is a copy of the final state of XER[SO] at the completion of the instruction. For floating-point compare instructions: One or both of fRA and fRB is a Not a Number (NaN).</td>
</tr>
</tbody>
</table>

Notes:
1. Here, the bit indicates the bit number in any one of the four-bit subfields, CR0–CR7.
2. For a complete description of instruction syntax conventions, refer to Table 31.

Both conditional and unconditional branch instructions include the option of placing the effective address of the instruction following the branch instruction in the LR.
1.7 Count Register (CTR)

The count register (CTR) is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. The CTR can hold a loop count that can be decremented during execution of branch instructions that contain an appropriately coded BO field. If the value in CTR is 0 before being decremented, it is –1 afterward. The CTR can also provide the branch target address for the Branch Conditional to Count Register (bcctr) instruction. The CTR is shown in Figure 8.

![CTR Diagram](image)

**Figure 8. Count Register (CTR)**

Fetching instructions along the target path is also possible provided the count register is loaded sufficiently ahead of the branch instruction.

The count register can be accessed by the `mtspr` and `mfspr` instructions by specifying SPR9. In branch conditional instructions, the BO field specifies the conditions under which the branch is taken. The first four bits of the BO field specify how the branch is affected by or affects the CR and the CTR. The encoding for the BO field is shown in Table 11.

<table>
<thead>
<tr>
<th>BO</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0 and the condition is FALSE.</td>
</tr>
<tr>
<td>0001y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0 and the condition is FALSE.</td>
</tr>
<tr>
<td>001zy</td>
<td>Branch if the condition is FALSE.</td>
</tr>
<tr>
<td>0100y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0 and the condition is TRUE.</td>
</tr>
<tr>
<td>0101y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0 and the condition is TRUE.</td>
</tr>
<tr>
<td>011zy</td>
<td>Branch if the condition is TRUE.</td>
</tr>
<tr>
<td>1000y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0.</td>
</tr>
<tr>
<td>1011y</td>
<td>Decrement the CTR, then branch if the decremented CTR = 0.</td>
</tr>
<tr>
<td>11zz</td>
<td>Branch always.</td>
</tr>
</tbody>
</table>

The z indicates a bit that is ignored. The z bits should be cleared to zero, as they may be assigned a meaning in some future version of the PowerPC architecture. The y bit provides a hint about whether a conditional branch is likely to be taken and is used by some PowerPC implementations to improve performance. Other implementations may ignore the y bit.
1.8 Machine State Register (MSR)

The machine state register (MSR), is a 64-bit register on 64-bit implementations (see Figure 9) and a 32-bit register in 32-bit implementations (see Figure 10).

```
<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 Bit</td>
<td>32 Bit</td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>SF</td>
<td>Sixty-four bit mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 The 64-bit processor runs in 32-bit mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 The 64-bit processor runs in 64-bit mode. Note that this is the default setting.</td>
</tr>
<tr>
<td>1-32</td>
<td></td>
<td>Reserved. Full function.</td>
</tr>
<tr>
<td>33-41</td>
<td></td>
<td>Reserved. Partial function.</td>
</tr>
<tr>
<td>42-44</td>
<td></td>
<td>Reserved. Partial function.</td>
</tr>
<tr>
<td>45</td>
<td>POW</td>
<td>Power management enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Power management disabled (normal operation mode).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Power management enabled (reduced power mode). Note: Power management functions are implementation-dependent. If the function is not implemented, this bit is treated as reserved.</td>
</tr>
<tr>
<td>46</td>
<td></td>
<td>Reserved—Implementation-specific</td>
</tr>
<tr>
<td>47</td>
<td>ILE</td>
<td>Exception little-endian mode. When an exception occurs, this bit is copied into MSR[LE] to select the endian mode for the context established by the exception.</td>
</tr>
<tr>
<td>48</td>
<td>EE</td>
<td>External interrupt enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 While the bit is cleared the processor delays recognition of external interrupts and decremter exception conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 The processor is enabled to take an external interrupt or the decrementer exception.</td>
</tr>
</tbody>
</table>
```

Figure 9. Machine State Register (MSR)—64-bit Implementations

Figure 10. Machine State Register (MSR)—32-bit Implementations

Table 12 shows the bit definitions for the MSR. Full function reserved bits are saved in SRR1 when an exception occurs; partial function reserved bits are not saved.
Table 12. MSR Bit Settings (Continued)

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
<td>PR</td>
<td>Privilege level</td>
</tr>
<tr>
<td>49-50</td>
<td>FP</td>
<td>Floating-point available</td>
</tr>
<tr>
<td>51</td>
<td>ME</td>
<td>Machine check enable</td>
</tr>
<tr>
<td>52</td>
<td>FE0</td>
<td>Floating-point exception mode 0 (see Table 13).</td>
</tr>
<tr>
<td>53</td>
<td>SE</td>
<td>Single-step trace enable (Optional)</td>
</tr>
<tr>
<td>54</td>
<td>BE</td>
<td>Branch trace enable (Optional)</td>
</tr>
<tr>
<td>55</td>
<td>FE1</td>
<td>Floating-point exception mode 1 (see Table 13).</td>
</tr>
<tr>
<td>56</td>
<td>—</td>
<td>Reserved. Full function.</td>
</tr>
</tbody>
</table>
| 57     | IP         | Exception prefix. The setting of this bit specifies whether an exception vector offset is prepended with Fs or Os. In the following description, nnnnn is the offset of the exception. See Table 30.
| 58     | IR         | Instruction address translation                                             |
| 59     | DR         | Data address translation                                                    |
| 60-61  | —          | Reserved. Full function.                                                    |
| 62     | RI         | Recoverable exception (for system reset and machine check exceptions).      |
| 63     | LE         | Little-endian mode enable                                                   |

The floating-point exception mode bits (FE0–FE1) are interpreted as shown in Table 13. Note that these bits can be logically ORed, so that if either is set the processor operates in precise mode.

Table 13. Floating-Point Exception Mode Bits

<table>
<thead>
<tr>
<th>FE0</th>
<th>FE1</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Floating-point exceptions disabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Floating-point imprecise nonrecoverable</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Floating-point imprecise recoverable</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Floating-point precise mode</td>
</tr>
</tbody>
</table>

Table 14 indicates the initial state of the MSR.

Table 14. State of MSR at Power Up

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>64 Bit</th>
<th>32 Bit</th>
<th>Name</th>
<th>64-Bit Description</th>
<th>32-Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–44</td>
<td>—</td>
<td>0–12</td>
<td>—</td>
<td>Unspecified⁰</td>
<td>Unspecified¹</td>
</tr>
<tr>
<td>45</td>
<td>13</td>
<td>0</td>
<td>POW</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>46</td>
<td>14</td>
<td>—</td>
<td>Unspecified⁰</td>
<td>Unspecified¹</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>15</td>
<td>0</td>
<td>ILE</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>48</td>
<td>16</td>
<td>EE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>49</td>
<td>17</td>
<td>PR</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>18</td>
<td>FP</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>51</td>
<td>19</td>
<td>ME</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>52</td>
<td>20</td>
<td>FE0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>53</td>
<td>21</td>
<td>SE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>54</td>
<td>22</td>
<td>BE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>55</td>
<td>23</td>
<td>FE1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>56</td>
<td>24</td>
<td>—</td>
<td>Unspecified⁰</td>
<td>Unspecified¹</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>25</td>
<td>IP</td>
<td>1²</td>
<td>1²</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>26</td>
<td>IR</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>59</td>
<td>27</td>
<td>DR</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
1.9 Processor Version Register (PVR)

The processor version register (PVR) is a 32-bit, read-only register that contains a value identifying the specific version (model) and revision level of the PowerPC processor (see Figure 11). The contents of the PVR can be copied to a GPR by the \texttt{mfspr} instruction. Read access to the PVR is supervisor-level only; write access is not provided.

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Name</th>
<th>64-Bit Description</th>
<th>32-Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>60–61</td>
<td>28–29</td>
<td>—</td>
<td>Unspecified(^1)</td>
</tr>
<tr>
<td>62</td>
<td>RI</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>63</td>
<td>LE</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Notes:
1. Unspecified can be either 0 or 1
2. 1 is typical, but might be 0

The PVR consists of two 16-bit fields:

- **Version (bits 0–15)**—A 16-bit number that uniquely determines a particular processor version and version of the PowerPC architecture. This number can be used to determine the version of a processor; it may not distinguish between different product models if more than one model uses the same processor.

- **Revision (bits 16–31)**—A 16-bit number that distinguishes between various releases of a particular version (that is, an engineering change level). The value of the revision portion of the PVR is implementation-specific. The processor revision level is changed for each revision of the device.
1.10 BAT Registers

Figure 12 and Figure 13 show the format of the upper and lower BAT registers for 64-bit PowerPC processors.

Figure 12. Upper BAT Register—64-Bit Implementations

Figure 13. Lower BAT Register—64-Bit Implementations

Figure 14 and Figure 15 show the format of the upper and lower BAT registers for 32-bit PowerPC processors.

Figure 14. Format of Upper BAT Registers—32-Bit Implementations

Figure 15. Format of Lower BAT Registers—32-Bit Implementations
Table 15 describes the bits in the BAT registers.

**Table 15. BAT Registers—Field and Bit Descriptions**

<table>
<thead>
<tr>
<th>Upper/ Lower BAT</th>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper BAT Register</td>
<td>0–46</td>
<td>0–14</td>
<td>BEPI</td>
</tr>
<tr>
<td>0–46</td>
<td>15–18</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td>51–61</td>
<td>19–29</td>
<td>BL</td>
<td>Block length. BL is a mask that encodes the size of the block. Values for this field are listed in Table 16.</td>
</tr>
<tr>
<td>62</td>
<td>30</td>
<td>Vs</td>
<td>Supervisor mode valid bit. This bit interacts with MSR[PR] to determine if there is a match with the logical address.</td>
</tr>
<tr>
<td>63</td>
<td>31</td>
<td>Vp</td>
<td>User mode valid bit. This bit also interacts with MSR[PR] to determine if there is a match with the logical address.</td>
</tr>
<tr>
<td>Lower BAT Register</td>
<td>0–46</td>
<td>0–14</td>
<td>BRPN</td>
</tr>
<tr>
<td>47–56</td>
<td>15–24</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td>57–60</td>
<td>25–28</td>
<td>WIMG</td>
<td>Memory/cache access mode bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>W</td>
<td>Write-through</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I</td>
<td>Caching-inhibited</td>
</tr>
<tr>
<td></td>
<td></td>
<td>M</td>
<td>Memory coherence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>G</td>
<td>Guarded</td>
</tr>
<tr>
<td>61</td>
<td>29</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td>62–63</td>
<td>30–31</td>
<td>PP</td>
<td>Protection bits for block</td>
</tr>
</tbody>
</table>

Table 16 lists the BAT area lengths encoded in the BL field of the upper BAT registers.

**Table 16. BAT Area Lengths**

<table>
<thead>
<tr>
<th>BAT Area Length</th>
<th>BL Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>128 Kbytes</td>
<td>000 0000 0000</td>
</tr>
<tr>
<td>256 Kbytes</td>
<td>000 0000 0001</td>
</tr>
<tr>
<td>512 Kbytes</td>
<td>000 0000 0011</td>
</tr>
<tr>
<td>1 Mbyte</td>
<td>000 0000 0111</td>
</tr>
<tr>
<td>2 Mbytes</td>
<td>000 0000 1111</td>
</tr>
<tr>
<td>4 Mbytes</td>
<td>000 0001 1111</td>
</tr>
<tr>
<td>8 Mbytes</td>
<td>000 0011 1111</td>
</tr>
<tr>
<td>16 Mbytes</td>
<td>000 0111 1111</td>
</tr>
<tr>
<td>32 Mbytes</td>
<td>000 1111 1111</td>
</tr>
</tbody>
</table>
1.11 SDR1
The SDR1 is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. Refer to Section 2.3.3, “SDR1 Register Definitions,” for a complete description of SDR1.

1.12 Address Space Register (ASR)
The address space register (ASR) is a 64-bit SPR that holds 0–51 of the segment table’s physical address. The segment table is the segment descriptor mechanism for 64-bit implementations. For more detailed information about the ASR, refer to Section 2.2.1.1, “Address Space Register (ASR).”

1.13 Segment Registers (SRs)
Segment registers are used in page and direct-store segment address translations. Refer to Section 2.2, “Segment Descriptor Definitions,” for information on segment registers.

1.14 Data Address Register (DAR)
The DAR is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. The DAR is shown in Figure 16.

![Figure 16. Data Address Register (DAR)](image)
The effective address generated by a memory access instruction is placed in the DAR if the access causes an exception (for example, an alignment exception). If the exception occurs in a 64-bit implementation operating in 32-bit mode, the high-order 32 bits of the DAR are cleared.
### 1.15 SPRG0–SPRG3

SPRG0–SPRG3 are 64-bit or 32-bit registers, depending on the type of PowerPC microprocessor. They are provided for general operating system use, such as performing a fast state save or for supporting multiprocessor implementations. The formats of SPRG0 through SPRG3 are shown in Figure 17.

![Figure 17. SPRG0–SPRG3](image)

Table 17 provides a description of conventional uses of SPRG0–SPRG3.

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPRG0</td>
<td>Software may load a unique physical address in this register to identify an area of memory reserved for use by the first-level exception handler. This area must be unique for each processor in the system.</td>
</tr>
<tr>
<td>SPRG1</td>
<td>This register may be used as a scratch register by the first-level exception handler to save the content of a GPR. That GPR then can be loaded from SPRG0 and used as a base register to save other GPRs to memory.</td>
</tr>
<tr>
<td>SPRG2</td>
<td>This register may be used by the operating system as needed.</td>
</tr>
<tr>
<td>SPRG3</td>
<td>This register may be used by the operating system as needed.</td>
</tr>
</tbody>
</table>

### 1.16 DSISR

The 32-bit DSISR, shown in Figure 18, identifies the cause of DSI and alignment exceptions.

![Figure 18. DSISR](image)

### 1.17 Machine Status Save/Restore Register 0 (SRR0)

The SRR0 is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. SRR0 is used to save machine status on exceptions and restore machine
status when an \texttt{rfi} instruction is executed. It also holds the EA for the instruction that follows the System Call (\texttt{sc}) instruction. The format of SRR0 is shown in Figure 19. For 32-bit implementations, the format of SRR0 follows the low-order bits (32–63) of Figure 19.

![Figure 19. Machine Status Save/Restore Register 0 (SRR0)](image)

When an exception occurs, SRR0 is set to point to an instruction such that all prior instructions have completed execution and no subsequent instruction has begun execution. When \texttt{rfi} is executed, the contents of SRR0 are copied to the next instruction address (NIA)—the 64- or 32-bit address of the next instruction to be executed. The instruction addressed by SRR0 may not have completed execution, depending on the exception type. SRR0 addresses either the instruction causing the exception or the instruction that immediately follows. The instruction addressed can be determined from the exception type and status bits.

If the exception occurs in 32-bit mode of the 64-bit implementation, the high-order 32 bits of SRR0 are cleared and the high-order 32 bits of the NIA are cleared when returning to 32-bit mode.

Note that in some implementations, every instruction fetch, when MSR[IR] = 1, and every instruction execution requiring address translation when MSR[DR] = 1, may modify SRR0.

### 1.18 Machine Status Save/Restore Register 1 (SRR1)

The SRR0 is a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. SRR1 is used to save machine status on exceptions and to restore machine status when an \texttt{rfi} instruction is executed. The format of SRR1 is shown in Figure 20.

![Figure 20. Machine Status Save/Restore Register 1 (SRR1)](image)

On 64-bit implementations, when an exception occurs, bits 33–36 and 42–47 of SRR1 are loaded with exception-specific information and bits 0–32, 37–41, and 48–63 of MSR are placed into the corresponding bit positions of SRR1.
For 32-bit implementations, when an exception occurs, bits 1–4 and 10–15 of SRR1 are loaded with exception-specific information and bits 0, 5–9, and 16–31 of MSR are placed into the corresponding bit positions of SRR1.

Note that, in some implementations, every instruction fetch when MSR[IR] = 1, and every instruction execution requiring address translation when MSR[DR] = 1, may modify SRR1.

1.19 Time Base Facility (TB)

The time base (TB), shown in Figure 21, is a 64-bit structure that contains a 64-bit unsigned integer that is incremented periodically. Each increment adds 1 to the low-order bit (bit 63). The frequency at which the counter is incremented is implementation-dependent.

![Figure 21. Time Base (TB)](image)

The TB increments until its value becomes 0xFFFF_FFFF_FFFF_FFFF ($2^{64} - 1$). At the next increment its value becomes 0x0000_0000_0000_0000. Note that there is no explicit indication that this has occurred (that is, no exception is generated).

The period of the time base depends on the driving frequency. The TB is implemented such that the following requirements are satisfied:

1. Loading a GPR from the time base has no effect on the accuracy of the time base.
2. Storing a GPR to the time base replaces the value in the time base with the value in the GPR.

The PowerPC VEA does not specify a relationship between the frequency at which the time base is updated and other frequencies, such as the processor clock. The TB update frequency is not required to be constant; however, for the system software to maintain time of day and operate interval timers, one of two things is required:

- The system provides an implementation-dependent exception to software whenever the update frequency of the time base changes and a means to determine the current update frequency; or
- The system software controls the update frequency of the time base.

Note that if the operating system initializes the TB to some ‘reasonable’ value and the update frequency of the TB is constant, the TB can be used as a source of values that increase at a constant rate, such as for time stamps in trace entries.
Even if the update frequency is not constant, values read from the TB are monotonically increasing (except when the TB wraps from $2^{64} - 1$ to 0). If a trace entry is recorded each time the update frequency changes, the sequence of TB values can be post-processed to become actual time values.

For information on reading, writing, and computing time of day on the time base, refer to Chapter 2, “PowerPC Register Set,” *The Programming Environments Manual*.

### 1.20 Decrementer Register (DEC)

The DEC, shown in Figure 22, is a 32-bit decrementing counter that provides a mechanism for causing a decrementer exception after a programmable delay. The DEC frequency is based on the same implementation-dependent frequency that drives the time base.

![Figure 22. Decrementer Register (DEC)](DEC)

For information on writing and reading the DEC, refer to Chapter 2, “PowerPC Register Set,” *The Programming Environments Manual*.

### 1.21 Data Address Breakpoint Register (DABR)

The data address breakpoint facility is controlled by the DABR, a 64-bit register in 64-bit implementations and a 32-bit register in 32-bit implementations. The data address breakpoint facility is optional to the PowerPC architecture, as is the DABR. However, if the data address breakpoint facility is implemented, it is recommended, but not required, that it be implemented as described in this section.

The data address breakpoint facility provides a means to detect accesses to a designated double word. The address comparison is done on an effective address, and it applies to data accesses only. It does not apply to instruction fetches.

The DABR is shown in Figure 23.

![Figure 23. Data Address Breakpoint Register—64-Bit Implementations](DABR)
Table 18 describes the fields in the DABR.

### Table 18. DABR—Field Descriptions

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0–60</td>
<td>DAB</td>
<td>Data address breakpoint</td>
</tr>
<tr>
<td>61</td>
<td>BT</td>
<td>Breakpoint translation enable</td>
</tr>
<tr>
<td>62</td>
<td>DW</td>
<td>Data write enable</td>
</tr>
<tr>
<td>63</td>
<td>DR</td>
<td>Data read enable</td>
</tr>
</tbody>
</table>

A data address breakpoint match is detected for a load or store instruction if the three following conditions are met for any byte accessed:

- $EA_{0–60} = DABR[DAB]$
- $MSR[DR] = DABR[BT]$
- The instruction is a store and $DABR[DW] = 1$, or the instruction is a load and $DABR[DR] = 1$.

In 32-bit mode of a 64-bit implementation, the high-order 32 bits of the EA are treated as zero for the purpose of detecting a match.

### 1.22 External Access Register (EAR)

The EAR is an optional 32-bit SPR that controls access to the external control facility and identifies the target device for external control operations. The external control facility provides a means for user-level instructions to communicate with special external devices. The EAR is shown in Figure 24. Note that the EAR is an optional register.

![Figure 24. External Access Register (EAR)](image)

The high-order bits of the resource ID (RID) field that correspond to bits of the RID beyond the width of the RID supported by a particular implementation are treated as reserved bits.

The EAR register is provided to support the External Control In Word Indexed (eciwx) and External Control Out Word Indexed (ecowx) instructions. Access to the EAR is supervisor-level, thus the operating system can determine which tasks are allowed to issue external access instructions and when they are allowed to do so. The bit settings for the EAR are described in Table 19.
The data access of eciwx and ecowx is performed as though the memory access mode bits (WIMG) were 0101. For example, if the external control facility is used to support a graphics adapter, the ecowx instruction could be used to send the translated physical address of a buffer containing graphics data to the graphics device. The eciwx instruction could be used to load status information from the graphics adapter.

This register can also be accessed by using the mtspr and mfspr instructions.

### Part 2 Memory Control Model

Memory in the PowerPC OEA is divided into 256-Mbyte segments. This segmented memory model provides a way to map 4-Kbyte pages of effective addresses to 4-Kbyte pages in physical memory (page address translation), while providing the programming flexibility afforded by a large virtual address space (80 or 52 bits).

The page address translation uses segment descriptors, which provide virtual address and protection information, and page table entries (PTEs), which provide the physical address and page protection information. The segment descriptors are programmed by the operating system to provide the virtual ID for a segment. In addition, the operating system also creates the page tables in memory that provide the virtual to physical address mappings (in the form of PTEs) for the pages in memory.

Segments in the OEA are defined as one of the following two types:

- **Memory segment**—An effective address in these segments represents a virtual address that is used to define the physical address of the page.
- **Direct-store segment**—References made to direct-store segments do not use the virtual paging mechanism of the processor.

The T bit in the segment descriptor selects between memory segments and direct-store segments, as shown in Table 20.

---

**Table 19. External Access Register (EAR) Bit Settings**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>E</td>
<td>Enable bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If this bit is set, the eciwx and ecowx instructions can perform the specified external operation. If the bit is cleared, an eciwx or ecowx instruction causes a DSI exception.</td>
</tr>
<tr>
<td>1–25</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>26–31</td>
<td>RID</td>
<td>Resource ID</td>
</tr>
</tbody>
</table>
All accesses generated by the processor map to a segment descriptor. If MSR[IR] = 0 or MSR[DR] = 0 for an instruction or data access, respectively, then real addressing mode translation is performed. Otherwise, if T = 0 in the corresponding segment descriptor (and the address is not translated by the BAT mechanism), the access maps to memory space and page address translation is performed.

After a memory segment is selected, the processor creates the virtual address for the segment and searches for the PTE that dictates the physical page number to be used for the access. Note that I/O devices can be easily mapped into memory space and used as memory-mapped I/O.

### 2.1 Address Translation Overview

The following sections provide a brief overview of the page and direct-store segment address translation. For more information, refer to Chapter 7, “Memory Management,” in *The Programming Environments Manual*.

#### 2.1.1 Page Address Translation

The first step in page address translation for 64-bit implementations is the conversion of the 64-bit effective address of an access into the 80-bit virtual address. The virtual address is then used to locate the PTE in the page tables in memory. The physical page number is then extracted from the PTE and used in the formation of the physical address of the access.

The translation of an effective address to a physical address for 64-bit implementations is described briefly:

- Bits 0–35 of the effective address comprise the effective segment ID used to select a segment descriptor, from which the virtual segment ID (VSID) is extracted.
- Bits 36–51 of the effective address correspond to the page number within the segment; these are concatenated with the VSID from the segment descriptor to form the virtual page number (VPN). The VPN is used to search for the PTE in either an on-chip TLB or the page table. The PTE then provides the physical page number (RPN).
- Bits 52–63 of the effective address are the byte offset within the page; these are concatenated with the RPN field of a PTE to form the physical address used to access memory.

### Table 20. Segment Descriptor Types

<table>
<thead>
<tr>
<th>Segment Descriptor T Bit</th>
<th>Segment Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Memory segment</td>
</tr>
<tr>
<td>1</td>
<td>Direct-store segment</td>
</tr>
</tbody>
</table>

The translation of effective addresses to physical addresses for 32-bit implementations is similar to that for 64-bit implementations, except that 32-bit implementations index into an array of 16 segment registers instead of segment tables in memory to locate the segment descriptor, and the address ranges are obviously different. Thus, the address translation is as follows:

- Bits 0–3 of the effective address comprise the segment register number used to select a segment descriptor, from which the virtual segment ID (VSID) is extracted.
- Bits 4–19 of the effective address correspond to the page number within the segment; these are concatenated with the VSID from the segment descriptor to form the virtual page number (VPN). The VPN is used to search for the PTE in either an on-chip TLB or the page table. The PTE then provides the physical page number (RPN).
- Bits 20–31 of the effective address are the byte offset within the page; these are concatenated with the RPN field of a PTE to form the physical address used to access memory.

2.1.2 Direct-Store Segment Address Translation

As described for memory segments, all accesses generated by the processor (with translation enabled) that do not map to a BAT area, map to a segment descriptor. If T = 1 for the selected segment descriptor, the access maps to the direct-store interface, invoking a specific bus protocol for accessing some special-purpose I/O devices. Direct-store segments are provided for POWER compatibility. As the direct-store interface is present only for compatibility with existing I/O devices that used this interface and the direct-store interface protocol is not optimized for performance, its use is discouraged. Applications that require low-latency load/store access to external address space should use memory-mapped I/O, rather than the direct-store interface.

2.2 Segment Descriptor Definitions

The format of the segment descriptors is different for 64-bit and 32-bit implementations. Additionally, the fields in the segment descriptors are interpreted differently depending on the value of the T bit within the descriptor. When T = 1, the segment descriptor defines a direct-store segment.

2.2.1 STE Format—64-Bit Implementations

In 64-bit implementations, the segment descriptors reside as segment table entries (STE) in hashed segment tables in memory. These STEs are generated and placed in segment tables in memory by the operating system. Each STE is a 128-bit entity (two double words) that maps one effective segment ID to one virtual segment ID. Information in the STE controls the segment table search process and provides input to the memory protection
mechanism. Figure 25 shows the format of both double words that comprise a $T = 0$ segment descriptor (or STE) in a 64-bit implementation.

![Figure 25. STE Format—64-Bit Implementations](image)

Table 21 lists the bit definitions for each double word in an STE.

<table>
<thead>
<tr>
<th>Double Word</th>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0–35</td>
<td>ESID</td>
<td>Effective segment ID</td>
</tr>
<tr>
<td></td>
<td>36–55</td>
<td>---</td>
<td>Reserved</td>
</tr>
<tr>
<td>56</td>
<td>V</td>
<td>Entry valid ($V = 1$) or invalid ($V = 0$)</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>T</td>
<td>$T = 0$ selects this format</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Ks</td>
<td>Supervisor-state protection key</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Kp</td>
<td>User-state protection key</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>N</td>
<td>No-execute protection bit</td>
<td></td>
</tr>
<tr>
<td>61–63</td>
<td>---</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0–51</td>
<td>VSID</td>
<td>Virtual segment ID</td>
</tr>
<tr>
<td></td>
<td>52–63</td>
<td>---</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The $K_s$ and $K_p$ bits partially define the access protection for the pages within the segment. The virtual segment ID field is used as the high-order bits of the virtual page number (VPN).

The segment descriptors are programmed by the operating system and placed into segment tables in memory, although some processors may additionally have on-chip segment lookaside buffers (SLBs). These SLBs store copies of recently-used STEs that can be accessed quickly, providing increased overall performance.

**2.2.1.1 Address Space Register (ASR)**

The ASR contains the control information for the segment table structure in that it defines the highest order bits for the physical base address of the segment table. The format of the
ASR is shown in Figure 26. The ASR contains bits 0–51 of the 64-bit physical base address of the segment table. Bits 52–56 of the STEG address are derived from the hashing function, (and bits 57–63 are zero at the beginning of a segment table search operation to point to the beginning of an STEG). Therefore, the beginning of the segment table lies on a $2^{12}$ byte (4 Kbyte) boundary.

Note that unless all accesses to be performed by the processor can be translated by the BAT mechanism when address translation is enabled (MSR[DR] or MSR[IR] = 1), the ASR must point to a valid segment table. If the processor does not support 64 bits of physical address, software should write zeros to those unsupported bits in the ASR. Otherwise, a machine check exception can occur.

Additionally, values x0, 0x1000, and 0x2000 should not be used as segment table addresses as they correspond to areas of the exception vector table reserved for implementation-specific purposes.

![Figure 26. ASR Register Format—64-Bit Implementations Only](image)

### 2.2.2 Segment Descriptor Format—32-Bit Implementations

In 32-bit implementations, the segment descriptors are 32-bits long and reside in one of 16 segment registers. Figure 27 shows the format of a segment register used in page address translation ($T = 0$) in a 32-bit implementation.

![Figure 27. Segment Register Format for Page Address Translation—32-Bit Implementations](image)

Table 22 provides the corresponding bit definitions of the segment register in 32-bit implementations.
The Ks and Kp bits partially define the access protection for the pages within the segment. The virtual segment ID field is used as the high-order bits of the virtual page number (VPN).

The segment register instructions are summarized in Table 23. These instructions are privileged in that they are executable only while operating in supervisor mode.

### Table 22. Segment Register Bit Definition for Page Address Translation—32-Bit Implementations

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>T</td>
<td>T = 0 selects this format</td>
</tr>
<tr>
<td>1</td>
<td>Ks</td>
<td>Supervisor-state protection key</td>
</tr>
<tr>
<td>2</td>
<td>Kp</td>
<td>User-state protection key</td>
</tr>
<tr>
<td>3</td>
<td>N</td>
<td>No-execute protection bit</td>
</tr>
<tr>
<td>4–7</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td>8–31</td>
<td>VSID</td>
<td>Virtual segment ID</td>
</tr>
</tbody>
</table>

The segment register instructions are summarized in Table 23. These instructions are privileged in that they are executable only while operating in supervisor mode.

### Table 23. Segment Register Instructions—32-Bit Implementations Only

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mtstr SR,rS</td>
<td>Move to Segment Register SR[SR]=rS</td>
</tr>
<tr>
<td>mtstrin rS,B</td>
<td>Move to Segment Register Indirect SR[rB[0–3]]=rS</td>
</tr>
<tr>
<td>mfstr rD,SR</td>
<td>Move from Segment Register rD=SR[SR]</td>
</tr>
<tr>
<td>mfstrin rD,B</td>
<td>Move from Segment Register Indirect rD=SR[rB[0–3]]</td>
</tr>
</tbody>
</table>

### 2.2.3 Segment Descriptors for Direct-Store Segments

The format of many of the fields in the segment descriptors depends on the value of the T bit. Figure 28 shows the format of segment descriptors (residing as STEs in segment tables) that define direct-store segments for 64-bit implementations (T bit is set).
Table 24. Segment Descriptor Bit Definitions for Direct-Store Segments—64-Bit Implementations

<table>
<thead>
<tr>
<th>Double Word</th>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0–35</td>
<td>ESID</td>
<td>Effective segment ID</td>
</tr>
<tr>
<td>36–55</td>
<td>—</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>V</td>
<td>Entry valid</td>
<td>(V = 1) or invalid (V = 0)</td>
</tr>
<tr>
<td>57</td>
<td>T</td>
<td>T = 0 selects this format</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Ks</td>
<td>Supervisor state protection key</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Kp</td>
<td>User-state protection key</td>
<td></td>
</tr>
<tr>
<td>61–63</td>
<td>—</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0–63</td>
<td>—</td>
<td>Device specific data for I/O controller</td>
</tr>
</tbody>
</table>

In 32-bit implementations, the segment descriptors reside in one of 16 segment registers. Figure 29 shows the register format for the segment registers when the T bit is set for 32-bit implementations.

Figure 28. Segment Descriptor Format for Direct-Store Segments—64-Bit Implementations

Table 24 shows the bit definitions for the segment descriptors when the T bit is set for 64-bit implementations.

Figure 29. Segment Register Format for Direct-Store Segments—32-Bit Implementations
Table 25 shows the bit definitions for the segment registers when the T bit is set for 32-bit implementations.

Table 25. Segment Register Bit Definitions for Direct-Store Segments

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>T</td>
<td>T = 1 selects this format.</td>
</tr>
<tr>
<td>1</td>
<td>Ks</td>
<td>Supervisor-state protection key</td>
</tr>
<tr>
<td>2</td>
<td>Kp</td>
<td>User-state protection key</td>
</tr>
<tr>
<td>3–11</td>
<td>BUlD</td>
<td>Bus unit ID</td>
</tr>
<tr>
<td>12–31</td>
<td></td>
<td>Device specific data for I/O controller</td>
</tr>
</tbody>
</table>

2.3 Page Table Entry (PTE) Definitions

Page table entries (PTEs) are generated and placed in page tables in memory by the operating system. The PowerPC OEA defines similar PTE formats for both 64- and 32-bit implementations in that the same fields are defined. However, 64-bit implementations define PTEs that are 128 bits in length while 32-bit implementations define PTEs that are 64 bits in length. Additionally, care must be taken when programming for both 64 and 32-bit implementations, as the bit placements of some fields are different. Some of the fields are defined as follows:

- The virtual segment ID field corresponds to the high-order bits of the virtual page number (VPN), and, along with the H, V, and API fields, it is used to locate the PTE (used as match criteria in comparing the PTE with the segment information).
- The R and C bits maintain history information for the page.
- The WIMG bits define the memory/cache control mode for accesses to the page.
- The PP bits define the remaining access protection constraints for the page.

Conceptually, the page table in memory must be searched to translate the address of every reference.

2.3.1 PTE Format for 64-Bit Implementations

In 64-bit implementations, each PTE is a 128-bit entity (two double words) that maps a virtual page number (VPN) to a physical page number (RPN). Information in the PTE is used in the page table search process (to determine a page table hit) and provides input to
the memory protection mechanism. Figure 30 shows the format of the two double words that comprise a PTE for 64-bit implementations.

Table 26 lists the corresponding bit definitions for each double word in a PTE as defined above.

Table 26. PTE Bit Definitions—64-Bit Implementations

<table>
<thead>
<tr>
<th>Double Word</th>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0–51</td>
<td>VSID</td>
<td>Virtual segment ID—corresponds to the high-order bits of the virtual page number (VPN)</td>
</tr>
<tr>
<td></td>
<td>52–56</td>
<td>API</td>
<td>Abbreviated page index</td>
</tr>
<tr>
<td></td>
<td>57–61</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>H</td>
<td>Hash function identifier</td>
</tr>
<tr>
<td></td>
<td>63</td>
<td>V</td>
<td>Entry valid (V = 1) or invalid (V = 0)</td>
</tr>
<tr>
<td>1</td>
<td>0–51</td>
<td>RPN</td>
<td>Physical page number</td>
</tr>
<tr>
<td></td>
<td>52–54</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>R</td>
<td>Referenced bit</td>
</tr>
<tr>
<td></td>
<td>56</td>
<td>C</td>
<td>Changed bit</td>
</tr>
<tr>
<td></td>
<td>57–60</td>
<td>WIMG</td>
<td>Memory/cache access control bits</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>—</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>62–63</td>
<td>PP</td>
<td>Page protection bits</td>
</tr>
</tbody>
</table>

The PTE contains an abbreviated page index rather than the complete page index field because at least 11 of the low-order bits of the page index are used in the hash function to select a PTE group (PTEG) address (PTEG addresses define the location of a PTE). Therefore, these 11 lower-order bits are not repeated in the PTEs of that PTEG.
2.3.2 PTE Format for 32-Bit Implementations

Figure 31 shows the format of the two words that comprise a PTE for 32-bit implementations.

![Figure 31. Page Table Entry Format—32-Bit Implementations](image)

Table 27 lists the corresponding bit definitions for each word in a PTE as defined above.

<table>
<thead>
<tr>
<th>Word</th>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>V</td>
<td>Entry valid (V = 1) or invalid (V = 0)</td>
</tr>
<tr>
<td></td>
<td>1–24</td>
<td>VSID</td>
<td>Virtual segment ID</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>H</td>
<td>Hash function identifier</td>
</tr>
<tr>
<td></td>
<td>26–31</td>
<td>API</td>
<td>Abbreviated page index</td>
</tr>
<tr>
<td>1</td>
<td>0–19</td>
<td>RPN</td>
<td>Physical page number</td>
</tr>
<tr>
<td></td>
<td>20–22</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>R</td>
<td>Referenced bit</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>C</td>
<td>Changed bit</td>
</tr>
<tr>
<td></td>
<td>25–28</td>
<td>WIMG</td>
<td>Memory/cache control bits</td>
</tr>
<tr>
<td></td>
<td>29</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>30–31</td>
<td>PP</td>
<td>Page protection bits</td>
</tr>
</tbody>
</table>

In this case, the PTE contains an abbreviated page index rather than the complete page index field because at least ten of the low-order bits of the page index are used in the hash function to select a PTEG address (PTEG addresses define the location of a PTE). Therefore, these ten lower-order bits are not repeated in the PTEs of that PTEG.

2.3.3 SDR1 Register Definitions

The SDR1 register contains the control information for the page table structure in that it defines the highest order bits for the physical base address of the page table and it defines the size of the table. The format of the SDR1 register differs for 64-bit and 32-bit implementations, as shown below.
2.3.3.1 SDR1 Register Definition for 64-Bit Implementations

The format of the SDR1 register for a 64-bit implementation is shown in Figure 32 and the bit settings are described in Table 28.

A page table can be any size $2^n$ bytes where $18 \leq n \leq 46$. The HTABSIZE field in SDR1 contains an integer value that specifies how many bits from the output of the hashing function are used as the page table index. HTABSIZE is used to generate a mask of the form $0b00...011...1$ (a string of $(HTABSIZE – 28)$ 0 bits followed by a string of 1 bits). As the table size increases, more bits are used from the output of the hashing function to index into the table. The 1 bits in the mask determine how many additional bits (beyond the minimum of 11) from the hash are used in the index; the HTABORG field must have this same number of lower-order bits equal to 0.

2.3.3.2 SDR1 Register Definition for 32-Bit Implementations

The format of SDR1 for 32-bit implementations is similar to that of 64-bit implementations except that the register size is 32 bits and the HTABMASK field is programmed explicitly into SDR1. Additionally, the address ranges correspond to a 32-bit physical address and the range of page table sizes is smaller. Figure 33 shows the format of the SDR1 register for 32-bit implementations; the bit settings are described in Table 29.
The HTABORG field in SDR1 contains the high-order 16 bits of the 32-bit physical address of the page table. Therefore, the beginning of the page table lies on a $2^{16}$ byte (64 Kbyte) boundary at a minimum. As with 64-bit implementations, if the processor does not support 32 bits of physical address, software should write zeroes to those unsupported bits in the HTABORG field (as the implementation treats them as reserved). Otherwise, a machine check exception can occur.

A page table can be any size $2^n$ bytes where $16 \leq n \leq 25$. The HTABMASK field in SDR1 contains a mask value that determines how many bits from the output of the hashing function are used as the page table index. This mask must be of the form 0b00...011...1 (a string of 0 bits followed by a string of 1 bits). As the table size increases, more bits are used from the output of the hashing function to index into the table. The 1 bits in HTABMASK determine how many additional bits (beyond the minimum of 10) from the hash are used in the index; the HTABORG field must have the same number of lower-order bits equal to 0 as the HTABMASK field has lower-order bits equal to 1.
Part 3 Exception Vectors

Exceptions, and conditions that cause them, are listed in Table 30.

Table 30. Exceptions and Conditions

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Vector Offset (hex)</th>
<th>Causing Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>00000</td>
<td>—</td>
</tr>
<tr>
<td>System reset</td>
<td>00100</td>
<td>The causes of system reset exceptions are implementation-dependent. If the conditions that cause the exception also cause the processor state to be corrupted such that the contents of SRR0 and SRR1 are no longer valid or such that other processor resources are so corrupted that the processor cannot reliably resume execution, the copy of the RI bit copied from the MSR to SRR1 is cleared.</td>
</tr>
<tr>
<td>Machine check</td>
<td>00200</td>
<td>The causes for machine check exceptions are implementation-dependent, but typically these causes are related to conditions such as bus parity errors or attempting to access an invalid physical address. Typically, these exceptions are triggered by an input signal to the processor. Note that not all processors provide the same level of error checking. The machine check exception is disabled when MSR[ME] = 0. If a machine check exception condition exists and the ME bit is cleared, the processor goes into the checkstop state. If the conditions that cause the exception also cause the processor state to be corrupted such that the contents of SRR0 and SRR1 are no longer valid or such that other processor resources are so corrupted that the processor cannot reliably resume execution, the copy of the RI bit copied from the MSR to SRR1 is cleared.</td>
</tr>
<tr>
<td>DSI</td>
<td>00300</td>
<td>A DSI exception occurs when a data memory access cannot be performed. Such accesses can be generated by load/store instructions, certain memory control instructions, and certain cache control instructions. For more detailed information, refer to Chapter 6, “Exceptions,” in The Programming Environments Manual.</td>
</tr>
<tr>
<td>ISI</td>
<td>00400</td>
<td>An ISI exception occurs when an instruction fetch cannot be performed. For more detailed information, refer to Chapter 6, “Exceptions,” in The Programming Environments Manual.</td>
</tr>
<tr>
<td>External interrupt</td>
<td>00500</td>
<td>An external interrupt is generated only when an external exception is pending (typically signaled by a signal defined by the implementation) and the interrupt is enabled (MSR[EE] = 1).</td>
</tr>
<tr>
<td>Alignment</td>
<td>00600</td>
<td>An alignment exception may occur when the processor cannot perform a memory access because of alignment or endian reasons. Note that an implementation is allowed to perform the operation correctly and not cause an alignment exception. For more detailed information, refer to Chapter 6, “Exceptions,” in The Programming Environments Manual.</td>
</tr>
<tr>
<td>Program</td>
<td>00700</td>
<td>A program exception is caused conditions which correspond to bit settings in SRR1 and arise during execution of an instruction. For more detailed information, refer to Chapter 6, “ Exceptions,” in The Programming Environments Manual.</td>
</tr>
<tr>
<td>Floating-point unavailable</td>
<td>00800</td>
<td>A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and move instructions) when the floating-point available bit is cleared, MSR[FP] = 0.</td>
</tr>
</tbody>
</table>
Part 4 PowerPC Instruction Set

The following sections include an instruction field summary, a list of split-field notation and conventions, and the entire PowerPC instruction set, sorted by mnemonic and opcode.

4.1 Instruction Field Summary

Table 30 describes the instruction fields used in the various instruction formats.

<table>
<thead>
<tr>
<th>Table 30. Exceptions and Conditions (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Exception</strong></td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>Decrementer</td>
</tr>
<tr>
<td>Reserved</td>
</tr>
<tr>
<td>Reserved</td>
</tr>
<tr>
<td>System call</td>
</tr>
<tr>
<td>Trace</td>
</tr>
<tr>
<td>Floating-Point</td>
</tr>
<tr>
<td>Assist</td>
</tr>
</tbody>
</table>

Table 31. Instruction Syntax Conventions

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA (30)</td>
<td>Absolute address bit. 0 The immediate field represents an address relative to the current instruction address (CIA). The effective (logical) address of the branch is either the sum of the LI field sign-extended to 64 bits and the address of the branch instruction or the sum of the BD field sign-extended to 64 bits and the address of the branch instruction. 1 The immediate field represents an absolute address. The effective address (EA) of the branch is the LI field sign-extended to 64 bits or the BD field sign-extended to 64 bits. Note: The LI and BD fields are sign-extended to 32 bits in 32-bit implementations.</td>
</tr>
<tr>
<td>BD (16-29)</td>
<td>Immediate field specifying a 14-bit signed two's complement branch displacement that is concatenated on the right with 0b00 and sign-extended to 64 bits (32 bits in 32-bit implementations).</td>
</tr>
<tr>
<td>BI (11-15)</td>
<td>Field used to specify a bit in the CR to be used as the condition of a branch conditional instruction.</td>
</tr>
<tr>
<td>BO (6-10)</td>
<td>Field used to specify options for the branch conditional instructions.</td>
</tr>
<tr>
<td>Field</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>crbA (11–15)</td>
<td>Field used to specify a bit in the CR to be used as a source.</td>
</tr>
<tr>
<td>crbB (16–20)</td>
<td>Field used to specify a bit in the CR to be used as a source.</td>
</tr>
<tr>
<td>crbD (6–10)</td>
<td>Field used to specify a bit in the CR, or in the FPSCR, as the destination of the result of an instruction.</td>
</tr>
<tr>
<td>crfD (6–8)</td>
<td>Field used to specify one of the CR fields, or one of the FPSCR fields, as a destination.</td>
</tr>
<tr>
<td>crfS (11–13)</td>
<td>Field used to specify one of the CR fields, or one of the FPSCR fields, as a source.</td>
</tr>
<tr>
<td>CRM (12–19)</td>
<td>Field mask used to identify the CR fields that are to be updated by the mtcrf instruction.</td>
</tr>
<tr>
<td>d (16–31)</td>
<td>Immediate field specifying a 16-bit signed two's complement integer that is sign-extended to 64 bits (32 bits in 32-bit implementations).</td>
</tr>
<tr>
<td>ds (16–29)</td>
<td>Immediate field specifying a 14-bit signed two's complement integer which is concatenated on the right with 0b00 and sign-extended to 64 bits. This field is defined in 64-bit implementations only.</td>
</tr>
<tr>
<td>FM (7–14)</td>
<td>Field mask used to identify the FPSCR fields that are to be updated by the mtfsf instruction.</td>
</tr>
<tr>
<td>frA (11–15)</td>
<td>Field used to specify an FPR as a source.</td>
</tr>
<tr>
<td>frB (16–20)</td>
<td>Field used to specify an FPR as a source.</td>
</tr>
<tr>
<td>frC (21–25)</td>
<td>Field used to specify an FPR as a source.</td>
</tr>
<tr>
<td>frD (6–10)</td>
<td>Field used to specify an FPR as the destination.</td>
</tr>
<tr>
<td>frS (6–10)</td>
<td>Field used to specify an FPR as a source.</td>
</tr>
<tr>
<td>fWM (16–19)</td>
<td>Immediate field used as the data to be placed into a field in the FPSCR.</td>
</tr>
<tr>
<td>L (10)</td>
<td>Field used to specify whether an integer compare instruction is to compare 64-bit numbers or 32-bit numbers. This field is defined in 64-bit implementations only.</td>
</tr>
<tr>
<td>LI (6–29)</td>
<td>Immediate field specifying a 24-bit signed two's complement integer that is concatenated on the right with 0b00 and sign-extended to 64 bits (32 bits in 32-bit implementations).</td>
</tr>
<tr>
<td>LK (31)</td>
<td>Link bit.</td>
</tr>
<tr>
<td>MB (21–25) and ME (26–30)</td>
<td>Fields used in rotate instructions to specify a 64-bit mask (32 bits in 32-bit implementations) consisting of 1 bits from bit MB + 32 through bit ME + 32 inclusive, and 0 bits elsewhere.</td>
</tr>
<tr>
<td>NB (16–20)</td>
<td>Field used to specify the number of bytes to move in an immediate string load or store.</td>
</tr>
<tr>
<td>OE (21)</td>
<td>Used for extended arithmetic to enable setting OV and SO in the XER.</td>
</tr>
<tr>
<td>OPCODE (0–5)</td>
<td>Primary opcode field.</td>
</tr>
<tr>
<td>rA (11–15)</td>
<td>Field used to specify a GPR to be used as a source or destination.</td>
</tr>
<tr>
<td>rB (16–20)</td>
<td>Field used to specify a GPR to be used as a source.</td>
</tr>
</tbody>
</table>
Table 32. Split-Field Notation and Conventions

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mb (21–26)</td>
<td>Field used in rotate instructions to specify the first 1 bit of a 64-bit mask (32 bits in 32-bit implementations). This field is defined in 64-bit implementations only.</td>
</tr>
<tr>
<td>me (21–26)</td>
<td>Field used in rotate instructions to specify the last 1 bit of a 64-bit mask (32 bits in 32-bit implementations). This field is defined in 64-bit implementations only.</td>
</tr>
<tr>
<td>sh (16–20)</td>
<td>Fields used to specify a shift amount (64-bit implementations only).</td>
</tr>
<tr>
<td>sh (30)</td>
<td>Fields used to specify a shift amount (64-bit implementations only).</td>
</tr>
<tr>
<td>spr (11–20)</td>
<td>Field used to specify a special purpose register for the mtspr and mfspr instructions.</td>
</tr>
<tr>
<td>tbr (11–20)</td>
<td>Field used to specify either the time base lower (TBL) or time base upper (TBU).</td>
</tr>
</tbody>
</table>
4.2 PowerPC Instruction Set Listings

This section lists the PowerPC architecture’s instruction set. Instructions are sorted by mnemonic and opcode. Note that split fields, that represent the concatenation of sequences from left to right, are shown in lowercase.

Table 33 lists the instructions implemented in the PowerPC architecture in alphabetical order by mnemonic.

### Table 33. Complete Instruction List Sorted by Mnemonic

| Name | 0 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|------|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| add  | 31 | D | A | B | JE | 266 | Rc |
| addc | 31 | D | A | B | JE | 10  | Rc |
| adde | 31 | D | A | B | JE | 138 | Rc |
| addi | 14 | D | A |    |    | SIMM |    |
| addic| 12 | D | A |    |    | SIMM |    |
| addic| 13 | D | A |    |    | SIMM |    |
| addmex| 31 | D | A | 0 0 0 0 0 0 | JE | 234 | Rc |
| adddx | 31 | D | A | 0 0 0 0 0 0 | JE | 202 | Rc |
| and  | 28 | S | A | B | 28 | Rc |
| andc | 29 | S | A | UIMM |    |    |
| andis| 28 | S | A | UIMM |    |    |
| bx   | 18 | LI | LI |    |    |    |
| bcsx | 16 | BO | BI | BD |    |    |
| bcctr| 19 | BO | BI | 0 0 0 0 0 0 | 528 | LK |
| bcctx| 19 | BO | BI | 0 0 0 0 0 0 | 16  | LK |
| cmp  | 31 | crfD | 0 | L | A | B | 0 | 0 |
| cmpl | 11 | crfD | 0 | L | A | SIMM |    |
| cmpli| 31 | crfD | 0 | L | A | B | 32 | 0 |
| cmpli| 10 | crfD | 0 | L | A | UIMM |    |
| cntlzdx | 31 | S | A | 0 0 0 0 0 0 | 58  | Rc |
| cntlzw| 31 | S | A | 0 0 0 0 0 0 | 26  | Rc |
| crand| 19 | orbD | orbA | orbB |    |    |    |

This document was created with FrameMaker 4.0.4
| Name   | 0  | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|--------|----|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| crandc | 19 | crbD | crbA | crbB | 129 | 0  |
| creqv  | 19 | crbD | crbA | crbB | 269 | 0  |
| crnand | 19 | crbD | crbA | crbB | 225 | 0  |
| crnor  | 19 | crbD | crbA | crbB | 33  | 0  |
| cror   | 19 | crbD | crbA | crbB | 449 | 0  |
| crorc  | 19 | crbD | crbA | crbB | 417 | 0  |
| crxor  | 19 | crbD | crbA | crbB | 193 | 0  |
| dcbf   | 31 | 0 0 0 0 | A | B | 86  | 0  |
| dcbi   | 31 | 0 0 0 0 | A | B | 470 | 0  |
| dcbs   | 31 | 0 0 0 0 | A | B | 54  | 0  |
| dcbsr  | 31 | 0 0 0 0 | A | B | 278 | 0  |
| dcbstmt| 31 | 0 0 0 0 | A | B | 246 | 0  |
| dcbz   | 31 | 0 0 0 0 | A | B | 1014| 0  |
| divedx | 31 | D | A | B | 489 | Rc |
| divedux| 31 | D | A | B | 457 | Rc |
| divex  | 31 | D | A | B | 491 | Rc |
| divexux| 31 | D | A | B | 459 | Rc |
| ecix   | 31 | D | A | B | 310 | 0  |
| eowx   | 31 | S | A | B | 438 | 0  |
| eieb   | 31 | 0 0 0 0 | 0 0 0 0 | 0 0 0 0 | 854 | 0  |
| eqvx   | 31 | S | A | B | 284 | Rc |
| extsbx | 31 | S | A | 0 0 0 0 | 954 | Rc |
| extshv | 31 | S | A | 0 0 0 0 | 922 | Rc |
| extswx | 31 | S | A | 0 0 0 0 | 986 | Rc |
| fabbx  | 63 | D | 0 0 0 0 | B | 264 | Rc |
| faddx  | 63 | D | A | B | 0 0 0 0 | 21 | Rc |
| faddux | 59 | D | A | B | 0 0 0 0 | 21 | Rc |
| fcfidx | 63 | D | 0 0 0 0 | B | 846 | Rc |
| fcmpo  | 63 | crfD | 0 0 | A | B | 32 | 0  |
| fcmpu  | 63 | crfD | 0 0 | A | B | 0 | 0  |
| fcfidx | 63 | D | 0 0 0 0 | B | 814 | Rc |
| fctlizx | 63 | D | 0 0 0 0 | B | 815 | Rc |
| fcilizx | 63 | D | 0 0 0 0 | B | 14  | Rc |

<p>| Name          | 0  | 6  | 7  | 8  | 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| fctiwz       | 63 | D  | 0  | 0  | 0  | 0  | 0  | 0  | B  | 15 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fdiv         | 63 | D  | A  | B  | 0  | 0  | 0  | 0  |    | 18 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fdivs        | 59 | D  | A  | B  | 0  | 0  | 0  | 0  |    | 18 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmadd        | 63 | D  | A  | B  | C  | 29 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmadds       | 59 | D  | A  | B  | C  | 29 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmx          | 63 | D  | 0  | 0  | 0  | 0  | 0  | B  | 72 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmsub        | 63 | D  | A  | B  | C  | 28 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmsubs       | 59 | D  | A  | B  | C  | 28 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmul         | 63 | D  | A  | 0  | 0  | 0  | 0  | C  | 25 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fmulx        | 63 | D  | A  | 0  | 0  | 0  | 0  | C  | 25 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnabs        | 63 | D  | 0  | 0  | 0  | 0  | B  | 136|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fneg         | 63 | D  | 0  | 0  | 0  | 0  | B  | 40 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnmadd       | 63 | D  | A  | B  | C  | 31 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnmadds      | 59 | D  | A  | B  | C  | 31 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnmsub       | 63 | D  | A  | B  | C  | 30 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnmsubs      | 59 | D  | A  | B  | C  | 30 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnres        | 59 | D  | 0  | 0  | 0  | 0  | B  | 0  | 0  | 0  | 0  | 24 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnresx       | 59 | D  | 0  | 0  | 0  | 0  | B  | 12 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fnresxs      | 59 | D  | 0  | 0  | 0  | 0  | B  | 26 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsel         | 63 | D  | A  | B  | C  | 23 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fselx        | 63 | D  | A  | B  | C  | 23 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsqrts       | 63 | D  | 0  | 0  | 0  | 0  | B  | 0  | 0  | 0  | 0  | 22 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsqrt        | 63 | D  | 0  | 0  | 0  | 0  | B  | 0  | 0  | 0  | 0  | 22 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsqrtsx      | 59 | D  | 0  | 0  | 0  | 0  | B  | 0  | 0  | 0  | 0  | 22 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsub         | 59 | D  | A  | 0  | 0  | 0  | 0  |    | 20 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| fsubx        | 59 | D  | A  | 0  | 0  | 0  | 0  |    | 20 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| icbi         | 31 | 0  | 0  | 0  | 0  | 0  | A  | B  | 982|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| isync        | 19 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 150|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| lbz          | 34 | D  | A  | d  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| lbzu         | 35 | D  | A  | d  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| lbzux        | 31 | D  | A  | B  | 119|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| lbzx         | 31 | D  | A  | B  | 87 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ld 4         | 58 | D  | A  | ds | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ldax 4       | 31 | D  | A  | B  | 84 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ldux 4       | 58 | D  | A  | ds | 1  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |</p>
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Table 34 lists the instructions defined in the PowerPC architecture in numeric order by opcode.

Table 34. Complete Instruction List Sorted by Opcode

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|------|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| xori | 26 | S | A | UIMM |
| xoris | 27 | S | A | UIMM |

1. Supervisor-level instruction
2. Supervisor- and user-level instruction
3. Load and store string or multiple instruction
4. 64-bit instruction
5. Optional instruction
6. 32-bit instruction only

Key: Reserved bits
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1 Supervisor-level instruction
2 Supervisor- and user-level instruction
3 Load and store string or multiple instruction
4 64-bit instruction
5 Optional instruction
6 32-bit instruction only
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