ENGR-2300
Electronic Instrumentation
Quiz 3
Fall 2018

Name 

SOLUTIONS

Section __

Question 1 (20 Points) 

Question 2 (20 Points) 

Question 3 (20 Points) 

Question 4 (20 Points) 

LMS Question is worth an additional 20pts

Total (80 points) 

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for answers that appear without justification. Read the entire quiz before answering any questions. Also it may be easier to answer parts of questions out of order.
Some Additional Background plus

555 Timer Block Diagram

Zener Diodes: From Wikipedia: A **Zener diode** is a diode which allows current to flow in the forward direction in the same manner as an ideal diode, but also permits it to flow in the reverse direction when the voltage is above a certain value known as the breakdown voltage, "zener knee voltage", "zener voltage", "avalanche point", or "peak inverse voltage". The device was named after Clarence Zener, who discovered this electrical property. Many diodes described as "zener" diodes rely instead on avalanche breakdown as the mechanism. Both types are used. Common applications include providing a reference voltage for voltage regulators, or to protect other semiconductor devices from momentary voltage pulses.

<table>
<thead>
<tr>
<th>Type Number</th>
<th>Nominal Zener Voltage $V_z$ (Volts)</th>
<th>Test Current $I_z$ (mA)</th>
<th>Maximum Zener Impedance $Z_{zm}$ (Ω)</th>
<th>Maximum Regulator Current $I_{z} (mA)$</th>
<th>Maximum Reverse Leakage Current $I_{z} (μA)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N746A</td>
<td>3.3</td>
<td>20</td>
<td>28</td>
<td>110</td>
<td>10</td>
</tr>
<tr>
<td>1N747A</td>
<td>3.6</td>
<td>20</td>
<td>24</td>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>1N748A</td>
<td>3.9</td>
<td>20</td>
<td>23</td>
<td>95</td>
<td>10</td>
</tr>
<tr>
<td>1N749A</td>
<td>4.3</td>
<td>20</td>
<td>22</td>
<td>85</td>
<td>2</td>
</tr>
<tr>
<td>1N750A</td>
<td>4.7</td>
<td>20</td>
<td>19</td>
<td>75</td>
<td>2</td>
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<tr>
<td>1N751A</td>
<td>5.1</td>
<td>20</td>
<td>17</td>
<td>70</td>
<td>1</td>
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<tr>
<td>1N752A</td>
<td>5.6</td>
<td>20</td>
<td>11</td>
<td>65</td>
<td>1</td>
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<tr>
<td>1N753A</td>
<td>6.2</td>
<td>20</td>
<td>7</td>
<td>60</td>
<td>0.1</td>
</tr>
<tr>
<td>1N754A</td>
<td>6.8</td>
<td>20</td>
<td>5</td>
<td>55</td>
<td>0.1</td>
</tr>
<tr>
<td>1N755A</td>
<td>7.5</td>
<td>20</td>
<td>6</td>
<td>50</td>
<td>0.1</td>
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<tr>
<td>1N756A</td>
<td>8.2</td>
<td>20</td>
<td>8</td>
<td>45</td>
<td>0.1</td>
</tr>
<tr>
<td>1N757A</td>
<td>9.1</td>
<td>20</td>
<td>10</td>
<td>40</td>
<td>0.1</td>
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<tr>
<td>1N758A</td>
<td>10</td>
<td>20</td>
<td>17</td>
<td>35</td>
<td>0.1</td>
</tr>
<tr>
<td>1N759A</td>
<td>12</td>
<td>20</td>
<td>30</td>
<td>30</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Question 1 (20 Points) Astable Multivibrator (An Iconic 555 Timer Application)

a. (4pt) The 555 timer circuit shown is to have a duty cycle of 80%. For a given \( C_1 \), what ratio of resistors \( R_1/R_2 \) will produce this duty cycle.

\[
\frac{T_1}{T} = \frac{0.693(R_1 + R_2)C_1}{0.693(R_1 + 2R_2)C_1} = \frac{R_1 + R_2}{R_1 + 2R_2} = 0.8
\]

\[
\frac{R_1}{R_2} = 3
\]

b. (4pt) Using this ratio of \( R_1/R_2 \) and \( C_1 = 10\mu F \), calculate the values for \( R_1 \) and \( R_2 \) needed to yield a frequency of 20Hz.

\[
f = \frac{1.44}{(R_1 + 2R_2)C_1} = 20 = \frac{1.44}{(3R_2 + 2R_2) \times 10^{-5}}
\]

\[
R_2 = 1.44k \text{ and } R_1 = 4.32k
\]

c. (2pt) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

Max = 6V, Min = 3 because of the internal divider of the 555

d. (4pt) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

Min = 0 since on pin 7 the transistor connects to zero
Max = 6V plus the voltage across R2 or 6 + (0.25)3 = 6.75V

On the next page, the freq must be 20 Hz so the period must be 1/20=50ms so the 3rd plot is out. The 2nd plot has the correct frequency. The first plot does not have an 80% duty cycle, so it has to be the middle plot. The individual curves must satisfy the voltages listed above so they are as labeled.
(6pts) Which of the sets of plots below shows the voltages on pins 2, 3, 6 and 7 for the case considered here? Label which plot is which in the correct figure.
In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for propagation of the signals through the gates. (The counter changes on the negative edge of DSTM1 and the flop flops change on the negative edge of U2A:Y.) DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.

a. The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the counter (U1A:QA, U1A:QB, & U1A:QC); the output from the combinational logic (U2C:Y=U3A:J, U4A:Y=U3A:K=U3B:J, & U2D:Y=U3B:K); and the output from the flip flops (U3A:Q & U4A:Q). (2pt per trace = 16pt)
b. (2 pts) A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 16 clock pulses? Clearly indicate the state of each signal.

<table>
<thead>
<tr>
<th>QD</th>
<th>QC</th>
<th>QB</th>
<th>QA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

15 \rightarrow 1111
16 \rightarrow 10000

4-bit counter output

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c. (2 pts) Consider the circuit below consisting of two NPN transistors Q1 and Q2. Vout1 is the collector terminal of Q1 and Vout2 is the collector terminal of Q2. For a given voltage V1, fill the table below indicating the status of Q1, Q2 (open/closed) and voltage level of Vout1 and Vout2 (High/low). Note: Transistor Q1 is open means Q1 is off and no current flows through it.

\[ V_{out} = V_1 \rightarrow \text{BUFFER!} \]

<table>
<thead>
<tr>
<th>V1</th>
<th>Q1 (open/closed)</th>
<th>Vout1 (High/Low)</th>
<th>Q2 (open/closed)</th>
<th>Vout2 (High/Low)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>Open</td>
<td>High</td>
<td>Closed</td>
<td>Low</td>
</tr>
<tr>
<td>3V</td>
<td>Closed</td>
<td>Low</td>
<td>Open</td>
<td>High</td>
</tr>
</tbody>
</table>
Question 3 (20 Points) Comparator and Schmitt Trigger

In this problem, we investigate the same properties of Schmitt Triggers we did in Experiment 6. Assume the output of the op-amps is capable of reaching the power supply voltages.

a. For the circuit shown the input signal, Vsignal is compared to Vref. For this part there isn’t any noise. Vnoise amplitude is 0V. The plot below has the Vsignal (without noise). On this plot, draw Vout. Label the plot as you would for an experiment report. (4pts)

b. Same circuit but now a digital type noise has corrupted the signal. Again plot Vout. Label as is done for report. (4pts)
c. It is desired to remove transitions of the output due to the noise. The output should look similar to part a, but the timing will be changed. In other words, there should only be one output pulse per cycle of the signal. Use the schematic below. This can be done using trial and error.

i. Ra is set at 1kΩ. Determine a value for Rb which will have the desired effect. There is a range of possible values. (2pts)

ii. For your value of Rb, determine the possible values for the voltage at the point labeled as Vc. (2pts)

iii. Plot Vout and Vc on the plot below for your values of Rb. (4pts)

\[ R_b = \text{value} \]
\[ V_c^{(\text{max})} = \text{value} \]
\[ V_c^{(\text{min})} = \text{value} \]

Plot Vc and Vout. Be sure to label significant voltages.
d. Now consider real op-amps but continue to use your values for $R_b$. The output voltage of the real op-amp won’t match the power supply voltage. If $V_{out}$ can only reach to 1V away from the power supply ($V_{out}$ max is 4V and $V_{out}$ min is -4V) what will now be your values for $V_c$ (use the same analysis as you used for part c.ii.) (2pts)

\[
R_b = 10k\Omega
\]

e. Will your design still work to eliminate the false transitions caused by the noise? Support your answer by giving your analysis. You don’t need to plot the results. (2pts)

\[
\text{Yes if } 2k \leq R_b \leq 13k\Omega \\
\text{No if } R_b > 13k\Omega
\]

Use plot if it helps answer part e.

$R_b = 5k\Omega$

Or words: The values of $V_c$ are sufficient different to avoid false transitions due to the noise.

P. M. Schoch and M. A. Hameed
Question 4 (20 Points) Diode Circuits

a. (4 Pts) We wish to regulate a 12V DC power supply using a Zener Diode from the table at the beginning of this quiz. Like all Zeners, this diode has three voltage ranges shown in its I-V curve below: the Off Region, The Forward Bias Region and the Reverse Bias Region.
Assuming ideal conditions for this diode, complete the following:
i. The voltage across the diode is $V_D \approx 0.7V$ in the Forward Region.
ii. The voltage across the diode is $V_D \approx 12V$ in the Reverse Region.
iii. The current through the diode is $I_D \approx 0\text{A}$ in the Off Region.
iv. What Zener part number would be used for this application?

b. For the circuit shown, the Zener is a 1N753A. Use the “Some Additional Background” information at the beginning of this exam. (3pts)
i. What is the Zener voltage for this diode?

\[ V_Z = 6.2V \]

ii. What is maximum Zener current recommended by the manufacturer? This is also referred to as the Maximum Regulator Current.

\[ I_{(\text{max})} = 60\text{mA} \]

iii. If operated at the maximum Zener current, how much power will be dissipated by the Zener.

\[ \text{Power} = V \cdot I = 372\text{mW} \]

\[ \text{or} \quad 0.372\text{W} \]
The circuit shown is the same circuit as part b and is still using the 1N753A Zener.

Complete the table for different values of $V_1$.

\[
V_1 = 4V \quad \text{Zener is off}
\]

\[
V_1 = 8V \quad V_{out} = 6.2V \quad I_{Zener} = 6.2/1.2 = 5.17mA
\]

\[
V_1 = 12V \quad V_{out} = 6.2 \quad I_{Zener} = (12-6.2)/0.1 = 58mA
\]

\[
I_Z = I_{Zener} = 58mA \quad I_T = 5.17mA
\]

\[
1.2\Omega \quad I_{Zener} = 5.17mA
\]

\[
V_{out} = V_{Zener} = 6.2V \quad R_{load} = 1k \Omega
\]

For the circuit shown, plot $V_{out}$ relative to ground on the plot below. $V_1$ is displayed on the plot. Use the $V_Z$ model with $V_{th}=0.7V$. Label as you would for a report. (3pts)
e. For the circuit shown, the input and the output voltages are shown in the plot below. Ignore the 1st 1/2 cycle. (3pts)

i. Determine the values of:
- \( V_{\text{ripple}} \approx 1.2V \) The peak to peak value of the ripple on the output.
- Ignore the 1st 1/2 cycle.
- \( f_{\text{ripple}} \approx 120 \text{Hz} \) The frequency of the ripple.

It is desired to reduce the magnitude of the ripple by a factor of approximately 2. List something that can be changed for this circuit to achieve this, and list how much it would need to be changed (and if it would need to be increased or decreased.)

1) Double \( C_1 \Rightarrow C_1 = 10 \mu F \)  
2) Double \( R_{\text{load}} \Rightarrow R_{\text{load}} = 4k\Omega \)

f. Do you expect to take the optional final? Your answer here is NON-BINDING. (1pt)

The optional final will:
- cover all topics in the class.
- generally be more difficult than the quizzes
- Not have an LMS portion,
- replace your lowest quiz grade, which includes the LMS portion,
- NOT replace your lowest quiz grade, IF the final grade is the lowest. i.e. you cannot hurt you overall grade by attempting the final.

Yes  No

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