Proposal Title: "SiGe BiCMOS Clockless Logic, Analysis, Synthesis and Systems"
Lead Organization: Rensselaer Polytechnic Institute, Troy, New York 12181
Contractor Business: OTHER EDUCATIONAL (University Education/Research)
Contractor Number: #452-03-101H
Collaborating Members: RPI, Theseus Research, FTL Systems
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II-A. Innovative Claims for the Proposed Research

Silicon Germanium Heterojunction Bipolar Transistors (SiGe HBTs) have revolutionized digital design, creating the possibility of attaining GaAs HBT device speeds in a Silicon processing technology. Recently IBM announced a 350 GHz SiGe HBT, setting a new world record for fastest device realized in Silicon. The SiGe HBT process can be made compatible with CMOS greatly extending the range of applications that can be addressed with either device alone. IBM's 8HP process combines 210 GHz HBT devices with a 0.13 micron CMOS process. The integrated circuit yield possible in SiGe HBT technology enables much larger and more ambitious designs to be undertaken at high speed, opening a new era for digital systems. However, at high frequencies there are many challenges for designers.   One of these is clock skew.

Clock skew is a result of many seemingly minor effects such as processing variations, temperature differences, and layout limitations. For example Chemical Mechanical Polishing (CMP) is a processing step used to planarize integrated circuit dielectric and metallization layers, but control over the thickness of the polished layers is often only maintainable in manufacturing to 10-15% tolerance. This converts directly into delay uncertainty. Temperature variations on modern chips can be substantial, and in the future 100-200 watt integrated circuits, these convert directly into mobility differences leading to timing skew. Modern fabrication lines also make frequent process improvements that affect circuit speeds affecting clock skew. Aging of the circuit can also lead to skew changes so that design for robust operation with built-in "slack" over lifetime service can be daunting, especially with clock signals approaching or exceeding 10 GHz. Generally a 100 ps clock requires skew much smaller than 10-15% to be effective. A clock period of 100 ps represents 10-20 ideal unloaded gate delays depending on which SiGe HBT process is being discussed. Wire delays at these frequencies encroach greatly on this number of gates/cycle especially if the number of gates is large. Hence uncertainties in wire delays encroach further. Certain functions in high-speed systems may demand the synchrony of a clock. Examples include regular analog to digital sampling. Other parts

of the system may need only to be fast, but not clocked. Examples include FIFO data storage or signal processing of data. Hence, clock skew considerations may only be required in certain portions of systems, while other portions of systems might be freed of this challenge, if only the completion of operations could be readily monitored. In these sections asynchronous or clockless operation is possible, and provided this can be attained without greatly increased device count, power dissipation, switching noise, broadband radiated EMI, or other undesirable effects can be avoided. **Asynchronous GHz rate SiGe HBT circuit design has been largely unexplored**, while CMOS asynchronous circuit design has begun to develop a methodology. This proposal is a joint project involving Rensselaer Polytechnic Institute, together with Theseus Research, and FTL Systems to explore whether some of the techniques (NCL) that these latter researchers have developed for CMOS may be adapted for SiGe HBT circuits. Additionally since SiGe HBT technology is present in a BiCMOS setting, an interface between any asynchronous HBT and CMOS NCL would need to be developed. In addition to the methodology and interface considerations, a CAD tool environment to facilitate these designs is required. Lastly a series of prototypes is required to demonstrate that the work is valid.

II-B. Planned Deliverables

This proposal is to develop a methodology for asynchronous or clockless design for SiGe HBT BiCMOS working closely with Theseus Research and FTL Systems, two companies that have extensive experience both in CMOS asynchronous design and in abstraction for design, and CAD tools. This proposal is primarily for innovative circuit design. Currently there is little or no work in the literature to address design of asynchronous circuits in the frequency range at 10 GHz and above for digital systems. Yet one can make an argument that nowhere is the development of a strategy for clockless design more needed than in this circuit domain. Hence, one of the main deliverables will be development of that strategy through styles of circuit design. This would be delivered in the form of the standard reportage required for DARPA contracts, quarterly, annual and final, together with the conventional medium of exchange of ideas through publications in the open literature. In addition, to development of these strategies, demonstration prototypes of varying complexity will be designed and simulated. In addition some fabrication of these prototype circuits will be attempted on an as-available basis. The sources of these opportunities will include any DARPA shared MPW space, donated space through MOSIS, and donated space from IBM through the so called Broad Band Center for Data Transport Science and Technology (BBCDT), an agreement between IBM and RPI and Cornell which includes some annual allotment of free SiGe BiCMOS processing over the next 5 years. These fabrications will include 5HP, and 7HP as well as some 8HP and beyond access. In exchange for these free fabrication resources, IBM expects to receive early awareness of any discoveries made using its processes.

The work proposed involves subcontracts with Theseus Research and FTL systems. Theseus Research is planning to serve as a consultant to RPI to help it develop SiGe HBT analogs to Null Convention Logic (NCL), which is its current technology offering in CMOS. The ideas of NCL are quite general, but the adaptation of these ideas to bipolar

design must take into account such issues as power, noise and yield which are quite different at the circuit level. At the very least the SiGe HBT methodology developed will have interfaces to NCL so that the two can communicate. Theseus Research will act as a consultant/advisor to students to build some basic CMOS NCL cells in IBM's BiCMOS kit so that co integration with the bipolar circuits will be possible. Theseus Research will also participate in the design of the prototype circuits, the prototype CAD framework and the design of the final large chip. Theseus Research expects to retain its existing intellectual property on CMOS.

FTL Systems will be a subcontractor to assist with CAD tools. FTL Systems has a long history of working with Theseus Research, and can expect to retain also its prior intellectual property agreements. FTL Systems will offer licensing for multiple, parallelized VHDL-AMS/VHDL-RF/MW simulator (GigaSim) and Merlin synthesis tools (modified for this effort) to Rensselaer and Theseus Research. These tools run on a variety of uni-processor and parallel machines such as RPI's SUN V880R SMP machines. These tools are for support of simulation activities related to development of system level demonstrations. Additional deliverables at each phase include a report identifying changes to the Merlin tools resulting from analysis of RPI's SiGe process and modifications to the Auriga and synthesis tool user guides associated with support of the modified FPGA target.

III-B. Description of the Results, Products, Transferable Technology and Expected Technology

Transfer Path

The purpose of the proposed research is to develop a circuit and system methodology for asynchronous design with SiGe HBT BiCMOS technology at frequencies > 10 GHz. This will include developing a variety of asynchronous building blocks and circuits, fabricating them and testing them to demonstrate their viability at GHz clock rates. These include One High Differential Logic, OHDL, and the Theseus Hysteretic Threshold Element (HTE). Additionally, a low cost methodology is sought to permit designers to explore, prototype, and possibly deploy asynchronous design. Three strategies are proposed for this, one is to build upon an existing XC 6200 SiGe FPGA emulator program funded by DARPA TEAM, by building up a superstructure of macro cells upon that architecture that can realize reconfigurable asynchronous circuits. The XC 6200 public domain tool sets will be interfaced to existing asynchronous CAD tools by RPI working in conjunction with FTL Systems a company that has worked with several defense contractors. It is felt this would provide a conduit for access to the technology.

Helpful URL's

 http://inp.cie.rpi.edu/research/mcdonald/frisc/