A 2-GHz Clocked AlGaAs/GaAs HBT Byte-Slice Datapath Chip

Steven R. Carlough, *Member, IEEE*, Robert A. Philhower, *Member, IEEE*, Cliff A. Maier, *Member, IEEE*, Samuel A. Steidl, *Student Member, IEEE*, Peter M. Campbell, *Member, IEEE*, Atul Garg, *Member, IEEE*, Kyung-Suc Nah, Matthew W. Ernest, *Student Member, IEEE*, James R. Loy, *Member, IEEE*, Thomas W. Krawczyk, Jr., *Student Member, IEEE*, Peter F. Curran, *Student Member, IEEE*, Russel P. Kraft, Hans J. Greub, *Member, IEEE*, and John F. McDonald, *Member, IEEE*

***Abstract*—A byte-slice datapath for exploring multi-chip RISC processor development in AlGaAs/GaAs heterojunction bipolar transistor (HBT) technology has been designed, fabricated and tested. The circuits are implemented using differential current-mode logic (CML) and emitter-coupled logic (ECL) with signal swings of 250 mV. Each datapath chip contains a single slice, including an 8-bit by 32-word single-port register file with a 230-ps read access time, and an 8-bit carry-select adder with a 140-ps select path and a 380-ps ripple-carry path. Each unpackaged die was tested using an at-speed boundary scan test scheme. The register file and adder carry chain are also implemented in a special test chip for accurate performance characterization of these critical circuits.**

***Index Terms*—Bipolar processor, current-mode logic, GaAs processor, heterojunction bipolar transistor, RISC processor.**

I. Introduction

As THE cost and technical obstacles of CMOS scaling continue to escalate, investigations into alternative technologies for processor design are being pursued. The goal of the effort reported in this paper is to explore high-clock-rate processor design using current-mode logic (CML) circuits with AlGaAs/GaAs heterojunction bipolar transistors (HBT's) [1]. In other efforts, processor design with alternative integrated circuit technologies such as GaAs MESFET's [2], Si Bipolar [3], GaAs HIIL [4], and numerous other technologies and circuit families [5], [6] have been investigated. One target application for this byte-slice datapath chip is a 32-bit integer RISC processor (FRISC/G) that was developed concurrently with the datapath design.

Ring oscillators, implemented with the AlGaAs/GaAs HBT devices in CML and emitter-coupled logic (ECL) gates, have stage delays as fast as 20 ps and generate very little switching noise. Due to low AlGaAs/GaAs HBT manufacturing yields this technology currently permits only tens of thousands of transistors per die if reasonable yields are to be obtained. The datapath chip and other components for a 32-bit processor application were developed with a budget of 10 000 HBT devices per chip. To circumvent limitations in device integration, the processor was partitioned into 23 chips designed for dense packaging on a high-density interconnect multi-chip module (MCM) [7]. This processor contains one instruction decoder chip, four copies of the datapath chip (each implementing a byte wide slice), two identical cache controller chips, and sixteen identical cache RAM chips (eight instruction and eight data memory chips).

A novel at-speed boundary scan test scheme was used during wafer probing to test the chips [8]. At 25 °C and with a supply voltage of −5.6 V, test measurements show correct operation of the datapath clocked at 2 GHz with a power dissipation of 13.4 W.

II. Technology and Circuit Design

The circuits discussed in this paper were fabricated in an AlGaAs/GaAs HBT technology with three levels of gold interconnect. The polyimide inter-layer dielectric nominally has an $\varepsilon_r = 2.9$ [1]. However, test results show the actual dielectric for the process is higher and anisotropic ($\varepsilon_{r\text{horizontal}} = 4.0, \varepsilon_{r\text{vertical}} = 3.2$) [9]. The anisotropy was modeled with 3-D capacitance extraction software [10] and the effects were incorporated into the simulation timing during the development of the datapath chip and other components.

A. Circuit Family

The standard cell library was implemented using three-level series gated differential CML and ECL logic, providing a circuit family with high functional complexity [11]. Any function of three variables, and some functions of five and six variables, can be implemented with a single current tree. Furthermore, logical inversions can be accomplished by swapping differential wires. Fig. 1 shows a latch with a two-bit multiplexer input.

Manuscript received October 1, 1999; revised February 10, 2000. This work was supported by the Defense Advanced Research Projects Agency under Contract DAAG-55-97-1-0316, Contract DAAH-04-93G-0477, Contract DAAL-03-92G-03-7, and Contract DAAL-03-90G-0187.

S. R. Carlough was with Rensselaer Polytechnic Institute, Troy, NY 12180 USA. He is now with IBM, Poughkeepsie, NY 12601 USA (e-mail: carlough@ieee.org).

R. A. Philhower is with IBM T. J. Watson Research Center, Yorktown Heights, NY 10598 USA.

C. A. Maier and A. Garg are with Advanced Micro Devices, Sunnyvale, CA 94088 USA.

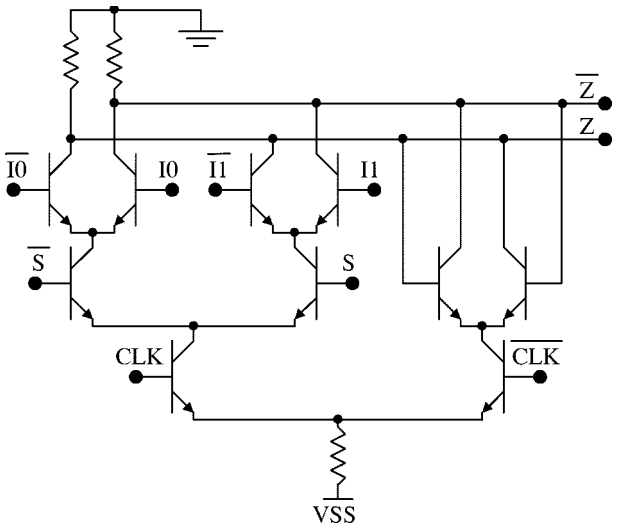
S. A. Steidl, M. W. Ernest, J. R. Loy, T. W. Krawczyk Jr., P. F. Curran, R. P. Kraft, and J. F. McDonald are with Rensselaer Polytechnic Institute, Troy, NY 12180 USA.

P. M. Campbell is with IBM, East Fishkill, NY 12533 USA.

K.-S. Nah is with Samsung Electronics Company Ltd., Kyungki-Do 440–600, Korea.

H. J. Greub is with Intel Corporation, Hillsboro, OR 97124 USA.

Publisher Item Identifier S 0018-9200(00)04461-9.



	High Voltage Level (V)	Low Voltage Level (V)
Level 1	**0**	**- 0.25**
Level 2 (-1 V_{BE})	**-1.4**	**-1.65**
Level 3 (-2 V_{BE})	**- 2.8**	**- 3.05**

Fig. 1. CML D-latch with 2-bit multiplexer.

TABLE I
POWER DISSIPATION OF THE STANDARD CELL LIBRARY AT −5.2 V

Power Levels	Logic Level 1	Logic Level 2	Logic Level 3
Low	4.2 mW	7.3 mW	7.3 mW
Medium	5.2 mW	8.8 mW	8.8 mW
High	7.8 mW	12.0 mW	12.0 mW
Ultra	10.4 mW	19.8 mW	19.8 mW
Super Buffer	NA	15.6 mW	15.6 mW
Clock Buffer	NA	62.4 mW	62.4 mW
Pad Receiver	15.6 mW	NA	NA
Pad Driver *	41.6 mW		

*Pad driver output voltage swing is 0 to −0.4 V

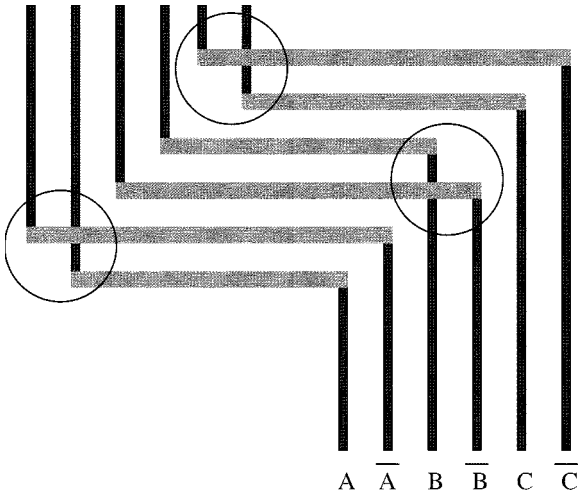


Fig. 2. Reducing data dependent switching between differential pairs.

The common-mode rejection ratio is typically greater than 5×10^5 for most of the logic circuits, though it can be as low as 23 for inputs at the lowest switching level due to the passive current sources. This common-mode noise rejection allows circuits to be designed with switching thresholds of 0.25 V at room temperature [12].

B. Voltage Levels

Resistive current sources were used in the logic trees to reduce the HBT device count and the supply voltage. The minimum supply voltage is determined by the forward active base to emitter voltage (1.4 V) of the AlGaAs/GaAs HBT [11]. A three-level CML current tree with an active source would require a −5.6 V minimum supply. To reduce the power, a minimum of 1 V was allocated for resistive current sources, requiring a minimum supply voltage of −5.2 V for correct operation. Higher supply voltages increase the current, providing additional speed at the cost of higher power dissipation.

The three input voltage levels to a current tree (Fig. 1) are offset by one V_{BE} to prevent device saturation, and the voltage swing is limited to 0.25 V. Level 2 and level 3 signals are generated with emitter follower output stages. Level shifting buffers and emitter follower inputs are used when matching levels to all of the inputs may not otherwise be possible. Drivers were designed with four power levels (shown in Table I) to permit the optimization of speed and power throughout the design.

Although passive current sources are sufficient for this prototyping effort, active sources are necessary in a production model of the chip to decrease sensitivity to processing variations. Unfortunately, active current sources require 12% more HBT devices, which would decrease die yields. Other disadvantages to passive current sources include lower common-mode noise rejection, and small current perturbations through the logic tree during switching.

The power dissipation of a logic gate is almost independent of the switching activity. Transitions on the lowest level input decrease the voltage across the tail resistor, which drops the current through a gate by 5% to 8%. The total dynamic power dissipation of a datapath chip clocked at 2 GHz is less than 200 mW, and constitutes a small decrease (1.5%) in the overall power dissipation.

C. Interconnect

Differential interconnections (differential pairs) were routed in adjacent routing tracks to minimize skew between the wire pairs, insuring proper circuit performance [11]–[13]. The routing resources necessary to route differential interconnect is partially offset by the high functional complexity of the logic gates, and the elimination of explicit inverters. The odd mode switching of the differential pair requires twice the voltage swing between the wires, increasing the effective capacitance by 30% [14]. Data dependent switching further limits performance if neighboring differential pairs transition

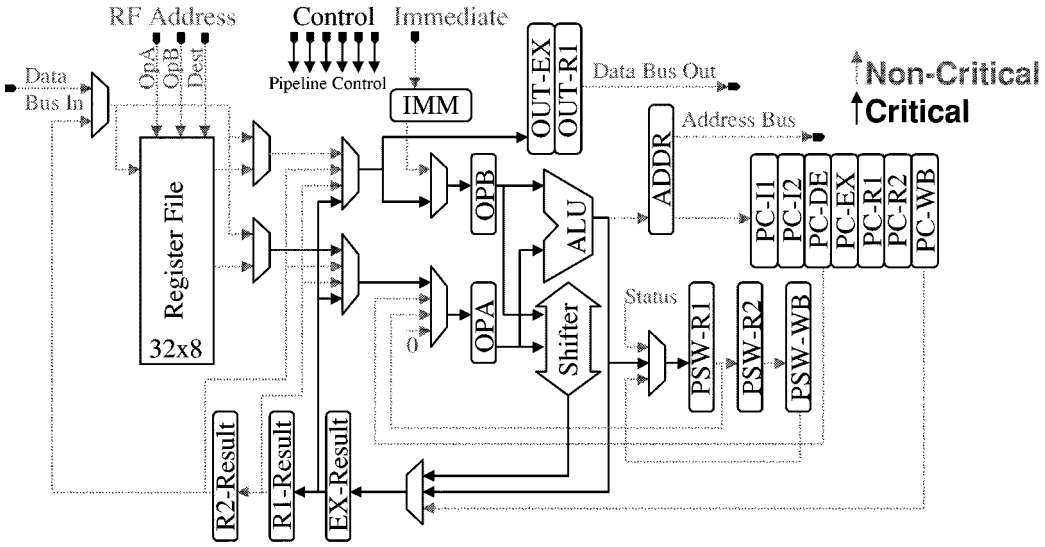


Fig. 3. Critical logic paths in data path chip.

simultaneously. This effect is less prominent in differential signals than in single-ended signals since one of a wire's two neighbors will always be switching in the opposite direction. Fig. 2 shows how signal crossovers are staggered in the routing channels to reduce this effect. Similar to bit line twisting in memory arrays, this routing technique balances the dynamic capacitance between neighboring differential pairs, reducing the worse-case switching time.

The resistance and capacitance of every net in the chip was extracted and modeled in SPICE with distributed *RC* segments to obtain the delays from the drivers to the receivers. A numerical analysis determined that the inductance affects the propagation delay through the longest wire in the chip (5 mm) by less than 3% at 2 GHz. Furthermore, the interconnect is overdamped (lowest damping factor $\zeta = 39$), so the distributed *RC* model provided accurate enough results for the design process [15]. The delays from these SPICE simulations were annotated into a netlist for use with a digital dynamic timing simulator.

III. Datapath Design

The datapath contains the hardware necessary to implement an instruction set similar to the MIPS I architecture [16]. The seven-stage processor pipeline begins with two instruction fetch stages (I1 and I2). Operands are accessed from the Register File (RF) during the decode stage (DE). Shift operations, arithmetic and logic unit (ALU) operations, branch decisions and destination address calculations are completed during the execute stage (EX). Data cache access begins in the first result stage (R1), and ALU results are written to the RF at the end of the second result stage (R2). Finally, store operations complete and load information arrives at the processor in the write-back stage (WB). A 3-bit field is defined in the jump and branch instructions to provide selective flushing of any combination of the three latency fields. This creates an annulling delayed branch function of all three of the latency regions, which improves the processor's average cycles per instruction (CPI) and code density.

The datapath chip provides the hardware necessary to support supervisor and user modes of operation for the processor. The upper half of the data and instruction memory space is only accessible to processes executing in supervisor mode, providing protected access to I/O devices, interrupt vectors, and control programs. The processor enters supervisor mode on interrupts, traps, or when a user program requests protected resources (software trap). The supervisor mode bit is stored in the processor status word (PSW) and may only be set through a transfer of control to a protected interrupt service routine (ISR). The datapath also contains circuitry for a restartable processor with 6 interrupt signals, an arithmetic trap, and a software trap. The instruction stream of a process is saved on the datapath chips in the program counter (PC) history registers (PC-I1 to PC-WB shown in Fig. 3) which are frozen on an interrupt placing the processor into protected mode. Re-entrant interrupts are handled by vectoring the processor (currently in protected mode) to a different set of ISR's that indicate normal PC history recovery resources are not available.

Fig. 4 shows a die micrograph of the 8.4×9.3 mm^2 datapath chip. The critical paths are dominated by interconnect delays for the following reasons: 1) the process only provides three interconnect layers; 2) devices and interconnect have large feature sizes; and 3) the gates have fast switching times, low output resistance, and low input capacitance. Fig. 3 shows a block diagram of the datapath outlining the critical paths. The input control signals are typically high fan-out nets and the capacitive impact of the wires significantly decreases the performance of these signals. To provide enough time for the control signals to reach all of the datapath chips in the DE stage, the pipeline stage had to be lengthened by 400 ps, skewing the EX stage with respect to the other pipeline stages. The R1 stage was then shortened by 400 ps realigning the stages before the register file write, which occurs in the R2 stage. The branch signal is determined in the EX stage based on the condition codes generated by a previous instruction (the earliest of which is now in the R1 stage). Skewing the EX stage creates a critical path for the branch signal when the decision is based on condi-

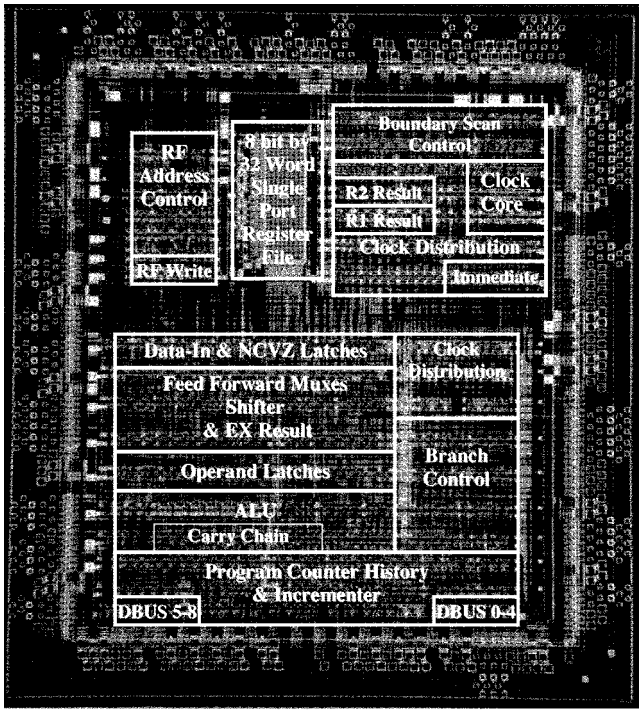
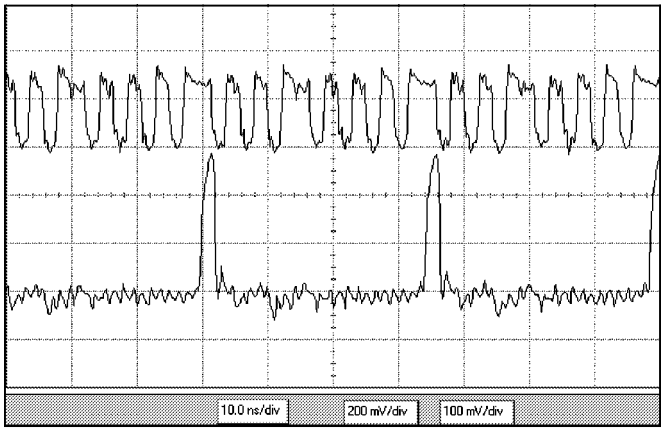
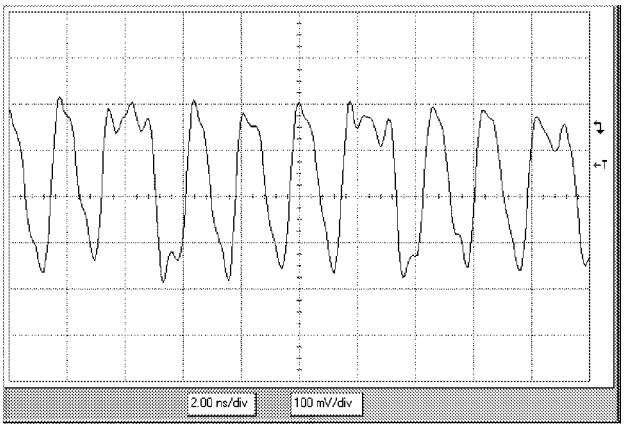


Fig. 4. Die micrograph of the datapath chip with overlay showing circuit placement.

tion codes set by the previous instruction. Fig. 5(a) shows the branch and carry-out signal from the datapath executing a repeating sequence of 32 addition operations, generating the pattern 0x555CCCCF. A critical path also exists on the ALU forwarding path from the EX stage. The data must move from the ALU output latches, through the operand multiplexer circuitry and into the operand latches in less than 80 ps. This result is also sent to the R1-Result pipeline latches, which is a considerable distance from the ALU. Buffers were placed near the EX forwarding path to isolate it from the interconnect capacitance of the long lines to the R1-Result latches. Fig. 5(b) shows the carry-out of the datapath from a sequence of 16 addition operations executing out of the EX forwarding path.



(a)



(b)

Fig. 5. (a) Carry-out and branch signals from datapath during 32 addition operations. Branch condition is ALU = 0. (b) Carry-out signal measured from a datapath chip during 16 addition operations. Pattern indicating correct operation is 0xD56A.

IV. Clock Generation and Distribution

A master clock is distributed to the instruction decoder, cache controllers, and datapath chips in the processor application. On each chip, the master clock is sent to a four-phase system clock generator. Fig. 6 shows the measured waveforms from the datapath's four-phase generator clocked at 2 GHz. A SYNC signal is used to keep the on-chip system clocks locked in phase 1 during system initialization. Accurate control of the four-phase generator is necessary when using the at-speed boundary scan testing scheme [8]. In test mode, the four-phase circuit can start in any selected phase, run for a specified number of clock phases and shut down.

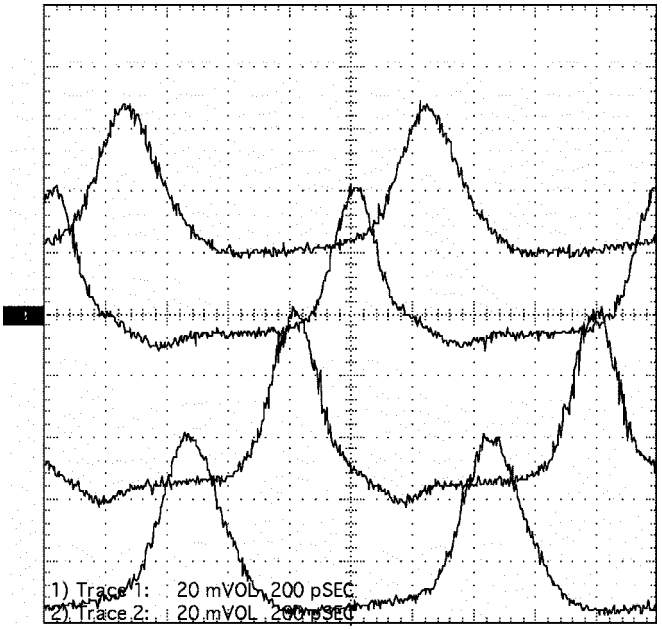


Fig. 6. Four-phase clock generator output.

V. Register File

Measurements of the 32-word by 8-bit register file (RF) slice (four slices are used for a 32-bit processor RF) show a read-access time of 230 ps and a static power dissipation of 1.9 W (7.4 mW per bit) with a −5.6 V supply. The RF consists of a 5-bit address decoder, a 256-bit Schottky clamped memory cell array,

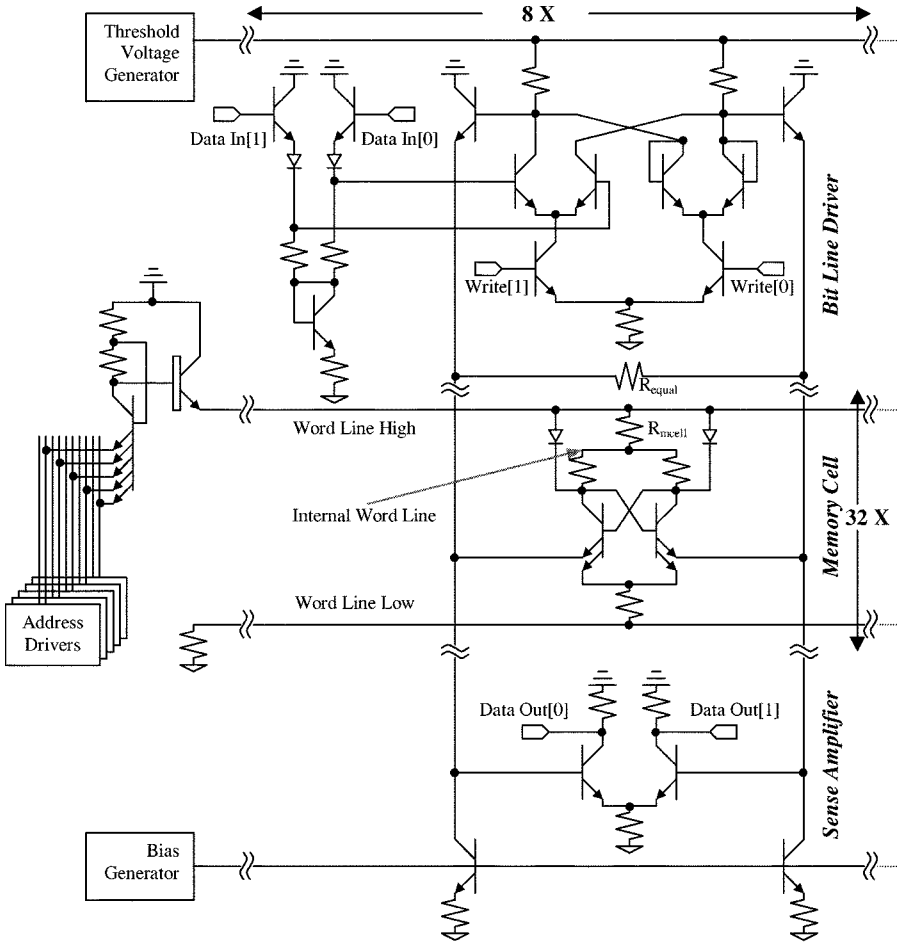


Fig. 7. Register file block diagram.

32 word-line drivers, 8 bit-line drivers, and 8 sense amplifiers as shown in Fig. 7 [17]. A single port register file design was used to minimize the required number of devices, and timing control is provided using the four-phase generator. Operand A is accessed during clock phase 3, operand B is accessed during phase 2, and write operations occur during phase 4 (address select) and phase 1 (write).

The Schottky clamped memory cell is composed of two dual-emitter HBT's, two Schottky diodes, and four resistors. The high word line must swing 850 mV to forward bias the Schottky diodes. A novel voltage-divider circuit at the top of the memory cell is used to reduce the internal word-line swing by 20 mV for the memory cells in the selected state. This decreases the bit-line swing, which reduces access time by 4%. For unselected memory cells, the current through R_{mcell} is small, providing sufficient voltage ($>$200 mV) between the base nodes to prevent data corruption from bit-line transients.

The address decoder selects one of the 32 word lines based on a 5-bit address input, and the corresponding word-line driver increases its high word line by 850 mV. During read operations, the bit-line drivers pass the threshold voltage generator output to the bit lines causing the appropriate dual-emitter HBT's of the selected memory cells to drive the corresponding bit lines high. During write operations, the bit-line driver forces data onto the bit lines, which overdrives the selected memory cells values, forcing them to the new states.

During consecutive read operations where the values of the data remains unchanged, the bit-line voltage rises higher than during read operations in which the data values change. This additional charge must be removed when the bit lines finally change value, resulting in a mismatch in speed between this "slow read" and a "fast read" operation. A bit-line equalization resistor (R_{equal}) is placed between the lines to reduce the amount of overcharging that occurs between the pairs and to decrease the switching time of a "slow read" operation. A clamping circuit could have been used to limit the swing of the bit lines; however, this would have increased bit line capacitance as well as device count.

Fig. 8(b) shows a die micrograph of a test chip that includes a carry-chain oscillator and a register file test structure to characterize the performance of these critical structures. The RF test structure, shown in Fig. 8(a), uses linear feedback shift registers (LFSR's) to provide address and data test patterns. A write-pulse generator creates the write signal to the RF core during write operations. The data generated during previous write operations and the accessed data of the RF is latched during the falling edge of the clock. The write time and read access can then be measured as half the clock period at the point of failure. Fig. 9(a) shows the write time and read access time for the register file at various supply voltages. Fig. 9(b) shows the measured voltage on bit 7 of the RF during a series of read operations to a sequence of memory locations that were previously written to with the data LFSR.

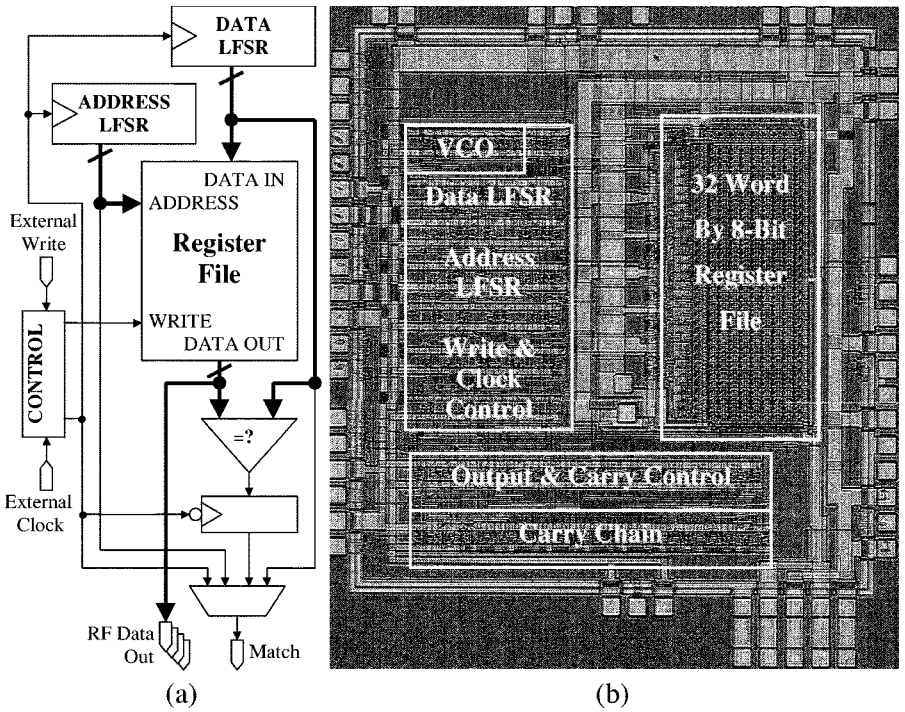


Fig. 8. (a) Block diagram of the register file test circuit. (b) Micrograph of test chip with overlay showing circuit placement.

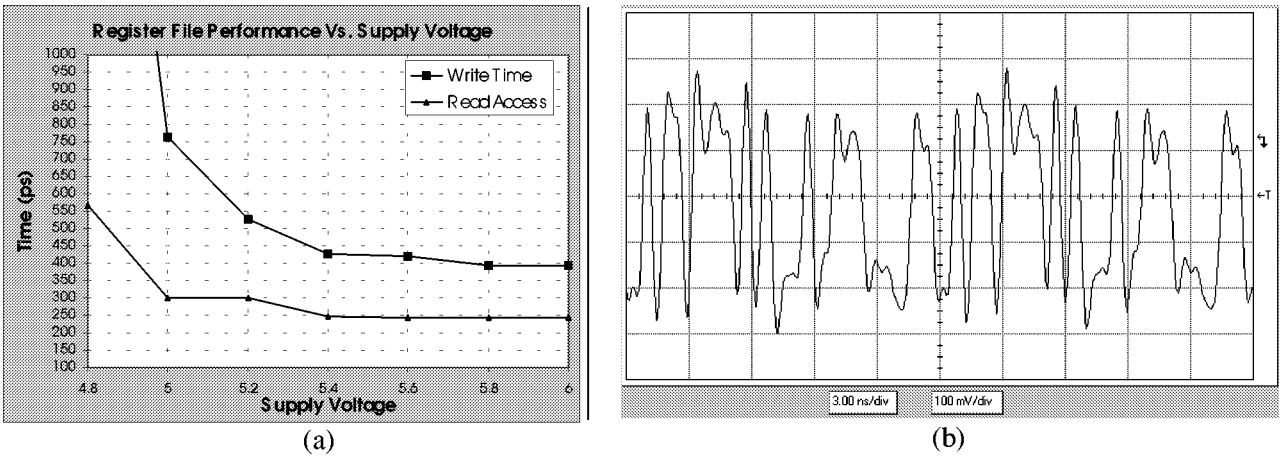


Fig. 9. (a) Register file performance versus supply voltage. (b) Output waveform of RF data bit-7 during sequential read operations to various memory locations.

VI. Carry Chain for a 32-Bit RISC Processor

For a 32-bit RISC application, each datapath chip would compute 8 of the 32 bits in the processor's ALU. A disadvantage of this bit-slice design (forced by insufficient yields for a single chip implementation) is that the carry bit must propagate across four datapath slices, making three crossings between the chips in a single cycle. Therefore, the maximum instruction rate possible in this byte-slice application is limited to 1 ns. Adder test circuits for designs targeting HBT processes with much higher yields demonstrate 32-bit addition can occur several times faster if the device integration is sufficient for a complete execution pipeline to be implemented in a single chip.

A high-density interconnect MCM provides wire layers for inter-chip communications in the 23-chip processor [7]. The MCM interconnect has a characteristic impedance of 50 Ω, and terminator pads on the chips provide a matched impedance termination at the far end of the MCM traces.

A carry-select adder was used to offset the delay caused by chip crossings on this critical path. For a 32-bit processor to meet a target 1 ns cycle time, the adder must complete its operation in 900 ps since 20 ps were allocated to cross-chip clock skew, and 80 ps to the forwarding path previously discussed. Fig. 10 shows a breakdown of the carry propagation timing. The three MCM delays are estimated at 50 ps each leaving only 750 ps for on-chip delays. The least significant slice must compute carry-out through the ripple-carry logic and pass the result to the next significant slice. At −5.6 V, SPICE simulations show this delay is 367 ps, leaving only 383 ps for the remaining three chips. From the carry-in pad to the carry-out pad, simulations show the delay is 138 ps since the carry bit only selects the appropriate value, resulting in a total delay of 931 ps. However, the

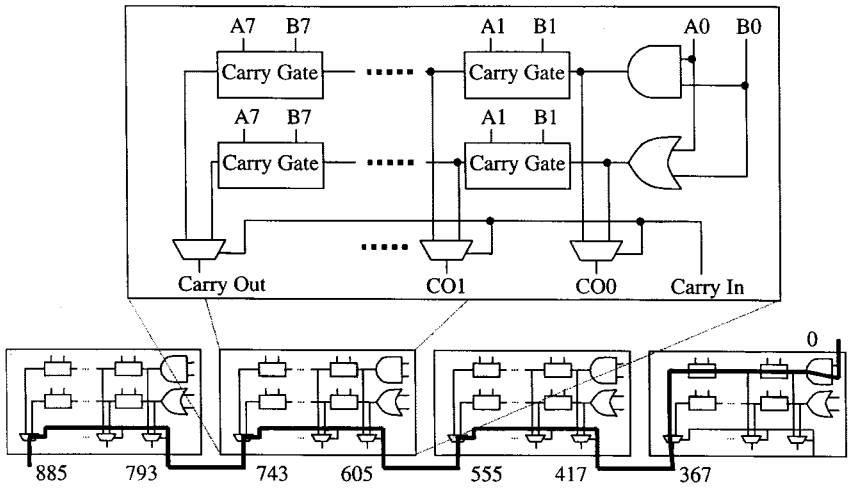


Fig. 10. Carry chain with projected propagation timing (in ps) from oscillator test circuits measured at −5.6 V.

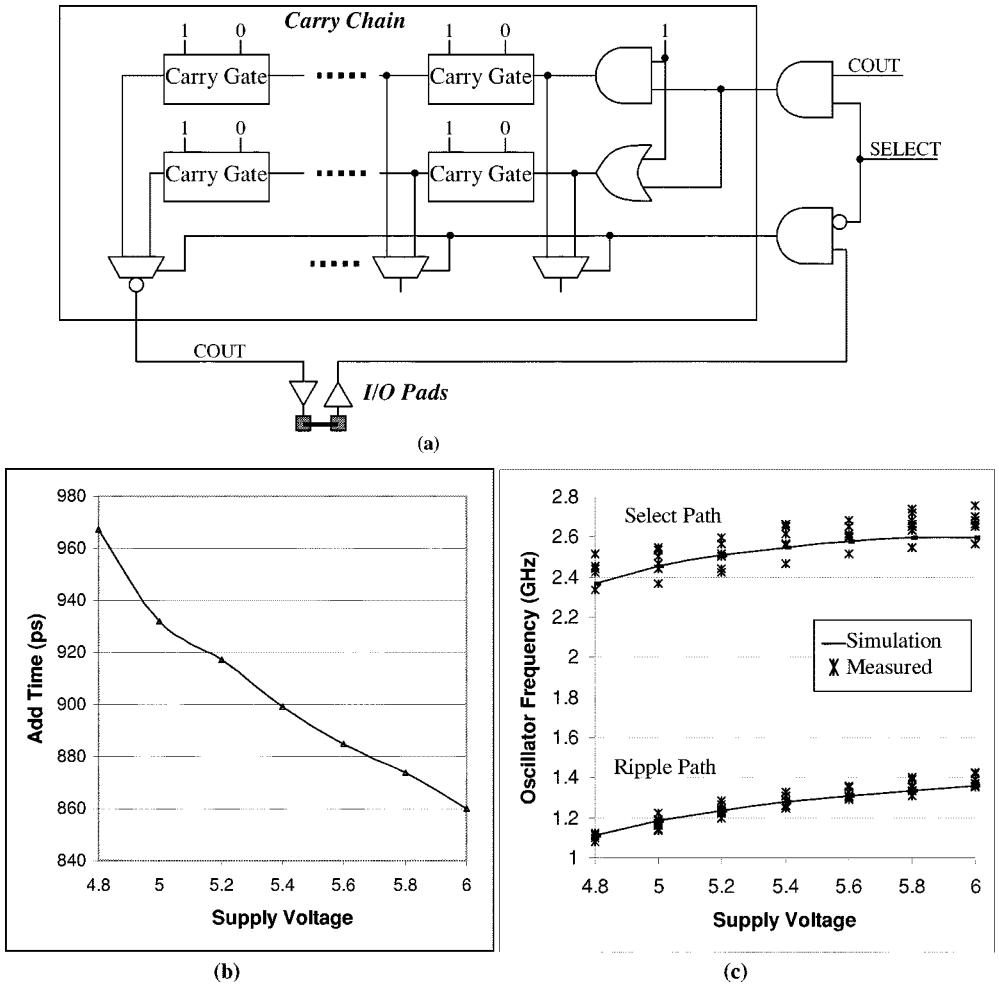


Fig. 11. (a) Carry chain oscillator test circuit. (b) Predicted time necessary to complete 32-bit addition. (c) Measured and simulated values for carry chain oscillator circuit at various supply voltages.

time required for the most significant slice to drive the carry-out to the pad is not part of the critical path reducing the total delay to 885 ps. These results indicate the adder chain requires 426 ps for the pad drivers, the pad receivers, and the MCM delays necessary for the bit-slice design. Therefore, a single chip solution using this adder would require only 459 ps. Of course with a single chip solution, better adder designs that provide higher performance would be possible.

A carry-chain oscillator, shown in Fig. 11(a), was included in a separate test chip to characterize the ALU critical path. Setting the carry-in bit to zero in the test setup forces the carry chain to oscillate through the ripple-carry logic. Likewise, by setting

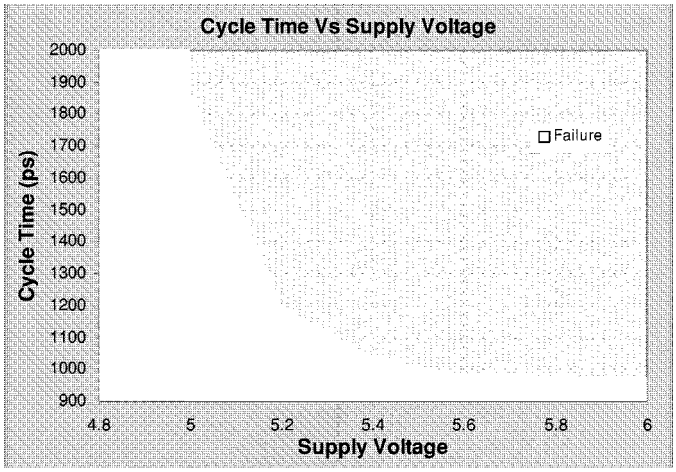


Fig. 12. Cycle time versus supply voltage for 32-bit processor application.

the A operand and carry-in bit to one, the carry chain oscillates through the select path logic. The layout used for the test chip is an identical copy of that used in the datapath. Furthermore, the oscillator loop includes both an output pad and an input pad in the feedback to match the circuits used on the datapath. The only differences between the test chip and datapath implementations of the carry-chain circuits involve control circuitry. Once these differences are accounted for, the carry-chain oscillators can be used to predict time required for the processor to complete an addition operation. Fig. 11(b) shows the time necessary for a 32-bit addition at various supply voltages. Fig. 11(c) shows the SPICE simulations of the carry-chain oscillator match the average measured results on the test chip to 3%, validating the simulation methodology.

VII. Testing and Measured Results

The datapath, instruction decoder, and cache controller chips were designed with an at-speed boundary scan test scheme [8]. The test vector is presented to the internal circuits at the same time the clock is activated. The vector is then run, at speed, for the selected number of clock phases, and the results on the output pads are sampled as the clock is deactivated. Control bits are used to determine, with 100 ps of resolution, when a vector is presented and when it is sampled with respect to the 4-phase generator.

The boundary scan test circuit may also be used to test circuit paths running with the clock in continuous run mode to determine if certain critical paths will make speed. Fig. 5 shows the voltages on the carry-out and branch pads of a datapath chip running a sequence of ADD operations.

The critical paths in the datapath were tested at various supply voltages, and the master clock was varied to determine the maximum operating frequency. Most operational datapath chips function properly with a 2-GHz clock and a -5.4-V supply. This is higher than the designed -5.2-V supply primarily because the results include voltage drop through the test equipment's power distribution network. However, some chips require a -5.6-V supply for similar performance due to processing variations between die. The voltage required for the minimum acceptable die bounds the supply voltage for the multi-chip processor. Fig. 12 shows the cycle time versus the supply voltage for the 32-bit FRISC/G processor using four datapath chips. These results reflect measured operation of the datapath as well as the predicted inter-chip connections necessary for a 32-bit RISC processor application. For a target cycle time of 1 ns, the datapath chips must be supplied with a -5.6 V supply at 2.4 A, resulting in a power dissipation of 13.4 W.

VIII. Conclusions

A byte-slice datapath chip has been designed and tested as an exploratory project for processor development using 9269 AlGaAs/GaAs HBT devices. At 25 °C and -5.6 V, test results show the datapath chip functions with a 2-GHz master clock, and dissipates 13.4 W. Despite the byte-slice design forced by the HBT yields, very high system clock rates are feasible if dense flip-chip packaging is used to minimize delays between the chips of a partitioned processor. The on-chip and off-chip interconnect delays dominate the critical paths, indicating that significantly higher performance levels can be achieved with sufficient yields for single chip solution.

References

[1] R. Huang, D. Nelson, S. Mony, R. Tang, R. Pierson, J. Penney, and R. Sahai, "Manufacturing AlGaAs/GaAs HBT's on 100 mm wafers," in *IEEE GaAs IC Symp.*, Oct. 1993, pp. 345–348.

[2] R. Brown, M. Upton, A. Chandna, T. Huff, T. Mudge, and R. Oettel, "Gallium-arsenide process evaluation based on a RISC microprocessor example," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1030–1036, Oct. 1993.

[3] N. P. Jouppi *et al.*, "A 300-MHz 115-W 32-b bipolar ECL microprocessor," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1152–1166, Nov. 1993.

[4] E. Fox, R. Heemeyer, K. Kiefer, R. Vangen, and S. Whalen, "A 32-bit GaAs microprocessor by CDC," in *Microprocessor Design for GaAs Technology*, V. Milutinovic, Ed. Englewood Cliffs, NJ: Prentice Hall, 1990.

[5] C. K. Tien, K. Lewis, H. Greub, T. Tsen, and J. McDonald, "Design of a 32 b monolithic microprocessor based on GaAs HMESFET technology," *IEEE Trans. VLSI Syst.*, vol. 5, no. 2, pp. 238–243, June 1997.

[6] Y. Harada, W. Hioe, K. Takagi, and U. Kawabe, "The design for a Josephson micro-pipelined processor," *IEEE Trans. Appl. Superconduct.*, vol. 4, no. 2, pp. 97–106, June 1994.

[7] M. Gdula, T. Haller, V. Krishnamurthy, and G. Forman, "High density overlay interconnect (HDI) delivers high frequency performance for GaAs systems," in *Proc. 1993 IEEE MCM Conf.*, Feb. 1993, pp. 33–38.

[8] C. Maier, H. Greub, R. Philhower, S. Steidl, A. Garg, M. Ernest, S. Carlough, P. Campbell, and J. McDonald, "Embedded at-speed testing schemes with low overhead for high speed digital circuits on multi-chip modules," in *IEEE Innovative Systems in Silicon Conf.*, Oct. 1996, pp. 210–216.

[9] A. Garg, Y. Le Coz, H. Greub, R. Iverson, R. Philhower, P. Campbell, C. Maier, S. Steidl, M. Ernest, R. Kraft, S. Carlough, J. Perry, T. Krawczyk, and J. McDonald, "Accurate high-speed performance predictions for full differential current-mode logic: The effect of dielectric anisotropy," *IEEE Trans. Computer-Aided Design*, vol. 18, pp. 212–219, Feb. 1999.

[10] Y. Le Coz and R. Iverson, "A stochastic algorithm for high speed capacitance extraction in integrated circuits," *Solid-State Electron.*, vol. 35, no. 7, pp. 1005–1012, 1992.

[11] H. Greub, J. McDonald, T. Creedon, and T. Yamaguchi, "High-performance standard cell library and modeling technique for differential advanced bipolar current tree logic," *IEEE J. Solid-State Circuits*, vol. 26, pp. 749–762, May 1991.

[12] P. Campbell, H. Greub, A. Garg, S. Steidl, C. Maier, S. Carlough, M. Ernest, R. Philhower, C. Maier, R. Kraft, and J. McDonald, "A very-wide-bandwidth digital VCO using quadature frequency multiplication and division implemented in AlGaAs/GaAs HBTs," *IEEE Trans. VLSI Syst.*, vol. 6, no. 1, pp. 52–55, Mar. 1998.

[13] M. Krishnamoorthy, J. Loy, and J. McDonald, "Optimal differential routing based on finite state machine theory," *VLSI Design*, vol. 9, no. 2, pp. 105–117, 1999.
[14] C. Maier, J. Markevitch, C. Brashears, T. Sippel, E. Cohen, J. Blomgren, J. Ballard, J. Pattin, V. Moldenhauer, J. Thomas, and G. Taylor, "A 533-MHz BiCMOS superscalar RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1625–1634, Nov. 1997.
[15] A. B. Kang and S. Muddu, "An analytic delay model for RLC interconnects," *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 237–240, 1996.
[16] P. Chow, *The MIPS-X RISC Microprocessor*. Norwell, MA: Kluwer, 1989.
[17] K. Nah, R. Philhower, H. Greub, and J. McDonald, "A 500 ps 32×8 register file implemented in GaAs/AlGaAs HBT's," *IEEE GaAs IC Symp.*, pp. 71–74, Oct. 1993.

Steven R. Carlough (S'97–M'00) was born in Port Jefferson, NY, in 1971. He received the B.S., M.S. and Ph.D. degrees in electrical engineering in 1993, 1997, and 2000, respectively, from Rensselaer Polytechnic Institute, Troy, NY.

He recently joined IBM, Poughkeepsie, NY, where he is working on the design of the S/390 fixed-point unit. His research area is processor design using heterojunction bipolar transistor technology. His research interests include high speed circuit design and programmable logic devices.

Robert A. Philhower (S'89–M'92) received the B.E., M.Eng., and Ph.D. degrees in computer and systems engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1986, 1988 and 1993, respectively.

He joined IBM Thomas J. Watson Research Center, Yorktown Heights, NY, in 1993, where he is presently a Research Staff Member. His research interests include high-performance microprocessor design, automated dynamic circuit and physical design and novel processor architectures.

Cliff A. Maier (M'94) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1992, 1994, and 1996, respectively.

He worked at Exponential Technology, San Jose, CA, from 1996 to 1997 as a Floating Point Designer for a high-performance bipolar microprocessor. Since 1997 he has worked for Advanced Micro Devices, Sunnyvale, CA, as a Member of Technical Staff, alternating between high-speed processor design and methodology research. His research has included bipolar circuit design methodologies, GaAs circuit and processor design, high-performance memory subsystem architectures, complex out-of-order processor architectures, physical design methodologies, and static timing and delay calculation algorithms. He has authored or co-authored roughly a dozen papers on testing, bipolar circuits, packaging, and high-speed processor design.

Samuel A. Steidl (S'94) received the B.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1991, and the M.S. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1998. He is currently working toward the Ph.D. degree in electrical engineering at Rensselaer Polytechnic Institute.

His research interests include high performance analog and mixed-signal circuit design.

Peter M. Campbell (S'93–M'97) received the B.S. in electrical engineering from George Washington University, Washington, D.C., in 1990, the M.S. from Northeastern University, Boston, MA, in 1992, and the Ph.D. from Rensselaer Polytechnic Institute, Troy, NY, in 1997.

He joined IBM, East Fishkill, NY, in 1997, where he is presently an Advisory Engineer working on a 1+ GHz floating-point unit in CMOS SOI. His background includes synthesis, testability, microprocessor architectures, circuit design and the impact of physical layout upon performance. His research interests include high-performance microprocessor architectures and high-speed circuit design.

Atul Garg (S'91–M'91) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Kanpur, India, in 1989, and the M.S. and Ph.D. degrees in computer and systems engineering from the Rensselaer Polytechnic Institute, Troy, NY, in 1991 and 1997, respectively.

He joined the Network Products Division at Advanced Micro Devices, Sunnyvale, CA, in 1997. His current interests include VLSI implementations of ultra high-speed digital communication systems and SOC design techniques. His research work contributed to the development of a 50-GHz AlGaAs/GaAs standard cell library, multi-GHz macrocell testchips, low-K interconnect models, and a 1-GHz cycle time 24-chip/250W air-cooled thin-film multichip package.

Kyung-Suc Nah was born in Seoul, Korea, on April 12, 1967. He received the B.S. degree in electrical engineering from the University of Virginia, Charlottesville, VA, in 1984, the M.S. degree in computer and systems engineering and the Ph.D. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1990 and 1994, respectively.

He joined Samsung Semiconductor Division, Kyungki-Do, Korea, as a Senior Engineer in 1994, and since then has participated in the design of analog integrated circuits for HDD PRML read channel chip and IF transceivers for CDMA wireless mobile phone applications.

Matthew W. Ernest (S'95) was born in Lewistown, PA, in 1974. He received the B.S.E.E. and M.S.E.E. in 1994 and 1996, respectively, from Rensselaer Polytechnic Institute, Troy, NY, where he is currently working toward the Ph.D. degree.

His research focuses on high-speed bipolar digital circuits, especially for applications to computer arithmetic and processor design.

Mr. Ernest is a member of the ASSOCIATION FOR COMPUTING MACHINERY.

James R. Loy (M'93) received the B.S. degree from the U.S. Military Academy (West Point), West Point, NY in 1974, the M.S. degree in computer science and the M.E. degree in computer engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1986; the M.A. degree in national security and strategic studies from the U.S. Naval War College in 1987, and the Ph.D. degree in computer engineering from Rensselaer Polytechnic Institute in 1993.

He instructed at West Point from 1987 to 1990, and returned in 1993, where he served as an Associate Professor in the Department of Electrical Engineering and Computer Science. He recently retired from the military and is currently working as Manager of Technology Operations, Tiger Management, L.L.C., in New York, NY. His research interests include VLSI routing algorithms, fuzzy logic, and optical electronic devices.

Dr. Loy served as the Chairman of Mid-Hudson Section of the IEEE in 1996.

Thomas W. Krawczyk, Jr. (S'98) was born in Catskill, NY, in 1973. He received the B.S. degree in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1995, where he is currently working toward the Ph.D. degree.

His research area is in high speed serial communication utilizing SiGe bipolar technology. His main research interests are in analog phase lock loops, bipolar VCO's, and broad-band communications.

Peter F. Curran (S'99) was born in Queens, NY, in 1964. He received the B.S.E.E. degree in 1993 from Rensselaer Polytechnic Institute, Troy, NY, where he is currently working toward the Ph.D. degree.

His research involves high-speed bipolar circuits for communications and computation.

Mr. Curran is a student member of the ASSOCIATION FOR COMPUTING MACHINERY.

Russell P. Kraft received the B.S.E.E., M.S.E.E., and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy, NY, in 1976, 1978, and 1983, respectively. His dissertation was on the optimization of phased ultrasonics and radar arrays for steering by nonlinearly adjusting the element gains and phases.

In 1986, he joined the Center for Manufacturing Productivity, Rensselaer Polytechnic Institute, as a Project Manager and Adjunct Faculty. The research group is now known as the Center for Integrated Electronics & Electronics Manufacturing. His research areas include electronic manufacturing, robotics, metrology, inspection, and fast digital IC design. His teaching responsibilities include control and communication laboratory applications and computer integrated manufacturing systems. In 1983, he was a Senior Controls Engineer at Mechanical Technology Inc., Latham, NY, where he developed vision-based inspection and gauging systems and real-time imbedded combustion controls for automotive and generator stirling engines. He has two patents in the computer-vision area for noncontact gauging and is co-author of several publications in high speed digital design, vision inspection, phased array design, homomorphic signal processing and control system design.

Dr. Kraft is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi and the Machine Vision Association of SME. He is a technical reviewer for the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY - PART C.

Hans J. Greub (M'91) received the Dipl. degree in electrical engineering from the Swiss Federal Institute of Technology, Lausanne, Switzerland, in 1983, and the M.S. and Ph.D. degrees in electrical, computer and systems engineering from Rensselaer Polytechnic Institute (RPI), Troy, NY, in 1985 and 1990, respectively. His studies at RPI were sponsored by a Fulbright Scholarship (M.S.) and a Tek Labs Scholarship (Ph.D.).

He worked as an Assistant Professor in the Electrical, Computer and Systems Department at RPI from 1990 to 1996. In 1996 he joined Intel Corporation, Hillsboro, OR. His research interests include high speed circuit design and computer architectures, and signal integrity analysis for deep sub-micron CMOS technologies. He holds five U.S. patents.

John F. McDonald (M'65) was born in 1942 in Narberth, PA. He received the B.S.E.E. in 1963 from the Massachusetts Institute of Technology (M.I.T.), Cambridge, MA. He received the M.Eng. degree and the Ph.D. degree in engineering and applied science from Yale University, New Haven, CT, in 1965 and 1969, respectively.

He served as a Member of Technical Staff at Bell Labs in 1964. He was an Instructor at Yale University in 1969, and Assistant Professor the following year. In 1974 he joined the faculty at Rensselaer Polytechnic Institute in the Department of Electrical, Computer and Systems engineering as Associate Professor. He was made Full Professor in 1985. He has coauthored 220 refereed articles, roughly one-third of which are archival journal articles, and has been awarded ten patents. His background includes a wide range of topics including communication theory and DSP, computer hardware design, focused electron and ion beam systems, HF and MCM packaging, GaAs/AlGaAs HBT RISC processor design, HBT technology, and VLSI Design and design automation. His current interests are concentrated on SiGe HBT BiCMOS circuit design and VLSI interconnection technology.