Accurate High-Speed Performance Prediction for Full Differential Current-Mode Logic: The Effect of Dielectric Anisotropy


Abstract—Integrated-circuit interconnect characterization is growing in importance as devices become faster and smaller. Along with this trend, interconnect geometry is becoming more complex, consisting of an increasing number of wiring levels. Accurate numerical extraction of three-dimensional (3-D) interconnect capacitance is essential for achieving design targets in the multigigahertz digital regime. Interconnect-capacitance extraction is complicated by the presence of inhomogeneous layers with differing dielectric constant. Dielectric anisotropy as well is common in many low-k polymeric dielectrics used in high-performance IC’s. A CAD procedure using the novel floating random-walk extractor QuickCAP is presented. Our procedure is efficient enough to extract a substantial amount of a chip’s 3-D wiring. We include as well dielectric anisotropy and inhomogeneity. The procedure is not based on effective conductor geometry or on a finite-sized conductor library but rather on the entire 3-D layout, accounting for actual local variations in conductor separations and shapes. We then apply our procedure to an experimental circuit vehicle implemented in AlGaAs/GaAs heterojunction bipolar transistor current-mode logic. This vehicle is used to validate the accuracy of our CAD procedure in predicting circuit speed. Measured and predicted test-capacitor values and ring-oscillator propagation times agreed generally to within 2–4%. To verify results on a larger digital circuit, we analyzed all interconnects in an adder carry-chain oscillator using our procedure. Predicted propagation delays were generally within 3% of measurement.

Index Terms—AlGaAs/GaAs HBT ring oscillators, current mode logic, dielectric anisotropy, floating-random-walk method, IC-interconnect modeling, 3-D capacitance extraction.

I. BACKGROUND AND INTRODUCTION

Advances in digital IC technology have produced faster and smaller devices, resulting in greater integration density and improved performance [1]. Faster devices and signal rise times have, by necessity, placed an emphasis on interconnects when attempting to control critical net propagation delay. Issues involving distributed transmission line modeling, skin-effect loss, substrate slow-wave degradation, crosstalk coupling, and, possibly, radiative electromagnetic effects must be addressed [2].

Wire resistance in scaled interconnects aggravates the propagation-delay and bandwidth problem severely, leading to the process of “reverse scaling” or “nonscaling” of interconnect cross sections. This has resulted in chips with extremely large numbers of interconnect levels—a trend that will continue. Accurate prediction of delay in complex conductor geometry requires taking into account their true three-dimensional (3-D) structure. See, for example, Fig. 1. Proper description of 3-D structure is particularly important when wiring congestion and layout geometry vary substantially. In addition, modern interconnect fabrication processes involve inhomogeneous and possibly anisotropic dielectrics. CAD analysis of these situations can cause substantial error when using capacitance extractors incapable of handling 3-D geometry and inhomogeneous, anisotropic dielectrics.

Three-dimensional effects have been found to be important in any style of high-performance circuit design. However, these effects are particularly important in delay prediction for heterojunction bipolar transistor (HBT) circuits as might be implemented in GaAs [3], [4], SiGe [5], InP [6], or other material systems. A desirable circuit class in these technologies is full-differential current-mode logic (CML) [7]–[9]. An example of this type of circuit is shown in Fig. 2. Differential signaling helps reduce digital switching noise since the current from the power supply is held relatively constant when the input differential signals are skew free. Smaller signal swings of satisfactory noise margin are thus possible. Also, the ability to drive purely capacitive loads is enhanced. CML circuitry dissipates a relatively small amount of dynamic power. On the negative side, differential wiring doubles the number of interconnects, complicating the routing problem [10]. Operating in differential mode can also increase interconnect capacitance by placing the effective ground plane between wires. More important, as can be seen in Fig. 3, odd-mode differential signals tend to be more sensitive to horizontal electric-field lines between conductors. Unwanted horizontal, odd-mode capacitive coupling can be, unfortunately, intensified with anisotropic interlayer dielectrics (ILD’s).

 Manuscript received May 6, 1998; revised September 30, 1998. This work was supported in part by the SRC Center for Advanced Interconnect Science and Technology under Contracts 448.023 and 448.024 and in part by the Defense Advanced Research Project Agency under Contracts ARPA/ARO DAAH04-93-G-0477 and DARPA/ARO DAAL03-90-G-0187. This paper was recommended by Associate Editor K. Mayaram.

A. Garg and C. A. Maier were with the Center for Integrated Electronics and Electronics Manufacturing, Rensselaer Polytechnic Institute, Troy, NY 12180 USA. They are now with Advanced Micro Devices, Sunnyvale, CA 94088 USA.

Y. L. Le Coz, P. M. Campbell, S. A. Steidl, M. W. Ernest, R. P. Kraft, S. R. Carlough, J. W. Perry, T. W. Krawczyk, and J. F. McDonald are with the Center for Integrated Electronics and Electronics Manufacturing, Rensselaer Polytechnic Institute, Troy, NY 12180 USA (e-mail: mcdonald@unix.cie.rpi.edu).

H. J. Greub was with the Center for Integrated Electronics and Electronics Manufacturing, Rensselaer Polytechnic Institute, Troy, NY 12180 USA. He is now with Intel Corporation, Portland, OR 98124 USA.

R. B. Iverson is with Random Logic Corporation, Fairfax, VA 22031 USA.

R. F. Philhower was with the Center for Integrated Electronics and Electronics Manufacturing, Rensselaer Polytechnic Institute, Troy, NY 12180 USA. He is now with IBM, Yorktown Heights, NY 10598 USA.

Publisher Item Identifier S 0278-0070(99)01018-0.
This paper presents the basis of the floating random-walk method for estimating 3-D capacitance and shows how it can be easily modified to handle uniaxial dielectric anisotropy. The second half of this paper concerns various capacitor structures and ring-oscillator modified to handle uniaxial dielectric anisotropy.

II. Capacitance Analysis

We present a floating random-walk method for extracting capacitance in a 3-D conductor geometry. As we have argued, the method must produce accurate estimates in large assemblages of arbitrarily shaped conductors that constitute a substantial amount of chip wiring. We begin this section with a brief review of a newly developed floating random-walk method, on which an extractor, QuickCAP, is based [11]. The method can include inhomogeneous dielectric media. We follow our presentation with a proof involving a simple spatial transformation. The transformation allows us to exactly account for uniaxial dielectric anisotropy by using a single effective isotropic constant along with a mathematical scaling of vertical conductor and dielectric geometry.

A. The Random-Walk Method for Calculating Capacitance [12]

The capacitance matrix of an assembly of conductors involves solution of Laplace’s equation for the electric potential ψ

\[ \nabla^2 \psi = 0. \]  

The floating random-walk method efficiently solves Laplace’s equation [12]. It can be used to directly extract a capacitance matrix for general-assembly conductors within a 3-D domain. Moreover, this method requires no numerical meshing, unlike conventional finite-element and boundary-integral approaches. The absence of mesh generation is one feature enabling the efficient analysis of large numbers of conductors [13].

The electric potential at the center of a 3-D cube can be related to the potential on its surface \( S \), provided there are no conductors or charges lying within. This center potential

\[ \psi(\xi) = \int_S d^3\xi' \ G(\xi' \xi) \psi_s(\xi') \]  

where \( G \) is the Green’s function between the cube-surface point at \( \xi' \) and the center of the cube \( \xi \).

We next consider so-called maximal cubes. These cubes are defined as the largest ones surrounding a point that has no conductors within it. Obviously, the largest such cube will just touch some of the conductors where the value of electric potential is known (in a capacitance calculation), making it possible to evaluate part of the integral (2). The remainder of the cube surface has unknown potentials. However, the unknown potentials can be in turn treated as the center points for second-order maximal cubes—part of the surface of which once again just touches some conductors where potentials are established. The noncontacting points on these surfaces can be used to define third-order maximal cubes, and so forth. Fig. 4 illustrates a two-dimensional (2-D) and 3-D sequence maximal squares and cubes.

Applying Gauss’ law about any particular conductor, one finds the conductor charge

\[ q = \varepsilon \int_G d^3\xi \ E(\xi) \cdot \hat{n}(\xi) \]  

where \( G \) is the enclosing surface with surface points \( \xi \). The electric field \( E \) and outward-normal vector \( \hat{n} \) are defined on the surface as well. The electric field in (3) can be expressed in terms of maximal cubes centered on \( G \)-surface points. It has been shown that [12]

\[ E(\xi) = -\int_S d^3\xi' \ G_E(\xi' \xi) \psi_s(\xi'). \]  

Here, the vector Green’s function \( G_E \) relates electric field to surface potential of maximal cubes \( S(\xi) \) centered on the \( G \) surface points \( \xi \). Substituting (4) into (3), and repeatedly using (2) to represent unknown surface potentials of higher order maximal cubes, yields, in the infinite limit, and expression for \( q \) in terms of known conductor potentials. To obtain the capacitance-matrix element \( c_{nn} \) between the enclosed conductor \( m \) and any other \( n \), we set the conductor \( n \) potential to unity. Remaining conductor potentials, including that of the enclosed conductor \( m \), are all set to zero. Our procedure results in the following infinite series for \( c_{nn} \), that is, charge divided by unity conductor-\( n \) potential:

\[ c_{nn} = \int_G d^3\xi \int_S d^3\xi' G_E(\xi' \xi) \cdot \hat{n}(\xi') + \int_G d^3\xi \int_S d^3\xi' \int_{S(\xi')} d^3\xi'' [G_E(\xi' \xi') G(\xi' \xi'')] \cdot [G_E(\xi' \xi') \cdot \hat{n}(\xi')] G(\xi' \xi'') G(\xi'' \xi''') \cdots. \]  

It is understood in multiple-integral series (5) that maximal-cube surfaces \( S \) coincide with the conductor-\( n \) surface. Maximal-cube surfaces \( \tilde{S} \) do not coincide with any conductor. Monte Carlo evaluation of (5) defines the floating random-walk method. Walks consist of maximal cube “hops” originating with centers on the surface \( G \).
B. Capacitance for Anisotropic Dielectric Media

It is generally accepted that the horizontal (parallel-to-chip-plane) dielectric constant \( \varepsilon_h \) of many polymers, such as polyimide, differs from the vertical (normal-to-chip-plane) constant \( \varepsilon_v \) [14]–[18]. We now furnish a proof resulting in a simple mathematical transformation that converts a medium with a pair of uniaxial dielectric constants \((\varepsilon_h, \varepsilon_v)\) into a single, more convenient, isotropic medium with constant \( \varepsilon' \). The transformation is mathematically exact. A similar result was previously obtained by Szentkuti for the case of a microstrip transmission line [19], [20]. We show here that the technique extends to conductors in arbitrary 3-D, layered dielectric geometry.

Fig. 5 depicts laminated dielectric layers, Each layer has given uniaxial dielectric constants \( \varepsilon_h \) in the \( x \) and \( y \) directions and \( \varepsilon_v \) in the \( z \) direction. Each layer extends infinitely in \( x \) and \( y \). The layers, of course, possibly contain conducting electrodes (interconnect wires) for which intra- and interlayer coupling capacitance is to be found.

We define within any given layer electric potential \( \psi = \psi(r) \), where \( r = [x, y, z] \). Outside conductors, but inside any given layer, \( \psi \) obeys the anisotropic Laplace equation

\[
\varepsilon_h (\psi_{xx} + \psi_{yy}) + \varepsilon_v \psi_{zz} = 0. \tag{6}
\]

The \( x, y, z \) subscripts denote partial differentiation. Equation (6) must satisfy intralayer conductor Dirichlet conditions and interlayer dielectric-interface conditions. We find

\[
\psi = f(r_S), \quad \psi(r_+) = \psi(r_-), \quad \varepsilon_h \psi_x(r_+) = \varepsilon_v \psi_x(r_-). \tag{7}
\]

Above, \( \psi \) is the electric potential at conductor surfaces within the layer of interest, \( r_S \) are coordinate vectors for points on conductor surfaces, and \( r_+ \) and \( r_- \) are coordinate vectors near any dielectric interface just within and just outside, respectively, the layer of interest. We also have \( \varepsilon_v = \varepsilon_v(r_+) \) and \( \varepsilon_h = \varepsilon_h(r_-) \).

Scaling all \( z \) coordinates in (6) and (7) according to

\[
z' = z \sqrt{\frac{\varepsilon_h}{\varepsilon_v}} \tag{8}
\]

produces an isotropic Laplace equation. In the primed, scaled coordinates, we can write

\[
\psi'_{xx} + \psi'_{yy} + \psi'_{zz} = 0 \tag{9}
\]
The thicknesses of the metal and dielectric layers are in the 0–5-

layer is also used as a dielectric for power-supply bypass and special
where

The functions \( \psi(t) = \psi'[t] \) and \( \psi(t_s) = \psi'[t_s] \). We have also defined

as an equivalent, isotropic dielectric constant.

We now show that transformations (8) and (11) do not change capacitance values. By definition

The total charge \( Q \) contained on the conductor is found with Gauss' law as an integral over the enclosing volume \( V \). The integrand of the \( Q \) integral [numerator of (12)] contributes solely at conductor surfaces. The potential difference \( V \) between any electrode pair is a line integral along \( L \). After transformations (8) and (11), we obtain our desired result, shown in (13) at the bottom of the page.

III. FABRICATION PROCESS AND TEST STRUCTURES

Validation of our modeling procedure was achieved with full-differential CML circuits fabricated in Rockwell International’s high-performance HBT AlGaAs/GaAs process. Baseline HBT devices for the process have unity-current-gain frequencies \( f_T \) on the order of 50 GHz in an emitter-up configuration [3]. The minimum-radius device has an emitter area of \( 1.4 \times 3 \) \( \mu \)m\(^2\). For a switching current of 2 mA, unloaded gate delays on the order of 20 ps and rise times of 30–40 ps are possible [4], [21]. The test chip was fabricated on 100-mm wafers [22]. Typical HBT base widths vary from 500 to 1000 \( \mu \)m. Interconnect wiring levels are situated over a 25-mil-thick semiinsulating GaAs substrate, with a ground plane plated on the wafer back side.

The process provides three layers of Au-metal interconnect with a polyimide ILD shown in Fig. 5. Additional Si\(_3\)N\(_4\) layers are used as a lower level insulator and as a top-side moisture barrier. The Si\(_3\)N\(_4\) layer is also used as a dielectric for power-supply bypass and special analog-circuit metal-insulator-metal (MIM) capacitors. A 50-\( \Omega \)/\( \square \) NiCr thin-film layer is available to implement resistors. A 25-mil-thick semiinsulating GaAs substrate lies underneath the interconnect. The thicknesses of the metal and dielectric layers are in the 0–5-\( \mu \)m range.\(^1\) Second- and third-level metals are thicker than first-level to provide low-resistance power-supply busing and global-net routing.

The polyimide used in the process is DuPont 2611, which exhibits a 25% anisotropy. Dielectric anisotropy depends on the orientation of polymer chains relative to the substrate during deposition. The process provided both inhomogeneous and anisotropic dielectric properties, making it suitable for validation test structures. Using conventional capacitance extraction methods, we predicted ring-oscillator frequencies 30–40% greater than those actually observed. The initial prediction error, prior to our QuickCAP correction, consisted of a combination of factors: some due to polyimide anisotropy and some due to the lack of a true 3-D capacitance extractor.

Validation was based on a set of test structures. The test structures included simple capacitors and ring oscillators. Ring oscillators were designed for heightened sensitivity to inhomogeneous and anisotropic ILD. Others were designed to explore typical sensitivity to 3-D conductor-geometry variability. We analyze as well a small complete logic circuit needed in an arithmetic-logic-unit (ALU) design, that is, an adder carry chain.

Fig. 6 is a die microphotograph of the test chip. It is rectangular, measuring 8.2 \( \times \) 6.1 mm\(^2\). The chip contains a number of useful passive and active structures and circuits, including resistors, capacitors, inductors, transmission lines, line-coupling structures, and ring oscillators. As noted in Section I, this work concerns two types of structures: capacitors and ring oscillators.

We have performed measurements and theoretical extractions for a variety of capacitor configurations.

- **Parallel Plate**—formed by sandwiching polyimide dielectric with any two of the available three metal layers (M1, M2, M3). Fig. 7(a) illustrates the parallel-plate geometry. This geometry is useful for establishing vertical (normal-to-chip-plane) dielectric constant. A high-value MIM capacitor is also available between bottom (M1) and middle (M2) metal layers (refer to Fig. 5).

\[ C = \int \frac{dx' dy' (d' / \sqrt{\varepsilon_h / \varepsilon_v}) \left[ k (\psi_{x,t}x' + \psi_{y,t}y') + \varepsilon_v (\sqrt{\varepsilon_h / \varepsilon_v})^2 \psi_{x,t} \right]}{\int \psi_{x,t} dx + \psi_{y,t} dy + (\sqrt{\varepsilon_h / \varepsilon_v}) \psi_{x,t} (d' / \sqrt{\varepsilon_h / \varepsilon_v})} = \int \frac{dx' dy' (d' / \sqrt{\varepsilon_h / \varepsilon_v}) (\psi_{x,t}x' + \psi_{y,t}y' + \psi_{x,t})}{\int \psi_{x,t}x' + \psi_{y,t}y' + \psi_{x,t} dx'} = C' \]
Fig. 8. Microphotograph of a ring-oscillator structure on the HBT test chip at 40x magnification.

MIM-capacitor dielectric consists of a thin layer of Si₃N₄ after removing any intervening polyimide.

- **Finger**—formed within the M1 layer as two interdigitated electrodes. Fig. 7(b) illustrates the finger geometry. This geometry is useful for establishing horizontal (parallel-to-chip-plane) dielectric constant. Because of space limitations on the test chip, finger capacitors were fabricated only on M1.

- **Crossover**—formed similarly to parallel-plate capacitors; the plates, however, are made up of common parallel lines, oriented so that the two plates together produce a cross-wire array. Fig. 7(c) illustrates the cross-wire geometry. This structure is useful for studying complex 3-D fringing fields likely to be encountered in modern multilevel IC’s.

We now turn our attention to the ring-oscillator circuits. We have fabricated eight-stage buffer loops implemented in differential CML. Differential wires connecting the last two stages are exchanged to produce inversion feedback necessary for oscillation. Seven stages have a fanout of one, while one stage has a fanout of two. Differential input voltage levels are 0 and ±250 mV. Three current $I_T$ for our operating circuits is 0.8 mA at a power-supply voltage $V_{CC} = -5.2$ V.

Four of the fabricated oscillators are shown in the microphotograph of Fig. 8. Both buffers and their interconnects are designated. In all, the test chip contained 28 oscillators, consisting of devices shown in the layout of Fig. 8. Devices were connected to interconnect loading structures identical to those shown in Fig. 7.

A total of six classes of 3-D buffer-interconnect environments exist on the test chip. Within any class, interconnect (interstage) wire length was 530, 1218, 1562, or 1906 μm. A single, essentially unloaded ring oscillator with an interconnect length of 15 μm was included, bringing the count to 6 x 4 + 1 = 25 oscillators per chip. Sufficient variation in parasitic interconnect capacitance was therefore ensured. All interconnects for any given oscillator were of identical class and length. Fig. 9 summarizes the various interconnect environments. Note that solid-electrode or parallel-wire planes may exist above the differential interconnects S and Š.

Fig. 9. (a) Schematic of an eight-stage ring-oscillator configuration. (b) Depiction of interconnect capacitive-load structures.

IV. MEASUREMENT AND MODELING

A. Experimental Measurement

Our test-chip wafer was divided into a square array of 25 projected reticle patterns. Each reticle contained two $8.2 \times 6.1$ mm² test chips. A Summit probe station, manufactured by Cascade Microtech, equipped with a microwave coplanar probe was used for test-capacitor measurement. Probe pads were on 150-mm pitch. Single-port s-parameter measurements on the test capacitors were performed using an HP 8510C vector network analyzer, deembedding the probe parasitics. Experimental capacitance values were derived from the extracted circuit model. Our measurement approach allowed capacitance measurement as small as 0.5 pF with an accuracy of 2%.

For ring-oscillator measurements, test-chip wafers were mounted in a Tektronix probe station and secured with a water-cooled vacuum chuck. Wafer temperature was controlled with a MELCOR thermoelectric cooler fitted between wafer and chuck. Cooler surface flatness was less than 1 mil, ensuring sufficient thermal contact with the wafer. A Tektronix 7104 oscilloscope equipped with an 54 sampling head displayed ring-oscillator waveforms. Electrical contact to the test chip was provided with a standard six-channel Cascade Microtech probe (SSPGSSGPSS) pad foot print.

Test chips were designed with the Compass tool suite. PSpice and MATLAB were used for circuit simulation and data fitting. Transistor circuit models were obtained from the process design manual. They were also independently extracted by two-port s-parameter measurement with the HP network analyzer. The small amounts of wire resistance in the Au interconnections were included in the simulations.

B. Capacitors

Measured data for a selection of test-chip parallel-plate, finger (FS), and crossover (CS) capacitors were in the 0.5–10 pF range. A planar interconnect model was generated using dielectric-thickness and metal-sheet-resistivity measurements from parallel-plate capacitors and on-chip metal resistors. The numerically extracted 3-D capacitances for finger and crossover capacitors, based on our planar model, are listed in Table I. Data were obtained with a single approximate isotropic dielectric constant of 3.2 (no anisotropic correction) based on fitting to parallel-plate results. Percent differences between measured and extracted values ranged approximately 6–20%. Anisotropy obviously is not measured with these structures.
TABLE I
COMPARISON OF MEASURED AND NUMERICALLY EXTRACTED CAPACITANCE USING AN ISOTROPIC POLYIMIDE $\varepsilon_r = 3.2$. FS: FINGER, CS: CROSSOVER

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Measured Capacitance (pF)</th>
<th>Anisotropic Model Capacitance (pF)</th>
<th>Difference (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS1 (M1)</td>
<td>0.839</td>
<td>0.752</td>
<td>11.5</td>
</tr>
<tr>
<td>FS2 (M1)</td>
<td>0.792</td>
<td>0.712</td>
<td>11.2</td>
</tr>
<tr>
<td>CS1 (M1/M2)</td>
<td>1.907</td>
<td>1.790</td>
<td>6.5</td>
</tr>
<tr>
<td>CS2 (M1/M2)</td>
<td>2.318</td>
<td>2.114</td>
<td>9.6</td>
</tr>
<tr>
<td>CS3 (M2/M3)</td>
<td>1.896</td>
<td>1.568</td>
<td>20.9</td>
</tr>
</tbody>
</table>

TABLE II
COMPARISON OF MEASURED AND NUMERICALLY EXTRACTED CAPACITANCE USING AN ANISOTROPIC POLYIMIDE $\varepsilon_h = 4.0$ and $\varepsilon_v = 3.2$. NOTE THAT ONLY FINGER AND CROSSOVER CAPACITORS ARE SIGNIFICANTLY AFFECTED BY ANISOTROPY

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Measured Capacitance (pF)</th>
<th>Anisotropic Model Capacitance (pF)</th>
<th>Difference (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FS1 (M1)</td>
<td>0.839</td>
<td>0.839</td>
<td>0.0</td>
</tr>
<tr>
<td>FS2 (M1)</td>
<td>0.792</td>
<td>0.784</td>
<td>1.0</td>
</tr>
<tr>
<td>CS1 (M1/M2)</td>
<td>1.907</td>
<td>1.901</td>
<td>0.3</td>
</tr>
<tr>
<td>CS2 (M1/M2)</td>
<td>2.318</td>
<td>2.399</td>
<td>0.8</td>
</tr>
<tr>
<td>CS3 (M2/M3)</td>
<td>1.896</td>
<td>1.863</td>
<td>1.7</td>
</tr>
</tbody>
</table>

For M1 finger capacitors, capacitance primarily depends on $\varepsilon_h$ for polyimide and $\varepsilon_{SiN}$, however, secondary fringing fields into polyimide and underlayer dielectric give capacitance contributions that depend on both $\varepsilon_h$ and $\varepsilon_v$, the vertical (out-of-plane) dielectric constant. Crossover capacitance is influenced by both $\varepsilon_h$ and $\varepsilon_v$ for polyimide and $\varepsilon_{SiN}$. To obtain good agreement with extracted values for finger and M1/M2 crossover capacitors, we established a 25% polyimide anisotropy $\varepsilon_h = 4.0$ and $\varepsilon_v = 3.2$ [14]–[18].

Table II shows corrected Table I finger and crossover capacitance data. Correction accounts for 3-D effects using QuickCAP and for polyimide anisotropy using the transformations of Section II-B. Percentage differences were less than 2%. Some of these structures are used to identify the anisotropy by adjusting it for fit, while others involve prediction and measurement to confirm it.

C. Ring Oscillators

Table III is a listing of all the types of eight-stage ring oscillators in our study. It includes their load configuration, measured and simulated periods of oscillation, and percentage difference between theory and experiment. Circuit simulations for oscillation period relied on experimentally verified HBT device models. Interconnect capacitance was included during circuit simulation, with our previously determined $\varepsilon_h = 4.0$ and $\varepsilon_v = 3.2$ polyimide-ILD values. Observe that our predicted oscillation periods are within 4% of measurement. Variations in prediction accuracy with structure type are all within this same 4% range.

Fig. 10 is a plot of oscillation period $P$ versus interconnect-load capacitance $C$ per stage. The plot displays measured and simulated data points for the 25 ring-oscillator loads on the test chip. The oscillation period can be written $P = 2N\tau$ for $N$ number of stages and $\tau$ delay per stage. The plot follows the linear relation $P = kC + P_{int}$, where $k$ is a constant slope, $C$ is load capacitance per stage, and the intercept $P_{int}$ is the total unloaded delay $2N\tau$ when $C = 0$. Because of constant-current charging and discharging of CML interconnect capacitance, the constant $k = \Delta V/I_E$, where $\Delta V$ is the differential voltage swing (250 mV) and $I_E$ is the tree current (0.8 mA). $P_{int}$ solely depends on intrinsic device switching speed ($C = 0$).

D. A Practical Application: ALU Carry Chain

The polyimide dielectric model previously developed in analyzing the test chip was applied to a complex, 8-bit, ALU carry-select chain [23], [24]. It was fabricated with the same HBT reticle and process. A logic schematic of this circuit is drawn in Fig. 11. The circuit is implemented in differential CML. The chain can be set into oscillation along either short or long paths for delay measurement. The main characteristics of the carry-chain circuit are summarized in Table IV.
to evaluate 3-D interconnect-capacitance effects in high-speed digital circuits. This process uses polyimide ILD. The chip contained capacitor structures and ring oscillators, which were implemented in full-differential CML. A uniaxial polyimide ILD anisotropy of 25% ($\varepsilon_x = 4.0, \varepsilon_y = 3.2$) was required to fit experiment with theory (QuickCAP) by adjustment of dielectric constants for some test structures while others were evaluated to confirm the predictions. Measured test-capacitor values and ring-oscillator periods were, generally, within several percent of CAD-tool prediction. Our 25% anisotropy model was independently applied to a complex microprocessor ALU carry-chain circuit. Measured and simulated self-oscillation periods of the carry chain were within 3%.

### REFERENCES


On the Design of Optimal Counter-Based Schemes for Test Set Embedding

Dimitri Kagaris and Spyros Tragoudas

Abstract—Counter-based mechanisms have been proposed for use in built-in test set embedding. A single counter or multiple counters may be used with one or multiple seeds. In addition, counters may be combined with ROM's. Each alternative design scenario introduces a difficult combinatorial optimization problem: minimization of the time required to reproduce the test patterns by an appropriate synthesis of the built-in test pattern generator. This paper presents fast synthesis techniques that result in almost optimal designs. For any given circuit, they efficiently determine whether counter-based schemes are applicable as built-in generators for a given circuit. The proposed techniques have been implemented and tested on the ISCAS'85 benchmarks. Comparative studies with a weighted random linear feedback shift register scheme show that counter-based designs may offer good hardware/time solutions.

Index Terms—Algorithms, automatic testing, delay effects, logic circuit testing.

I. INTRODUCTION

The process of built-in test pattern generation (TPG) can be separated (implicitly or explicitly) into two tasks: generation of patterns for the easy-to-detect faults and generation of patterns for the hard-to-detect faults. The first task can be easily handled with a pseudorandom pattern generator like a linear feedback shift register (LFSR). The second task is more difficult and requires some form of a deterministic test pattern generator. In deterministic test pattern generation, the generating mechanism has to take into account in some way each one of the specific patterns (or groups of patterns) that target the hard-to-detect faults. Below we give a brief classification of the deterministic test pattern generation methods (assuming combinational circuits and stuck-at faults with no sequential behavior).

A. A Classification of Deterministic TPG Schemes

There is a great variety of schemes that have been proposed for deterministic TPG. These schemes can be classified under different criteria, such as:

i) Weighting Logic—Mapping Logic: A pseudorandom generator (typically, LFSR) is used as a basic subcomponent. The patterns generated by this generator are then transformed into the target deterministic patterns. The transformation can be done by “weighting” the bit probabilities of the pseudorandom source, or by explicitly “mapping” a subset of the pseudorandom patterns to the target deterministic patterns. Examples in the first category are [7], [20], [24], and [27] and in the second [4], [8], [28], and [30], among others.

ii) Test Length Bound—Fault Coverage Bound: Some schemes give priority to not exceed a prescribed bound on the test...