High-Performance Standard Cell Library and Modeling Technique for Differential Advanced Bipolar Current Tree Logic

Hans J. Greub, Member, IEEE, John F. McDonald, Member, IEEE, Ted Creedon, and Tadanori Yamaguchi

Abstract—A high-performance standard cell library for the Tektronix advanced bipolar process GST1 has been developed. The library is targeted for the 250-MIPS Fast Reduced Instruction Set Computer (FRISC) project. The GST1 devices have a minimal emitter size of 0.6 µm × 2.4 µm and a maximum f<sub>T</sub> of 15.5 GHz. By combining advanced bipolar technology and high-speed differential logic, gate propagation delays of 90 ps can be achieved at a power dissipation of 10 mW. The fastest buffers/inverters have a propagation delay of only 68 ps. A 32-b ALU partitioned into four slices can perform an addition in 3 ns using differential standard cells with improved emitter-follower outputs and fast differential I/O drivers. A modeling technique for high-speed differential current tree logic is introduced. The technique gives accurate timing information and models the transient behavior of current trees.

I. INTRODUCTION

THIS PAPER describes an experimental standard cell library for the advanced bipolar process GST1 under development at Tektronix [1]. The library was designed for the Fast Reduced Instruction Set Computer (FRISC) project [2], [3]. The 32-b processor is partitioned into circuits with a maximum complexity of 1000 current tree gates since the process yield is too low for a single-chip implementation. The standard cell library was optimized for speed to achieve a processor cycle time of 4 ns. Differential ECL logic is used to lower propagation, interconnect delays, and switching noise.

Because of the low targeted complexity, a higher power dissipation could be accepted in the speed versus power trade-off than in previously reported advanced bipolar libraries [4], [5]. The current trees are built out of the smallest GST1 devices with ECL output drivers to lower interconnect loading delays. The resulting standard cells are characterized by a high drive capability combined with a low fan-in load. Each cell is made available with three different output drivers. The drive capability of the ECL output driver circuits was improved to reduce the need for high-power gates.

The transient behavior of the high-speed, high-power cells is not dominated by interconnect capacitance as current starved ECL. Thus transients and glitches intrinsic to the structure of current trees are visible and cannot be simulated with a simple behavioral logic model. A structural modeling technique for high-speed current tree logic has been developed to improve the delay accuracy and to capture transients that could lead to circuit failure.

To reduce I/O delays, high-speed differential drivers and receivers with a low logic swing of ±250 mV are provided besides standard single-ended I/O circuits. The single-ended drivers are ECL 10K compatible and have a voltage swing of 865 mV. Low I/O delays are crucial for the carry propagation in the FRISC data path, which had to be partitioned into four 8-b slices. In particular, the 32-b ALU is on the most critical delay path of the processor and is, therefore, examined in detail.

II. ADVANCED BIPOLAR CIRCUIT TECHNOLOGY

A. Advanced Bipolar Process

The GST1 advanced bipolar n-p-n transistor devices are built with a self-aligned polysilicon emitter–base (E–B) process with a coupling base implant. This results in shallow emitter and base junction depths [6]. Fig. 1 shows the structure of n-p-n devices and polysilicon resistors and Fig. 2 shows a SEM device cross section. The 1-µm trench isolation reduces the collector-to-substrate (C–S) capacitance and increases device density. The smallest devices have an emitter stripe of 0.6 µm × 2.4 µm and can be placed on a dense 8-µm × 12-µm grid. A self-aligned titanium-silicide layer on top of the polysilicon layer for emitter and collector contacts reduces the sheet resistance to 1 Ω/ İz and thereby provides an additional layer for short interconnect. The same polysilicon layer without the silicide is used for resistors. Two gold metal layers with a 4-µm pitch are available for interconnect. The advanced bipolar n-p-n devices have a maximum f<sub>T</sub> of 15.5 GHz [1]. Ring-oscillator delays of 55 ps per stage have been measured. Further, dual 4-b analog-to-digital converters with a performance of 1.5

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H. J. Greub and J. F. McDonald are with the Center for Integrated Electronics, Rensselaer Polytechnic Institute, Troy, NY 12181.

T. Creedon was with the Electronic Systems Laboratory, Tektronix, Inc., Beaverton, OR 97007. He is now with Kestrel Technologies, Lake Oswego, OR 97035.

T. Yamaguchi is with Integrated Circuit Operation, Tektronix, Inc., Beaverton, OR 97007.
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Gs/s have been demonstrated [7]. The dimensions and key parameters of the smallest GST1 device are summarized in Table I.

**B. Current Switch**

Fig. 3 shows the basic building block of current tree logic, the current switch (CSW). The input current into the common-emitter node is switched left or right depending upon the two base voltages. Using a simplified Ebers–Moll model for the bipolar transistor, the dc characteristics of a current switch buffer can be expressed in a closed form [8]. However, the effect of the parasitic emitter and base resistances should be included to obtain a good match. Unfortunately, the analysis does not yield a closed-form solution even if only the emitter resistance $R_e$ is included.

Fig. 4 shows the delay of current switch buffers with and without 500 μm of interconnect capacitance as a function of switching current. The switching current was fixed at 400 μA since increasing the switching current any further would mainly increase power dissipation. The nominal switching current should be set below the optimal current to avoid operation in the region where delays increase rapidly with higher current and power. With a logic swing of ±250 mV and a fan-out of 1, a current-mode logic (CML) buffer has a delay of 64 ps and an emitter-coupled logic (ECL) buffer with an emitter-follower current $I_{ef}$ of 800 μA has a delay of 66 ps. The CML buffer dissipates only 2 mW but has a propagation delay sensitivity $R_s$ of 400 Ω. The delay sensitivity $R_s$ multiplied by the load capacitance $C_L$ gives the incremental gate delay due to interconnect loading. A linear delay dependence is a good approximation for ECL or CML circuits [9]:

$$T_d = T_0 + \Delta T_d = T_0 + R_s C_L.$$  

The ECL buffer has a power dissipation of 10 mW with an $R_s$ of only 119 Ω. To save power, CML is used within standard cells where the interconnect length is short. The nominal voltage swing was fixed at ±250 mV. This drives the current switch well beyond the points with maximum noise margin (gain = 1) and results in a voltage gain of 2.6 at 360 K. The voltage swing is determined by a trade-off between the delay sensitivity to capacitive loading and the desired voltage gain and noise margin of the logic. The current must be fully switched left or right at nominal input voltage levels, otherwise logic level degradation will occur if current switches are cascaded or stacked to build current trees. Fig. 5 shows the buffer delays as a function of logic swing $V_t$. The delays of CML buffers increase rapidly at high logic swings because the devices start to saturate.

The voltage swing is an important characteristic of a logic family since propagation and interconnect delays as well as switching noise increase with $V_t$. The ECL buffer delays with 500 μm of interconnect increase by 17% if the logic swing is changed from differential (±250 mV) to single-ended levels (500 mV). If the interconnect capacitance $C_L$ is large, the incremental gate delay $\Delta t_d$ as a function of the logic swing $V_t$ can be approximated by

$$\Delta t_d = K_\text{f} \frac{V_t}{I} = K_\text{f} R_s C_L.$$  

The constant $K_\text{f}$ can be derived from a sensitivity analysis and depends upon the circuit configuration (ECL = 0.31 for $I = I_{eff}$, CML = 0.65) and the device technology [9]. To lower interconnect loading delays either the logic swing $V_t$ must be lowered or the switching current $I_t$ must be increased. Higher switching current implies, however, higher power dissipation. Hence, a low logic swing is the key to high-speed logic with low power dissipation! The switches must exhibit high gain and generate little switching noise to support low logic swings. Bipolar logic with a logic swing of only 250 mV has a big advantage over CMOS with a logic swing of 3–5 V in this respect.
Fig. 3. Bipolar current switch.

\[ V_t = R \cdot I/q \]
\[ I^+ = I_s \cdot \exp((V^+ - V_c)/V_t) \]
\[ I^- = I_s \cdot \exp((V^- - V_c)/V_t) \]
\[ V_{in} = V^+ + V^- \]
\[ I^+ / I^- = \exp((V^+ - V^-)/V_t) \]
\[ I^+ + I^- = I_0 \]
\[ I^+ = I_0 - (I^- / I^+) \cdot I^+ \]
\[ I^- = I_0 / (1 + I^- / I^+) \]
\[ I^+ = I_0 / (1 + \exp(-V_{in}/V_t)) \]
\[ I^- = I_0 / (1 + \exp(+V_{in}/V_t)) \]
\[ V_m = -I_0 \cdot R / (1 + \exp(-V_{in}/V_t)) \]
\[ V_p = -I_0 \cdot R / (1 + \exp(+V_{in}/V_t)) \]

Fig. 4. CML and ECL buffer delays versus switching current.

Fig. 5. ECL and CML buffer delays versus logic swing.
Fig. 6 shows the switching noise (power) of differential ($V_T = \pm 250$ mV) and single-ended ECL buffers ($V_T = 500$ mV) for a positive and negative signal transition. The single-ended buffer generates considerable switching noise because of its higher logic swing and unbalanced load. Differential ECL logic produces only small switching transients and hence evades the delta-I noise problem common to high-speed logic.

**C. Differential Current Tree Logic**

The high speed and low switching noise of differential logic make it very attractive for bipolar [10], [11] or GaAs logic [12]. Differential GaAs logic is called source-coupled FET logic (SCFL). The high performance and efficient logic implementation of cascaded differential logic trees has led to the development of a similar CMOS logic family at IBM [13], called cascode voltage switch logic (CVSFL).

Fig. 7 shows a differential AND/OR gate with three levels of series gating. An equivalent single-ended gate needs twice the voltage swing to obtain the same noise margin. Twice the voltage swing is sufficient, despite the fact that the generation of the reference voltages is sensitive to supply voltage drops on power rails, because doubling the voltage swing also doubles the maximum gain of the current switch. To obtain twice the voltage swing either the load resistance $R_i$ or the switching current $I_s$ must be increased by a factor of 2:

$$\text{gain}_{\text{max}} = g_m R_i = \frac{I_s}{2V_T} R_i = \frac{V_j}{2V_T}.$$  \hspace{1cm} (1)

The number of switches that can be stacked with standard ECL supply voltages is limited to three for ECL and to four for CML. The input signals for current switches at different levels must be offset by at least one base-emitter junction voltage $V_{BE0} \approx 0.85$ V to avoid saturating the bipolar devices. The nominal logic swing at each level is $\pm 250$ mV.

Since a full current tree with three levels of current switches forms a 3-to-8 decoder, any Boolean function of three variables can be implemented in a single current tree by using collector dotting at the top level. An efficient logic implementation is obtained by eliminating current switches with both collectors connected together and by using collector dotting at level two for intermediate decoding states. A four-input multiplexer gate can also be implemented with a single current tree as shown in Fig. 8.

By using feedback from the outputs of the current tree, data latches with any two-input gate at the input can be implemented as shown in Fig. 9. The feedback signals are taken from the top of the tree rather than from the output because of layout considerations.

Differential signals can be inverted with zero delay and power by exchanging the true and inverted signal pair connections at any input or output port. This reduces the number of cells in the standard cell library since dual gates like AND/OR are physically identical. Dual gates get mapped into the same cell during netlist generation.

Emitter followers are used to increase the drive capability of the gates and to shift output levels. A standard cell can drive only one output level because emitter followers tend to ring if they have to drive outputs at multiple levels. Since most of the power is dissipated in the emitter followers, each logic gate is available with three different strength drivers ($I_{QE1} = 400$, 800, and 1200 $\mu$A).

The propagation delays of differential logic depend upon the path the current takes through the tree. The delay from inputs at a given level to the top of the tree can, therefore, depend upon input signals at higher levels. For example, in the differential AND gate shown in Fig. 7, the delay from the lowest level input depends upon whether the current flows through current switch $S2$ to $q$ or through $S2$ and $S3$ to $q$ or $\bar{q}$. The maximum propagation delays for a medium-power AND gate with a level-one output are 90 ps from level 1, 135 ps from level 2, and 180 ps from level 3. An equivalent three-input single-ended OR gate has a propagation delay of 95 ps for the OR output. The delay sensitivity $R_i$ of a single-ended OR gate is 131 $\Omega$ for the rising edge and 257 $\Omega$ for the falling edge at a power dissipation of 10.5 mW. The medium-power differential AND/OR gate has a power dissipation of 10 mW and a delay sensitivity $R_i$ of only 116 $\Omega$. The differential gate has no decisive speed advantage over the single-ended gate at low loads, but the interconnect delay sensitivity of the differential gate is considerably lower and does not depend upon the signal transition.

While differential logic is faster than single-ended logic due to its low logic swing and can be efficiently implemented with current trees, there are also disadvantages. Twice as many signal interconnections must be routed. This increases the average interconnect length since the width of routing channels and feedthroughs doubles. Further, two emitter followers are needed for every gate, which increases power dissipation. However, differential logic requires no power for inverters or reference voltage generators and its sensitivity towards voltage drops on power rails is low.

Existing CAD tools can easily be modified to support three different signal offset levels, differential signal inversion, and checking for input-level violations that cause saturation in standard cells. However, the designer has to assign signals levels avoiding level violations and keeping the propagation delays on critical paths minimal. The standard cell router should support differential wiring. All differential wires should be routed right next to each other to obtain equal loading on differential nets. Parallel routing of differential signals further reduces crosstalk since crosstalk signals will couple almost equally to both wires and thereby produce mainly common-mode noise, which is largely rejected by current switches.

**D. Emitter Followers and Buffers**

Emitter followers have a tendency to ring, which leads to long settling times. Propagation delays are quite diffi-
Fig. 6. Switching noise of single-ended and differential ECL buffers.

Fig. 7. Differential three-input AND gate.

dicult to model for input signals that arrive while the outputs have not yet settled. Therefore, emitter-follower and level-shifter configurations were developed to obtain faster settling times and lower interconnect delays.

The improved emitter followers have a damping resistor between the differential outputs to reduce ringing, as shown in Fig. 10. For level-2 and -3 emitter followers an $f_0$ doubler circuit is used to reduce ringing and increase driving capability. The damping resistors cause a maximum loss of 20 mV in voltage swing since the current flowing through the emitter–base junction is higher for the transistor with a logic-high output signal. The buffers
Fig. 8. Differential four-input multiplexor.

$$\text{OUT} = W\bar{b} \cdot \text{OUT} + W \cdot (A \text{ XOR } B)$$

Fig. 9. Differential latch with xor inputs.
with the improved differential emitter followers for level 2 and 3 show lower interconnect sensitivities (−21%, −23%). Only the emitter follower for level 1 has an 8 ps higher unloaded propagation delay. However, at high loads the interconnect delays are 17% lower. Without damping resistor the buffer has an underdamped step response with a high overshoot and a long settling time.

Highly loaded emitter followers have largely different rise and fall delays. The rise-time delay is quite small due to the high transconductance $g_m$ of the bipolar devices. The fall time is dominated by the available pull-down current. This leads to highly asymmetrical signal transitions in current-starved ECL.

A special buffer is available for driving long interconnect lines as encountered in clock distribution trees. This super buffer (SBUF1H) has a delay of only 68 ps and a sensitivity $R_s$ of only 60 $\Omega$ at a power dissipation of 12 mW. The SBUF1H circuit shown in Fig. 11 consists of a current switch buffer with a switched current source for the emitter followers. This results in a push–pull output stage with a high pull-down current of 2 mA. Resistor $R_3$ provides damping and keeps a minimal current of 800 $\mu$A flowing through $Q_5$ or $Q_6$. It prevents the high output from slowly charging up to the $V_{cc}$ power level through the base–emitter junctions of the output transistors. The SBUF1H has lower power dissipation and lower interconnect delays than a standard high power buffer, but the fan-in load is three times higher.

### E. Input/Output Circuits

High-speed I/O drivers are especially important in advanced bipolar logic since large circuits need to be partitioned because of power dissipation limits and fabrication yields. Two different types of drivers and receivers are provided as shown in Fig. 12. Single-ended 10K ECL-compatible drivers/receivers have a driver plus receiver delay of 300 ps for a rising edge and 312 ps for a falling edge with an I/O pad capacitance of 1 pF. The driver has the typical unbalanced power dissipation of single-ended drivers. These unbalanced drivers cause considerable delta-I noise because of voltage drops on bondwires and power rails. Therefore, a dedicated power rail $V_{PP}$ (0 V) is used for single-ended drivers to keep the delta-I noise away from the standard cell core.

The high current (16 mA) that is switched on and off by single-ended drivers causes a significant voltage drop on the bondwires, which have an inductance of about 20 pF/mil and are typically 10–15 mils long. Simulations predict 30 mV of delta-I noise for a single-ended I/O driver with a 15-mil bondwire on the $V_{PP}$ power supply. Therefore, only two to three drivers can be supplied with
one $V_{cc}$ power pad else the voltage drop on the bondwire and power rails can cause saturation of the output devices. By using tab bonding or a flip-chip die mount, the power supply inductance could be substantially reduced.

The second driver is a differential open-collector driver with a voltage swing of only $\pm 250$ mV. The two transmission lines are terminated with $50$-ohm resistors to $V_{cc}$. The differential driver plus receiver delay is only 220 ps with a pad capacitance of 1 pF. Differential drivers have the disadvantage of using up two I/O pads, however, since they have lower and balanced power dissipation fewer power pads per driver are required. The receivers use the same circuit configuration as the super buffer to drive the typically long interconnect from the chip periphery to the core. Fig. 13 shows a standard cell test chip with single-ended and differential 1/O cells, a toggle flip-flop, and a
structure to measure interconnect delays of ECL buffers, and a bias voltage generator circuit.

F. ALU Circuit

The 32-b ALU is on a critical path of FRISC since the data path had to be partitioned into four 8-b slices. The ALU has a 3-ns time slot to produce a 32-b result from the arrival of the level-2 operand. The carry select scheme is used to speed up carry propagation. The carry for each slice is calculated in two parallel carry chains, one for an assumed carry-in of one and the other for a carry-in of zero. The actual carry-in of the slice selects only the result of the appropriate carry chain. This reduces the fall-through time for the carry to a receiver, multiplexer, and driver delay if the carry chains have had time to settle. Further, the carry-in signal of the first slice must only be available on chip when the carry chains have settled. The carry select ALU can be implemented with only five current trees per bit as shown in Fig. 14.

The carry propagate gate CARRP1M and the multiplexer with clear MUXCLRIM are medium-power (10 mW) gates since they are on the critical path but drive only short interconnect. The programmable function gate ALUMAC2L generates the Boolean XOR, OR, and function of the two operands. A low-power gate (6 mW) is used since it is not on a critical path. A high-power gate (14 mW) is used for the data latch with XOR inputs DLXOR1H since it has to drive long interconnect and is on a critical path. Differential I/O drivers and receivers are used to minimize the carry fall-through time.

The ALU can perform ADD, AND, OR, and XOR functions. A subtraction is performed by inverting the carry-in and operand B. The output latch DLXOR1H not only latches the result but also generates the sum by performing an XOR of the carry and the XOR of the two input operands generated by the ALUMAC2L gate. Table II shows worst-case propagation delays for a 32-b add based upon SPICE simulations.

The simulation results include an average on-chip interconnect length of 600 μm between the clusters of cells that form a bit slice. The carry-in receiver and carry-out driver are placed right next to each other to avoid routing the carry-in signal all the way across the chip. The four data-path slices are mounted right next to each other on a multichip module. The off-chip interconnect between slices is at most 8 mm long. The microtransmission lines on the multichip module have a polyimide dielectric with an εs of 3.2 resulting in a low interconnect delay of 6 ps/mm. The 32-b ADD delay is the silicon delay plus
three chip-to-chip interconnect delays (3 x 48 ps) resulting in a worst-case delay of 2.79 ns. Assuming the clock skew can be controlled within ±100 ps the ALU can perform a worst-case 32-b add within the allocated 3-ns time slot. By using carry select over a group of 3 and then 5 b the delay of the first slice could be reduced to 850 ps, resulting in a worst-case delay of only 2.446 ps.

G. Standard Cell Library

The following list shows the differential standard cells used for the FRISC project. Many cells map into dual logic gates like AND and OR. Dual cells are available in the schematic library but are mapped onto the same cell during netlist expansion. Further, every input and output port of a differential cell can be inverted at no cost. Most cells are available with three different power levels (a): low power = 6 mW, medium power = 10 mW, high power = 14 mW and with three different output levels (b): level 1, level 2, level 3. Master/slave latches dissipate an additional 2 mW. The library also includes a 32 x 8-b single-port memory cell for the register file of the processor [3], [14].

**Combinational Cells**
- **AND2(p,i)** dual-input AND gate
- **XOR2(p,i)** dual-input XOR gate
- **AND3(p,i)** three-input AND gate
- **XOR3(p,i)** three-input XOR/full adder
- **COMP(p,i)** comparator with enable
- **ANDOR(p,i)** AND/OR gate
- **ALUMAC(p,i)** programmable AND/XOR/OR gate
- **CARRY(p,i)** carry propagate gate

**Multiplexer Cells**
- **MUX2(p,i)** dual-input multiplexer
- **MUXCLR(p,i)** dual-input multiplexer with clear
- **MUX4(p,i)** four-input multiplexer

**Buffers and Level Shifters**
- **BUF(p,i)** buffer
- **SBUFH(p,i)** super buffer
- **LS(p,i)** level shifter

**Storage Cells**
- **SRF(p,i)** set/reset flip-flop
- **DL(p,i)** simple data latch
- **DLC(p,i)** data latch with synchronous clear
- **DLAND(p,i)** data latch with AND gate inputs
- **DLXOR(p,i)** data latch with XOR gate inputs
- **DLMUX(p,i)** data latch with MUX gate inputs
- **MSL(p,i)** master/slave latch
- **MSAND(p,i)** master/slave latch with AND gate inputs
- **MSMUX(p,i)** master/slave latch with MUX gate inputs

**I/O Cells**
- **SEDS** single-ended driver ECL 10K
- **SER** single-ended receiver ECL 10K
- **DD** differential driver
- **DR** differential receiver

**Special Cells**
- **RF32 x 8** 32 x 8-b memory cell
- **SYNC** four-phase clock generator

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### TABLE II

<table>
<thead>
<tr>
<th>Chip/Circuit</th>
<th>Path</th>
<th>Delay</th>
</tr>
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<tbody>
<tr>
<td>SLICE 1</td>
<td>A Op → C₉₃₄</td>
<td>1.196 ns</td>
</tr>
<tr>
<td>SLICE 2</td>
<td>C₉₃₄ → C₉₃₅</td>
<td>0.451 ns</td>
</tr>
<tr>
<td>SLICE 3</td>
<td>C₉₃₅ → C₉₃₆</td>
<td>0.451 ns</td>
</tr>
<tr>
<td>SLICE 4</td>
<td>C₉₃₆ → Sum₃₂</td>
<td>0.550 ns</td>
</tr>
<tr>
<td>32-b ALU</td>
<td>A Op → Sum₃₂</td>
<td>2.648 ns</td>
</tr>
</tbody>
</table>

### TABLE III

<table>
<thead>
<tr>
<th>Typical Logic Delays</th>
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</thead>
<tbody>
<tr>
<td>Current Switch Delay</td>
</tr>
<tr>
<td>Level-1 Output</td>
</tr>
<tr>
<td>Level-2 Output</td>
</tr>
<tr>
<td>Level-3 Output</td>
</tr>
<tr>
<td>Fan-out Penalty per Current Switch</td>
</tr>
</tbody>
</table>

A simple delay model is given to the designer which allows quick evaluation of different circuit configurations. Table III gives approximate delay figures for the current switches and the emitter followers.

The fan-out penalty for a medium-power gate is only 5 ps. However, gates like the four-input multiplexer shown in Fig. 8 can have two current switches connected to the same cell input port. Only one of the current switches can, however, be active. A detailed delay model will be described in the following section. Table IV shows typical interconnect delays.

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III. MODELING OF DIFFERENTIAL CURRENT TREE LOGIC

The design of high-speed digital circuits relies heavily on accurate circuit simulation to detect problems and predict performance before fabrication. For simulation at the circuit level, SPICE provides excellent results, however, its simulation speed is prohibitively slow for large digital circuits. Digital simulators use simple digital models and event-driven timing control [15], which allows simulation of very large circuits. However, most simulators are geared towards CMOS because of its dominance in the market place. As described in [16], single-ended bipolar transistor subcircuits can be mapped into equivalent logic gates that can be simulated on a conventional digital simulator. Another modeling technique transforms the transistor-level circuits into labeled weighed graphs [17] requiring a highly specialized simulation tool.

The model presented here uses a current switch, two or more transistors connected at a common-emitter node, as a model primitive, and allows the simulation of either differential or single-ended circuits. Only the mapping of transistors with a common-emitter node to a current switch is required to generate a simulation model from a device-level (SPICE) description. The structure of the tree models is the same as the physical structure. The current switch primitive can easily be added to digital simulators that support user extensions.
High-speed current tree logic has several properties that needed to be modeled. The signal path and therefore the delay from an input to the output can depend upon input signals at higher levels in the tree. Thus the propagation delays from a certain level input to the output can depend upon the state of other input signals. A simple behavioral model cannot capture these delay dependencies since the delays are calculated in most simulators before the simulation starts. However, they can easily be captured by a structural model based on current switches since the actual signal path through the tree is simulated. The current switch primitive can be described with a simple behavioral model that is easy to implement on most digital simulators. The output of a current tree can be independent of a signal at a lower level. For example, if the lowest input signal of an and current tree is undefined, the output should still be low if any of the other input signals is low. This is very important because most digital simulators set all nodes initially to the undefined state, "x." Further, the treatment of glitches is important for latches. Clock signals generated by a gate with an unsymmetrical tree have short glitches at each differential signal transition. The two signals of a differential pair are both low or both high during the glitch. Latches must be able to capture valid data if the necessary setup and hold times have been observed, even if such glitches occur on clock lines.

A. Digital Current Switch Model

Asymmetrical current trees have nonsimultaneous output signal transitions and transient glitches. The output signals of a tree can be equal during transients even though no output change should occur according to the truth table. If such glitches occur on clock lines latched data can be disturbed. The current switch model must, therefore, handle differential and nondifferential input signal conditions as shown in Fig. 15.

The simulation of differential logic on the current switch level increases the number of nodes and elements in the netlist and will slow down simulations. However, the slower simulation time must be traded off against increased accuracy and the ability to capture transients which might affect circuit performance.

Simulation efficiency could be improved by representing each differential signal pair with a single digital node. The two differential current tree outputs (q, qb) can be converted into a single-ended signal with a differential-to-single-ended converter. This converter marks nondifferential outputs of the current tree with an unknown logic signal. The current switch can be reduced for such a single-ended simulation of differential circuits to a four-terminal device. The single-ended modeling of differential signals reduces the number of nodes, but it requires inverter primitives for differential signal inversion. In the unlikely case that each gate output signal needs to be inverted, the total number of nodes will be larger due to the additional inverters. The single-ended modeling of differential signals makes probing and saving of simulation results more efficient and allows the use of standard fault simulation and test-pattern generation software.

Negative logic is used to represent a current flowing in or out of the common-emitter node or the q and qb output nodes. Both outputs are active if the two inputs are equal and current is flowing into the common-emitter node. Latches would lose data just copied if the current switch connected to the clock signal would output no current for nondifferential inputs. However, if it outputs current on both sides no data is lost as long as the input current switch and the feedback current switch outputs agree. This will be the case as long as the data input is stable. The model will therefore correctly indicate a longer hold time and not loss of data. Sending current on both outputs for a nondifferential input condition reduces

<table>
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<th>Table IV</th>
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<tbody>
<tr>
<td>Interconnect Delays</td>
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<tr>
<td>Offset</td>
</tr>
<tr>
<td>level 1</td>
</tr>
<tr>
<td>level 2</td>
</tr>
<tr>
<td>level 3</td>
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</tbody>
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Extended Truth Table

<table>
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<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>COM INb</td>
<td>Q, qb</td>
</tr>
<tr>
<td>1 ? ?</td>
<td>1 1</td>
</tr>
<tr>
<td>X ? ?</td>
<td>X X</td>
</tr>
<tr>
<td>0 1 0 0 1</td>
<td></td>
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<tr>
<td>0 0 1 1 0</td>
<td></td>
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<tr>
<td>0 0 0 0 0</td>
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</tr>
<tr>
<td>0 X X 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 T 0 1</td>
<td></td>
</tr>
<tr>
<td>0 0 T 1 0</td>
<td></td>
</tr>
<tr>
<td>0 T T 0 0</td>
<td></td>
</tr>
<tr>
<td>0 X T 0 0</td>
<td></td>
</tr>
</tbody>
</table>

X=undefined, T=threshold, ?=output | 0, 1, X, T |
COM, Q, qB represent current levels (low=0, high=1) |
Signal Strength: low > high

Fig. 15. Digital current switch model.

<p>| Table V |</p>
<table>
<thead>
<tr>
<th>Parameters of Current Switch Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cc</td>
</tr>
<tr>
<td>Cr</td>
</tr>
<tr>
<td>Cg</td>
</tr>
<tr>
<td>Td</td>
</tr>
</tbody>
</table>
modeling pessimism in general since the tree output might not depend upon which way the current flows for a given set of input signal states.

The current switch model uses only a simple inertial delay model with capacitive load delays. If at least four signal strength values are available, the signal strength can be used to mark signal levels, which allows the detection of level violations causing saturation. The model includes capacitors to model input and output loading. It assumes differential input signals since the base capacitors are physically between base and emitter and can only be modeled as shown for differential input signals. However, most digital simulators support only capacitors connected to ground. The model parameters (Table V) depend on the operating conditions of the current switch like the switching current $I_s$, the voltage swing at the output, and $V_{CEO}$ of the transistors. The capacitor $C_p$ is 20% larger in an active current switch. This represents a dynamic load change that is hard to simulate. However, it will be shown that a simple current switch model for all three levels can give excellent results since the dependencies are intrinsically small. In order to see the small differences the digital simulator would have to be run with a time step $\Delta t$ below 5 ps. The match to a current switch at level 1 is most important since long and therefore critical signals are routed preferably on the topmost level to reduce propagation delays. The biggest simulation error is introduced by using a fixed $C_p$. Table V shows the parameters for the current switch with $I_s = 400 \, \mu A$, $V_t = 250 \, mV$, and $V_{CEO} = 0.85 \, V$.

B. Modeling of Current Trees

Figs. 16 and 17 show a comparison of SPICE simulation results with a digital simulation of a three-input XOR tree and an AND/OR tree. The match for the symmetrical XOR
Table VI

<table>
<thead>
<tr>
<th>PATH</th>
<th>SPICE</th>
<th>FASTSIM Δt = 1 ps</th>
<th>FASTSIM Δt = 5 ps</th>
<th>FASTSIM Δt = 25 ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Op → C_{out}</td>
<td>1196 ps</td>
<td>1185 ps</td>
<td>1185 ps</td>
<td>1300 ps</td>
</tr>
<tr>
<td>C_{out} → C_{out}</td>
<td>451 ps</td>
<td>448 ps</td>
<td>450 ps</td>
<td>475 ps</td>
</tr>
<tr>
<td>C_{in} → Sum</td>
<td>550 ps</td>
<td>567 ps</td>
<td>570 ps</td>
<td>550 ps</td>
</tr>
</tbody>
</table>

Fig. 18. Glich of three-input and tree.

C. Modeling Accuracy Compared to SPICE

For verification of the accuracy of the standard cell models, the ALU slice shown in Fig. 14 was modeled with SPICE and FASTSIM, a digital simulator from Tektronix. Current switch and level-shifter primitives were added through its C-language interface. Table VI shows that excellent agreement (4% deviation) is possible. However, the digital simulator must be run with a sufficiently small time step (5 ps) to avoid the accumulation of rounding errors. The delay sensitivities towards interconnect capacitance were extracted from SPICE data by a six point linear regression analysis in the range 0–500 fF.

IV. CONCLUSION

An experimental standard cell library with a typical gate delay of 90 ps for a 10-mW gate has been developed. High performance is achieved by combining advanced bipolar technology and differential current tree logic design. Interconnect delay sensitivities have been reduced by using low differential logic swings of ±250 mV and improved ECL output drivers and buffers. Power and performance has been improved by providing different output drivers for each cell such that speed versus power can be traded off for every signal.

I/O delays can be significantly reduced by using high-speed differential drivers with a low logic swing of ±250 mV and multiplexing packaging. Differential I/O circuits consume further less power and are balanced, thereby avoiding delta-I noise problems.

Modeling differential logic at the current switch level gives excellent delay accuracy and allows the designer to capture transients and glitches that could cause circuit failure. Further, the modeling approach can be implemented on conventional digital simulators.

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REFERENCES

Since November 1990 he has been a Visiting Assistant Professor at Rensselaer Polytechnic Institute. His research interests include high-speed digital circuits, logic design, and reduced instruction set architectures. He holds three patents.

John F. McDonald (S’63–M’71) was born on January 14, 1942 in Narberth, PA. He received the B.S.E.E. degree from the Massachusetts Institute of Technology, Cambridge, in 1963, the M.Eng. degree from Yale University, New Haven, CT, in 1965, and the Ph.D. degree from Yale University in 1969. He spent a brief period as a Member of the Technical Staff at Bell Laboratories in 1965. He held the position of lecturer at Yale University in 1969 and was appointed Assistant Professor there in 1970. In 1974 he joined Rensselaer Polytechnic Institute, Troy, NY, as an Associate Professor, where he is currently a full Professor in the Department of Electrical, Computer and Systems Engineering. He was one of the founding members of the RPI Center for Integrated Electronics in 1980. His publication record consists of roughly 150 articles, approximately a third of which are journal articles. He holds six patents, and an additional eight disclosures. His interests include VLSI and computer design, with emphasis on very high-speed electronic packaging and GaAs RISC processors.

Dr. McDonald is listed in 24 compilations of technical recognition, including Who’s Who in the World and American Men and Women of Science.

Ted Creeden was with Tektronix Research Labs in Beaverton, OR. He is now President of Kestrel Technologies in Lake Oswego, OR. Kestrel manufactures R&D RF probe stations and has developed low-cost RF probes for 1-ns FRISC device and slice characterization.

Tadanori Yamaguchi received the B.S. degree in electrical engineering from Miyakonojo Institute of Technology, Japan, in 1969.

In 1969 he joined Sony Corporation, Japan, where he worked on wafer processing and device characterization of high-frequency bipolar and MOS transistors. From 1971 to 1976 he was engaged in research and development of exploratory MOS devices and process technologies. His main accomplishments were nonvolatile MAOS memory devices and integrated circuits (MAOS EPROM), continuously variable threshold-voltage MOS devices, ion implantation for MOS devices, resistive-gate charge-transfer devices, and CMOS integrated circuit technology using SIPOS film. Since 1977 he has been with Tektronix, Inc., Beaverton, OR, where he developed a new approach for submicrometer-channel NMOS device technology, a 1000-V NMOS-IC technology, a 2-μm double-layer metal CMOS-VLSI technology, latch-up-free submicrometer-channel CMOS devices using deep-trench isolation and self-aligned TSI2 technologies, and worked on small-gamma MOS device characterization and modeling. Currently, he is a manager of the Advanced Technology Development Department at Tektronix, where he has developed and directed high-speed self-aligned double-polysilicon bipolar and BiCMOS technologies and integrated circuits. He holds eight U.S. patents, and has published and presented over 60 technical papers including several invitational seminars.

Hans J. Greub received the diploma in electrical engineering from the Swiss Federal Institute of Technology in December 1983. He received the Master’s degree in 1985 and the Ph.D. degree in 1990 from Rensselaer Polytechnic Institute in Troy, NY. He studied at Rensselaer Polytechnic Institute with the aid of a Fulbright and a Tek Labs Scholarship. During his Ph.D. studies he spent a year at Tektronix, Inc. in Beaverton, OR, working on advanced bipolar circuit design.


